M52767FP

PLL-SPLIT VIF/SIF

DESCRIPTION

M52767FP is a semiconductor integrated circuit consisting of VIF/SIF signal processing for CTVs and VCRs. M52767FP provide low cost and high performance system with the coil-less AFT.

FEATURES

- Coil-less AFT.
- PLL FM demodulation for Audio. No external parts and adjustment.
- The PLL-SPLIT system provides good sound sensitivity and reduces buzz.
- Video output is 1.3Vp-p through EQ AMP.
- Easy to add Buzz canceler.
- Hi speed IF AGC.
- Built-in QIF AGC.
- Improve over modulation characteristics and Vcc ripple rejection.

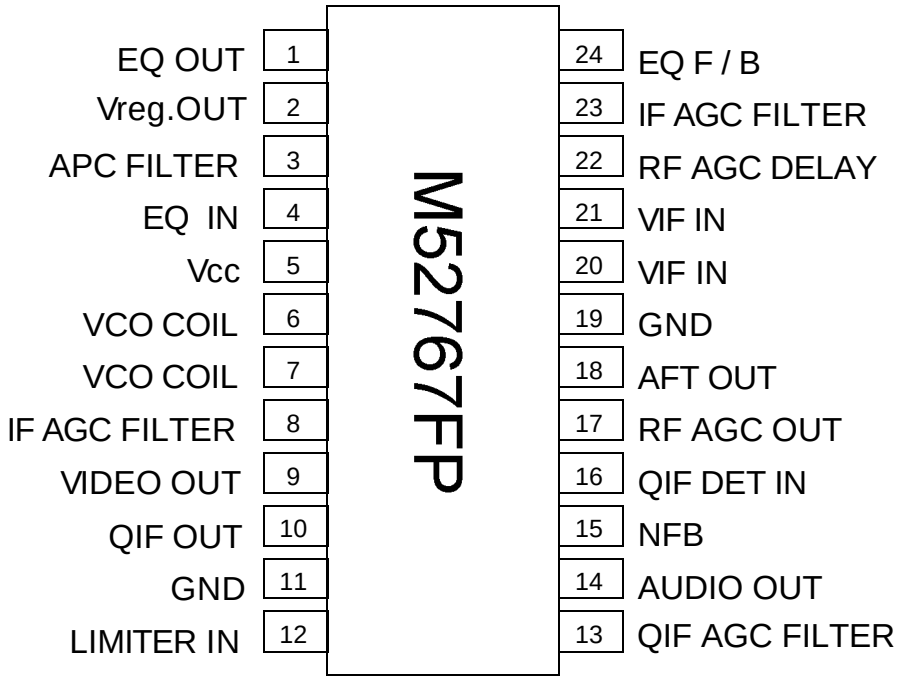
RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range (Vcc) • • • • • • • • 4.7 to 5.3 V
Rated Supply Voltage (Vcc) • • • • • • • • 5.0 V

APPLICATION

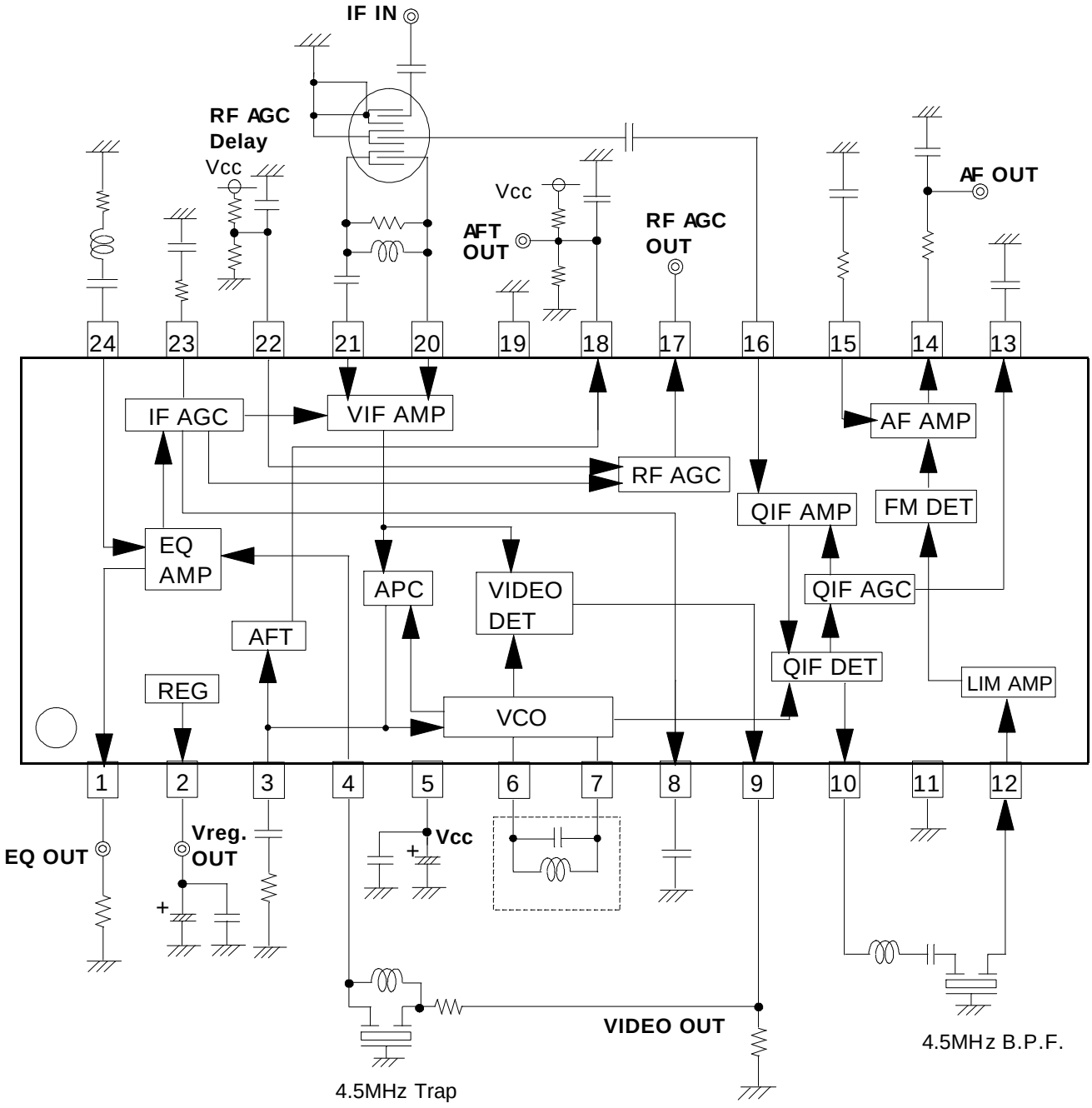
TV,VTR

PIN CONFIGURATION (TOP VIEW)



24pin SSOP

BLOCK DIAGRAM and PERIPHERAL CIRCUIT

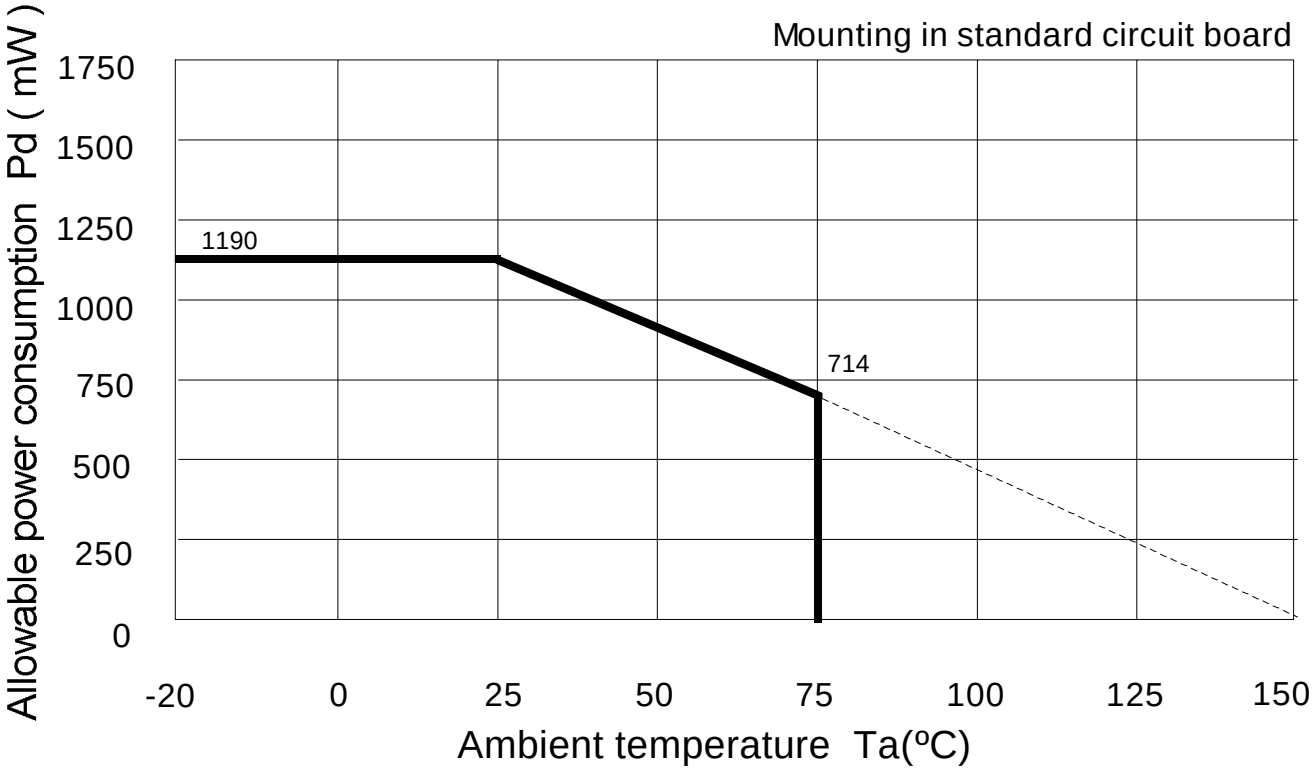


ABSOLUTE MAXIMUM RATINGS

(Ta = 25ºC, unless otherwise noted)

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage 1	Vcc	6.0	V	
Power Consumption	Pd	1190	mW	
Operating Temperature	Topr	-20 to +75	ºC	
Storage Temperature	Tstg	-40 to +150	ºC	

Temperature Characteristics (maximum ratings)



ELECTRICAL CHARACTERISTICS

VIF Section (Vcc=5V,Ta=25ºC unless otherwise noted)

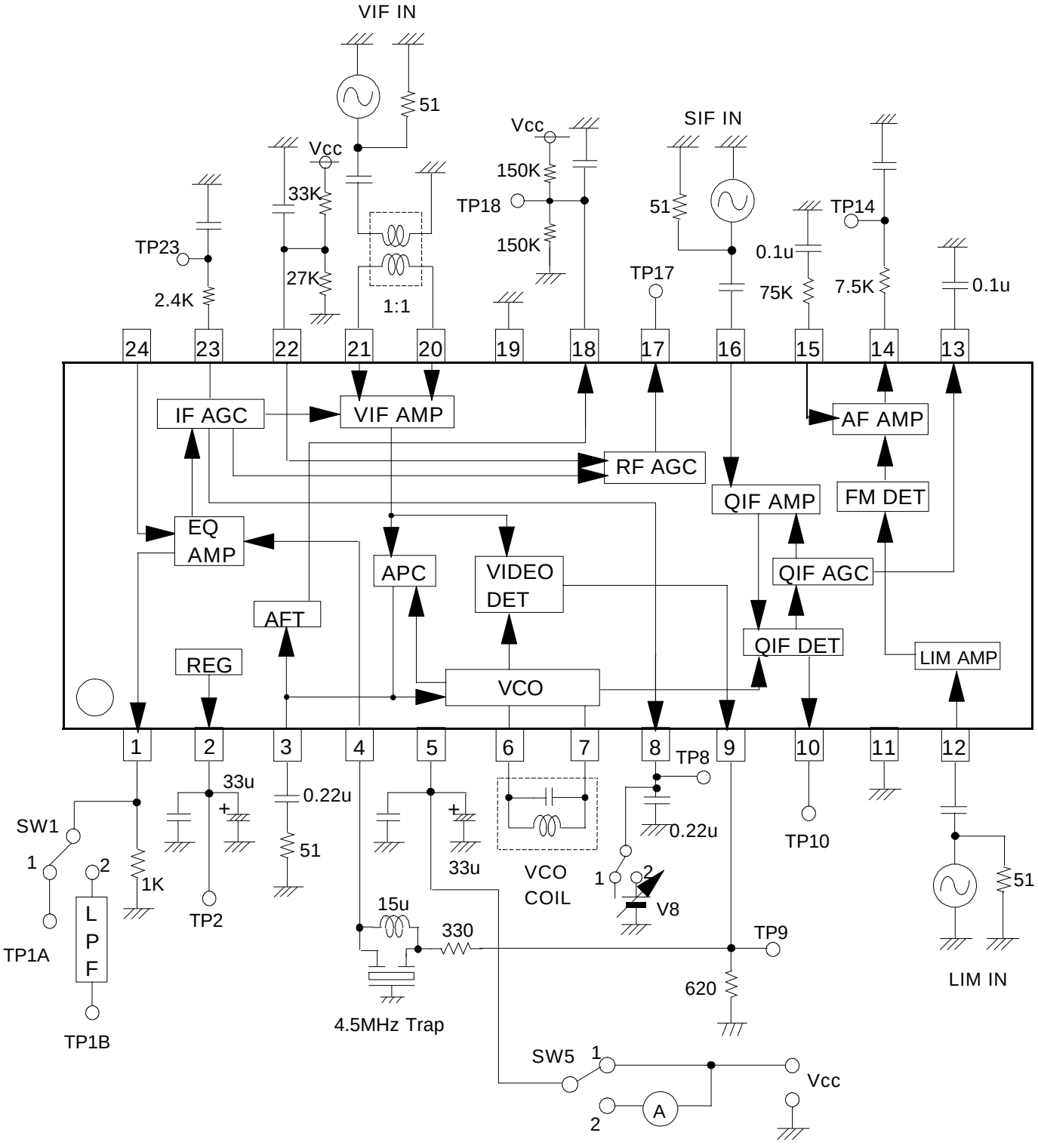
No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
1	Circuit Current 1 Vcc=5V	Icc1	1	A	-	-	SW5=2	36	45	54	mA	
2	Vreg. Output Voltage	Vreg.	1	TP2	-	-		3.2	3.5	3.8	V	
3	Video Output Voltage 9	Vo det9	1	TP9	VIF IN	SG1		0.46	0.6	0.74	Vp-p	
4	Video Output Voltage 1	Vo det	1	TP1A	VIF IN	SG1		1.0	1.3	1.6	Vp-p	
5	Video S/N	Video S/N	1	TP1B	VIF IN	SG2	SW1=2	51	56	–	dB	1
6	Video Band Width	BW	1	TP1A	VIF IN	SG3	SW8=2 V8=Variable	5.0	7.0	–	MHz	2
7	Input Sensitivity	VIN MIN	1	TP1A	VIF IN	SG4		–	48	52	dBµ	3
8	Maximum Allowable Input	VIN MAX	1	TP1A	VIF IN	SG5		104	110	–	dBµ	4
9	AGC Control Range Input	GR	-	-	-	-		55	62	–	dB	5
10	IF AGC Voltage 1	V8	1	TP8	VIF IN	SG6		2.8	3.1	3.4	V	
11	IF AGC Voltage 2	V23	1	TP23	VIF IN	SG6		2.8	3.1	3.4	V	
12	Maximum RF AGC Voltage	V17H	1	TP17	VIF IN	SG6		4.1	4.7	–	V	
13	Minimum RF AGC Voltage	V17L	1	TP17	VIF IN	SG7		–	0.1	0.5	V	
14	RF AGC Delay Point	V17	1	TP17	VIF IN	SG8		86	89	92	dBµ	6
15	Capture Range U	CL-U	1	TP1A	VIF IN	SG9		1.0	1.5	–	MHz	7
16	Capture Range L	CL-L	1	TP1A	VIF IN	SG9		1.4	2.0	–	MHz	8
17	Capture Range T	CL-T	-	-	-	-		2.7	3.5	–	MHz	9

No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
18	AFT Sensitivity	μ	1	TP18	VIF IN	SG10		20	30	70	mV/kHz	10
19	AFT Maximum Voltage	V18H	1	TP18	VIF IN	SG10		3.85	4.15	–	V	10
20	AFT Minimum Voltage	V18L	1	TP18	VIF IN	SG10		–	0.7	1.2	V	10
21	AFT defeat	AFT def 1	1	TP18	VIF IN	-		2.2	2.5	2.8	V	
22	Inter Modulation	IM	1	TP1A	VIF IN	SG11	SW8=2 V8=Variable	35	40	–	dB	11
23	Differential Gain	DG	1	TP1A	VIF IN	SG12		–	2	5	%	
24	Differential Phase	DP	1	TP1A	VIF IN	SG12		–	2	5	deg	
25	Sync. tip level	V1 SYNC	1	TP1A	VIF IN	SG2		0.8	1.1	1.4	V	

SIF Section (Vcc=5V,Ta=25ºC unless otherwise noted)

No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
26	QIF Output Voltage 1	QIF1	1	TP10	VIF IN QIF IN	SG2 SG13		94	100	106	dBµ	
27	QIF Output Voltage 2	QIF2	1	TP10	VIF IN QIF IN	SG2 SG14		94	100	106	dBµ	
28	SIF Detection Output	Vos	1	TP10	VIF IN	SG15		86	92	98	dBµ	
29	AF Output (4.5MHz)	VoAF 1	1	TP14	SIF IN	SG16		460	680	1000	mVrms	
30	AFOutput Distortion (4.5MHz)	THD AF 1	1	TP14	SIF IN	SG16		–	0.3	0.9	%	
31	Limiting Sensitivity (4.5MHz)	LIM 1	1	TP14	SIF IN	SG17		–	42	55	dBµ	12
32	AM Rejection (4.5MHz)	AMR 1	1	TP14	SIF IN	SG18		55	62	–	dB	13
33	AF S/N (4.5MHz)	AF S/N 1	1	TP14	SIF IN	SG19		55	62	–	dB	14

Measuring Circuit Diagram



Note 1) All the capacitors are 0.01µF, unless otherwise noted.

2) The Measuring Circuit is Mitsubishi standard evaluation fixture.

INPUT SIGNAL

SG	50Ω Termination
1	f_0 = 45.75 MHz AM 20 KHz 77.8 % 90 dBμ
2	f_0 = 45.75 MHz 90 dBμ Cw
3	f_1 = 45.75 MHz 90 dBμ Cw f_2 = Frequency Variable 70 dBμ Cw } Mixed Signal
4	f_0 = 45.75 MHz AM 20 KHz 77.8% Level Variable
5	f_0 = 45.75 MHz AM 20 KHz 14.0% Level Variable
6	f_0= 45.75 MHz 80 dBμ Cw
7	f_0 = 45.75 MHz 110 dBμ Cw
8	f_0 = 45.75 MHz Cw Level Variable
9	f_0 = Frequency Variable AM 20 KHz 77.8 % 90 dBμ
10	f_0 = Frequency Variable 90 dBμ Cw
11	f_1 = 45.75 MHz 90 dBμ Cw f_2 = 42.17 MHz 80 dBμ Cw } Mixed Signal f_3 = 41.25 MHz 80 dBμ Cw
12	f_0 = 45.75 MHz 87.5 % TV modulation Ten-step waveform Sync Tip Level 90 dBμ
13	f_1 = 41.25 MHz 95 dBμ Cw
14	f_1 = 41.25 MHz 75 dBμ Cw
15	f_1 = 45.75 MHz 90 dBμ Cw f_2 = 41.25 MHz 70 dBμ Cw } Mixed Signal
16	f_0 = 4.5 MHz 90 dBμ FM 400 Hz ±25 KHzdev
17	f_0 = 4.5 MHz Level Variable FM 400Hz ±25KHzdev
18	f_0 = 4.5 MHz 90 dBμ AM 400 Hz 30 %
19	f_0 = 4.5 MHz 90 dBμ Cw
20	f_0 = 4.5 MHz Level Variable Cw

Notes

1. Video S/N

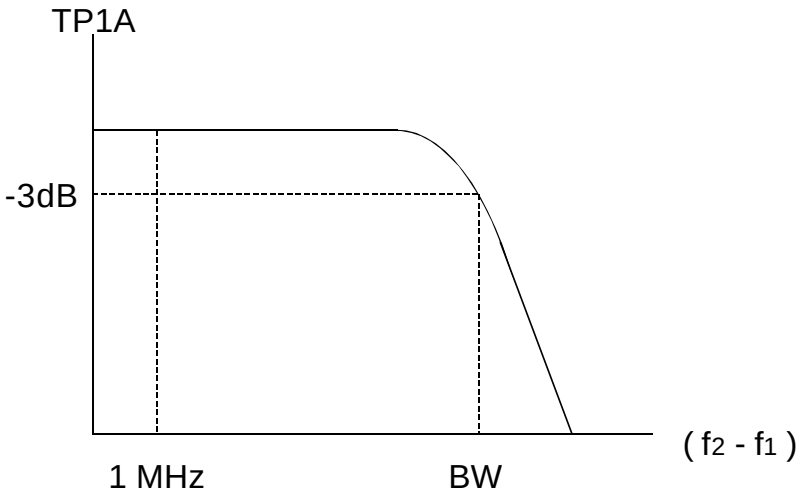
Input SG2 to VIF IN and measure the video out(Pin 1) noise in r.m.s at TP1B through a 5MHz (-3dB) L.P.F.

$$S/N=20\log\left(\frac{0.7\times Vo\ det}{NOISE}\right)\quad [dB]$$

2. Video Band Width: BW

1. Measure the 1MHz component level of Video output TP1A with a spectrum analyzer when SG3(f_2=44.75MHz) is input to VIF IN. At that time, measure the voltage at TP8 with SW8, set to position 2, and then fix V8 at that voltage.

2. Reduce f_2 and measure the value of (f_2-f_1) when the (f_2-f_1) component level reaches -3dB from the 1MHz component level as shown below.



3. Input Sensitivity: VIN MIN

Input SG4 (Vi=90dBμ) to VIF IN , and then gradually reduce Vi and measure the input level when the 20KHz component of Video output TP1A reaches -3dB from Vo det level.

4. Maximum Allowable Input: VIN MAX

1. Input SG5 (Vi=90dBμ) to VIF IN , and measure the level of the 20KHz component of Video output.

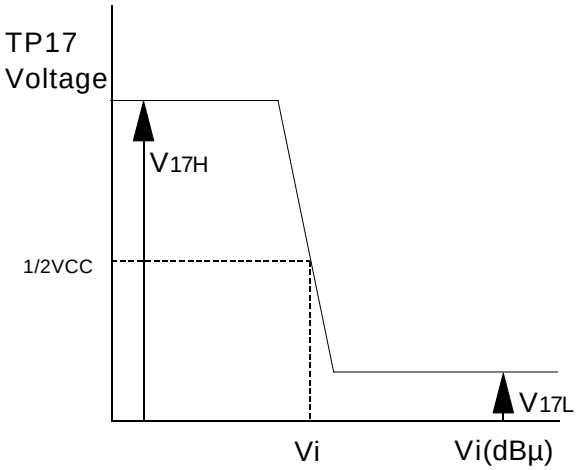
2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.

5. AGC Control Range: GR

GR = VIN MAX - VIN MIN [dB]

6. RF AGC Operating Voltage: V17

Input SG8 to VIF IN and gradually reduce Vi and then measure the input level when RF AGC output TP17 reaches 1/2 VCC, as shown below.



7. Capture range: CL - U

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. And decrease the frequency of SG9 and measure the frequency fU when the VCO is locked.

CL - U = fU - 45.75 [MHz]

8. Capture range: CL - L

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. And increase the frequency of SG9 and measure the frequency fL when the VCO is locked.

CL - L = 45.75 - fL [MHz]

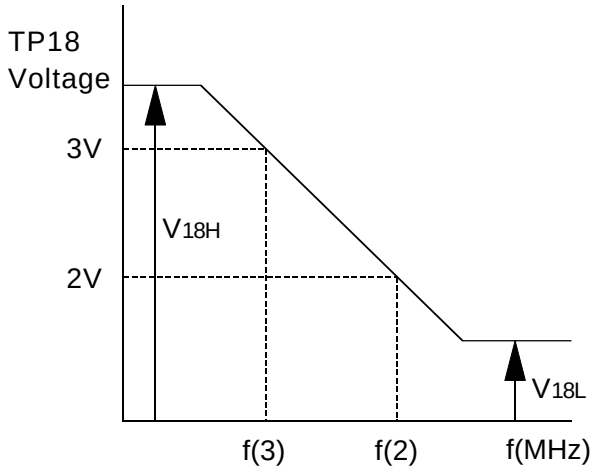
9. Capture range: CL - T

CL - T = CL - U + CL - L [MHz]

10. AFT sensitivity μ, Maximum AFT voltage V_{18H} , Minimum AFT voltage V_{18L}

1. Input SG10 to VIF IN , and set the frequency of SG10 so that the voltage of AFT output TP18 is 3[V] . This frequency is named f(3).
2. Set the frequency of SG10 so that the AFT output voltage is 2[V]. This frequency is named f(2)
3. IN the graph, maximum and minimum DC voltage are V_{18H} and V_{18L}, respectively.

$$\mu = \frac{1000 \quad [mV]}{f(2) - f(3) \quad [kHz]} \quad [mV/kHz]$$



11. Inter modulation: IM

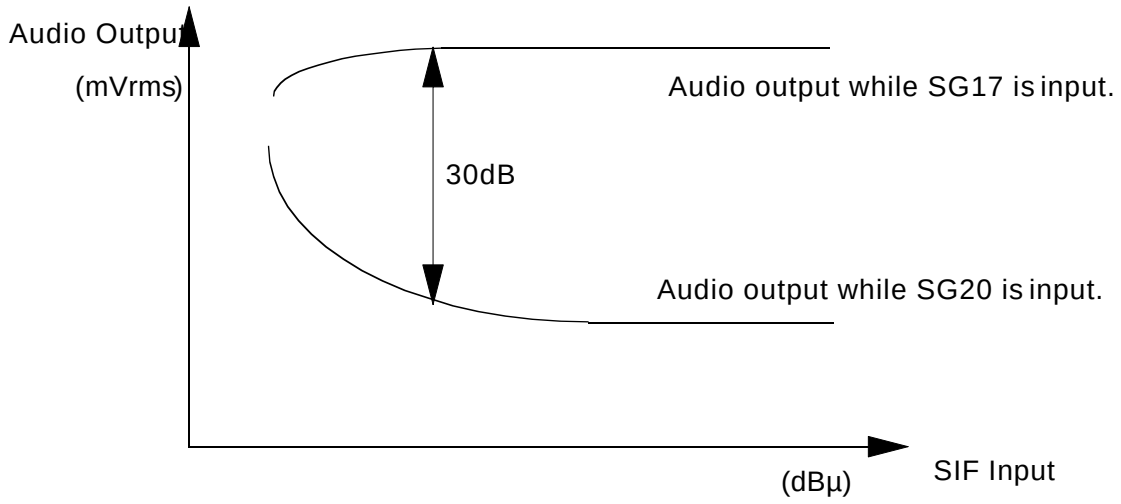
1. Input SG11 to VIF IN, and measure video output TP9 with an oscilloscope.
2. Adjust AGC filter voltage V23 so that the minimum DC level of the output waveform is 1.5V.
3. At this time, measure TP9 with a spectrum analyzer . The inter modulation is defined as a difference between 0.92MHz and 3.58 MHz frequency components.

12. Limiting Sensitivity: LIM

1. Input SG17 to SIF IN, and measure the 400Hz component level of AF output TP14.

2. Input SG20 to SIF IN, and measure the 400Hz component level of AF output TP14 .

3. The input limiting sensitivity is defined as the input level when a difference between each 400Hz components of audio output (TP14) is 30dB, as shown below.



13. AM Rejection: AMR

1. Input SG18 to SIF IN ,and measure the output level of Audio output (TP14). This level is named VAM.

2. AMR is;

$$AMR = 20\log\left(\frac{VoAF\ (mVr.m.s)}{VAM\ (mVr.m.s)}\right) \quad [dB]$$

14. AF S/N: AF S/N

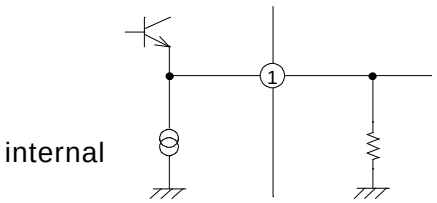
1. Input SG19 to SIF IN ,and measure the output noise level of Audio output (TP14). This level is named VN.

2. S/N is;

$$S/N = 20\log\left(\frac{VoAF\ (mVr.m.s)}{VN\ (mVr.m.s)}\right) \quad [dB]$$

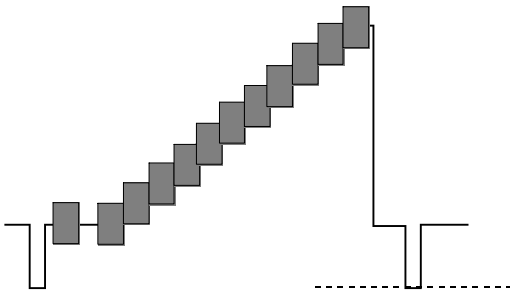
Pin peripheral circuit explanation

Pin 1 (EQ OUTPUT)

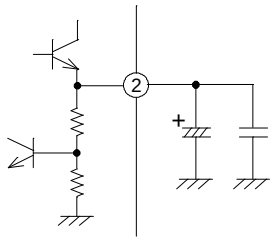


driving current : 1mA

An output amplitude is positive 1.3Vp-p in case of 87.5% video modulation.

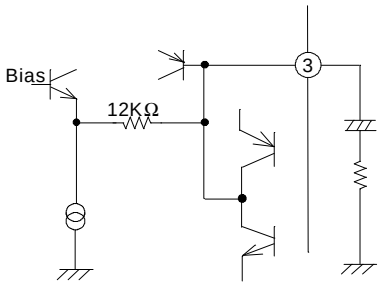


Pin 2 (REG.OUTPUT)

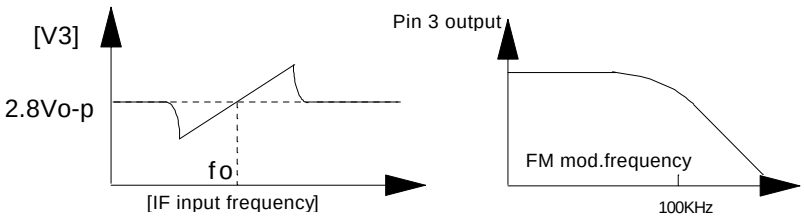


It is a regulated 3.5V output which has current drive capability of approximately 5mA

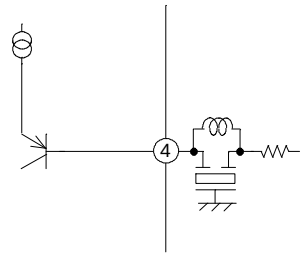
Pin 3 (APC FILTER)



In the locked state,the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200kHz.
In case the cut-off frequency is lower,the pull-in speed becomes slow.On the other hand,a higher cut-off frequency widen the pull-in range and band width,which results in a degradation in the S/N ratio.So, in the actual TV system design,the appropriate constant should be chosen for getting desirable performance considering above conditions.

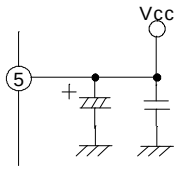


PIN 4 (EQ INPUT)



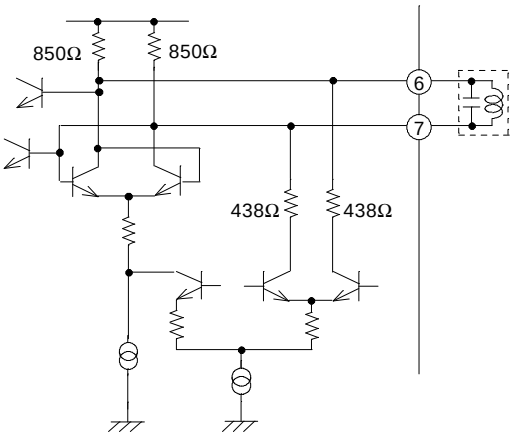
The input is Open Base.
If DC information is not input to Pin 9,IF AGC dose not work normally.
Please pay attention.

PIN 5 (Vcc)



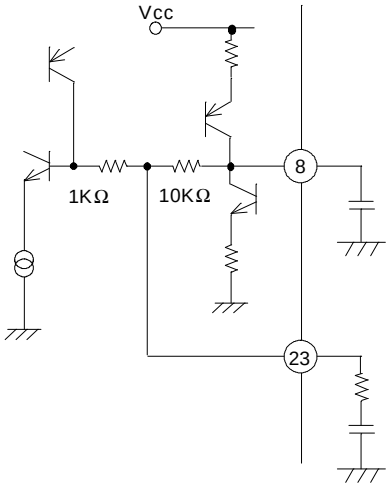
It is Vcc pin (only one Vcc pin in this IC)

PIN 6 and 7 (VCO COIL)

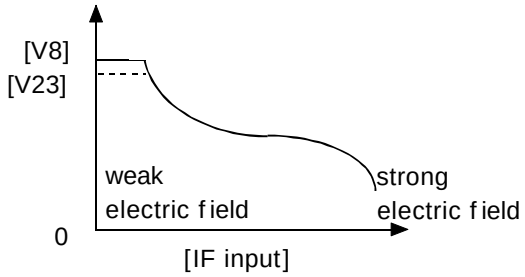


Connecting a tuning coil and capacitor to these pins enables an oscillation.
The oscillation frequency is tuned in f0.
In the actual adjustment, the coil is tuned so that the AFT voltage is reached to Vcc/2 with f0 as an input.
The printed pattern around these pins should be designed carefully to prevent an pull-in error of VCO, caused by the leakage interference from the large signal level oscillator to adjacent pins. The interconnection should be designed as short as possible.
In case the printed pattern has the interference problem, a capacitor of about 1pF is connected between pin 6 or 7 and GND so as to cancel the interference and keep enough pull-in range even in a low input level.

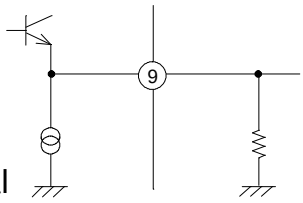
PIN 8 ,PIN 23 (IF AGC FILTER)



2-pin filter characteristics are available by utilizing the dynamic AGC circuit.
And AGC speed can be changed,if pin-23 on the external resistors is variable.



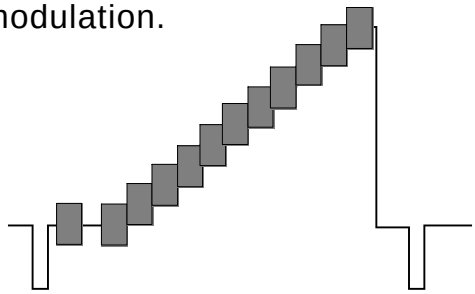
PIN 9 (VIDEO OUTPUT)



internal

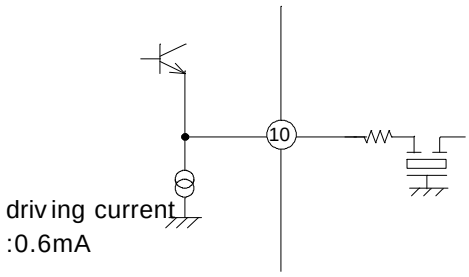
driving current:1.5 mA

An output amplitude is positive 0.6Vp-p in case of 87.5% video modulation.



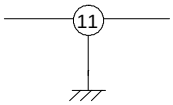
PIN 10 (QIF OUTPUT)

terminal voltage:2.25V



In the split system,the carrier signal to SIF provided from pin 10 through an emitter follower.
And, please open this pin ,when it is used INTER.

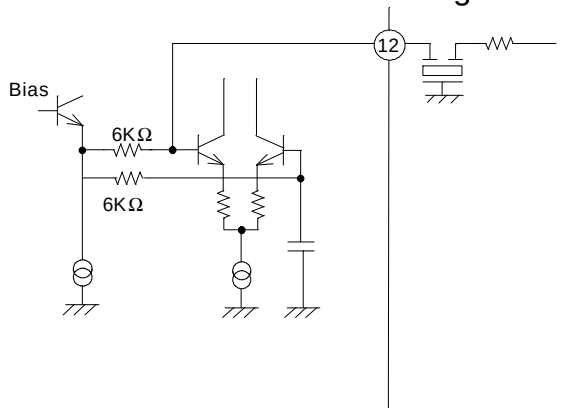
PIN 11 (GND)



This is GND of the SIF.

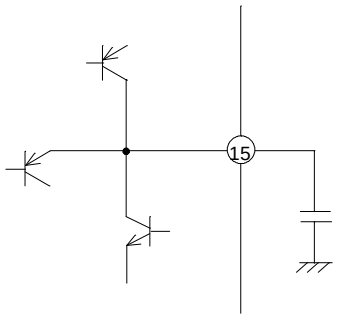
PIN 12 (LIMITER INPUT)

terminal voltage : 2.35V



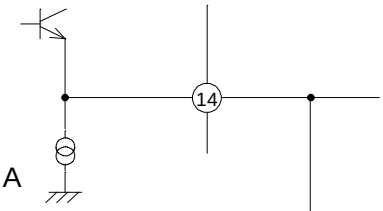
The input impedance is 6kΩ

PIN 13 (QIF AGC FILTER)



AGC speed can be changed by this pin's external capacity.

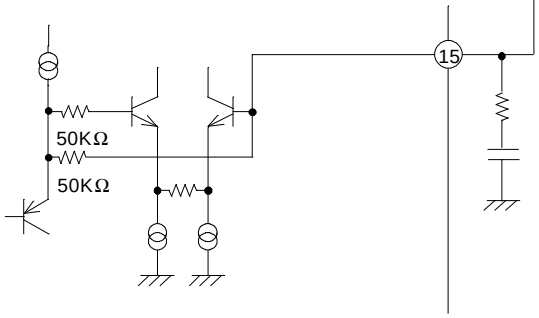
PIN 14 (AF OUTPUT)



internal
driving current:1mA

The FM detector can respond to several kinds of SIF signals without an adjustment and external components by adopting the PLL technique.
The capacitor between pin 14 and 15,which fixes the deemphasis characteristics,can be determined considering the combination of an equivalent resistance of the IC and this capacitor itself.

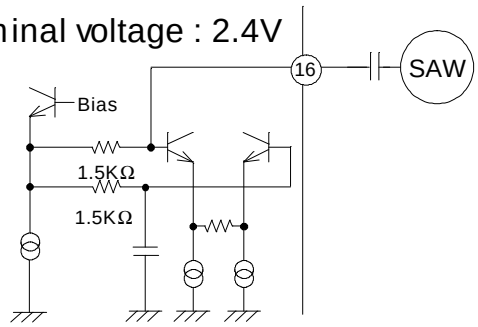
PIN 15 (AUDIO F/B)



Frequency characteristic of audio output is decided with 15-pin external capacitor value.
And audio output amplitude can make it small when it connected 15-pin external capacitor and resistance in series.

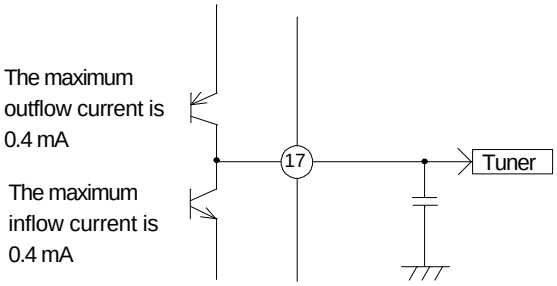
PIN 16 (QIF INPUT , INTER SW)

terminal voltage : 2.4V

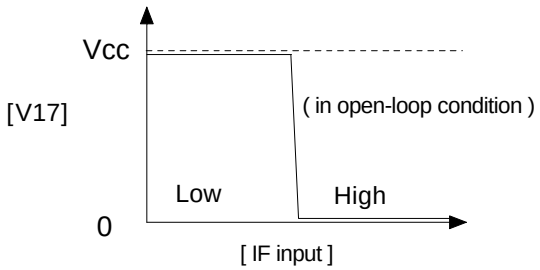


The input impedance is 1.5kΩ.

PIN 17 (RF AGC OUTPUT)



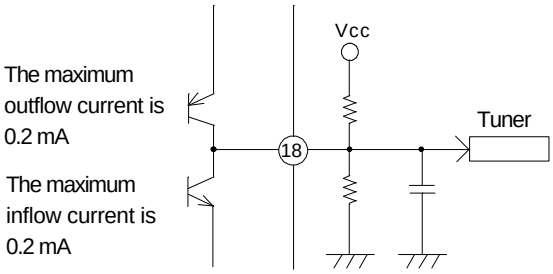
A current mode output is available in the reverse AGC operation.



Connecting a nonpolarity capacitor of 1µF between pin 17 and pin 22 improves AGC operating speed.

In that case , the capacitors between pin17/pin22 and ground should be removed.

PIN 18 (AFT OUTPUT)

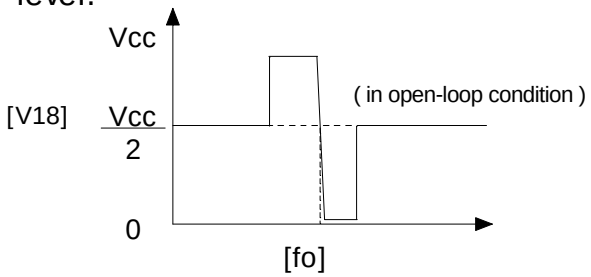


Since an AFT output is provided by a high impedance source,the detection sensitivity can be set by an external resistor.

The muting operation will be on in following two cases;

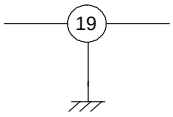
1) the APC is out of locking,

2) the video output becomes small enough in a low input level.



note) AFT maximum voltage is about 4.2 V.RF AGC maximum voltage is about 4.7 V.
Those do not increase it over.Please pay attention.

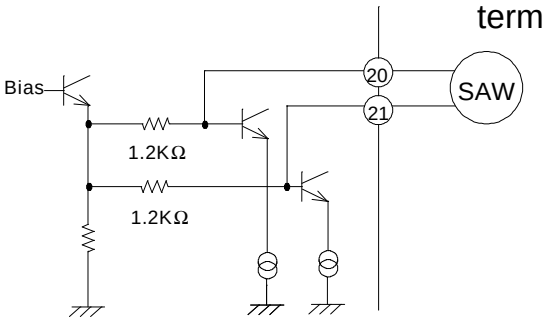
PIN 19 (GND)



This is GND other than SIF part.

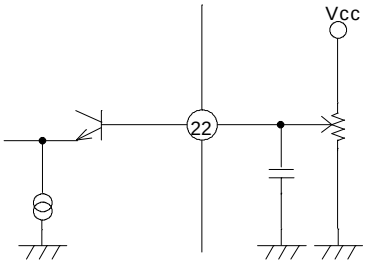
PIN 20,PIN 21 (VIF INPUT)

terminal voltage : 1.45V



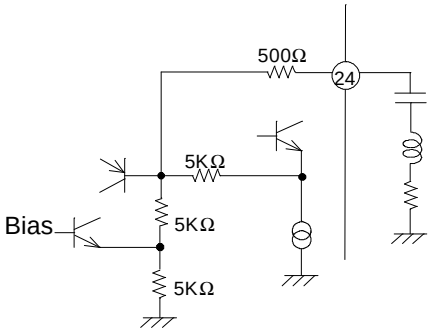
It should be designed considering careful impedance matching with the SAW filter.

PIN 22 (RF AGC DELAY)

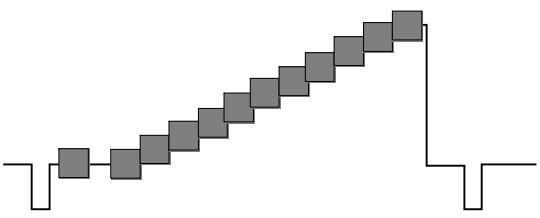


An applied voltage to the pin 22 is for changing a RF AGC delay point.

PIN 24 (EQ F/B)

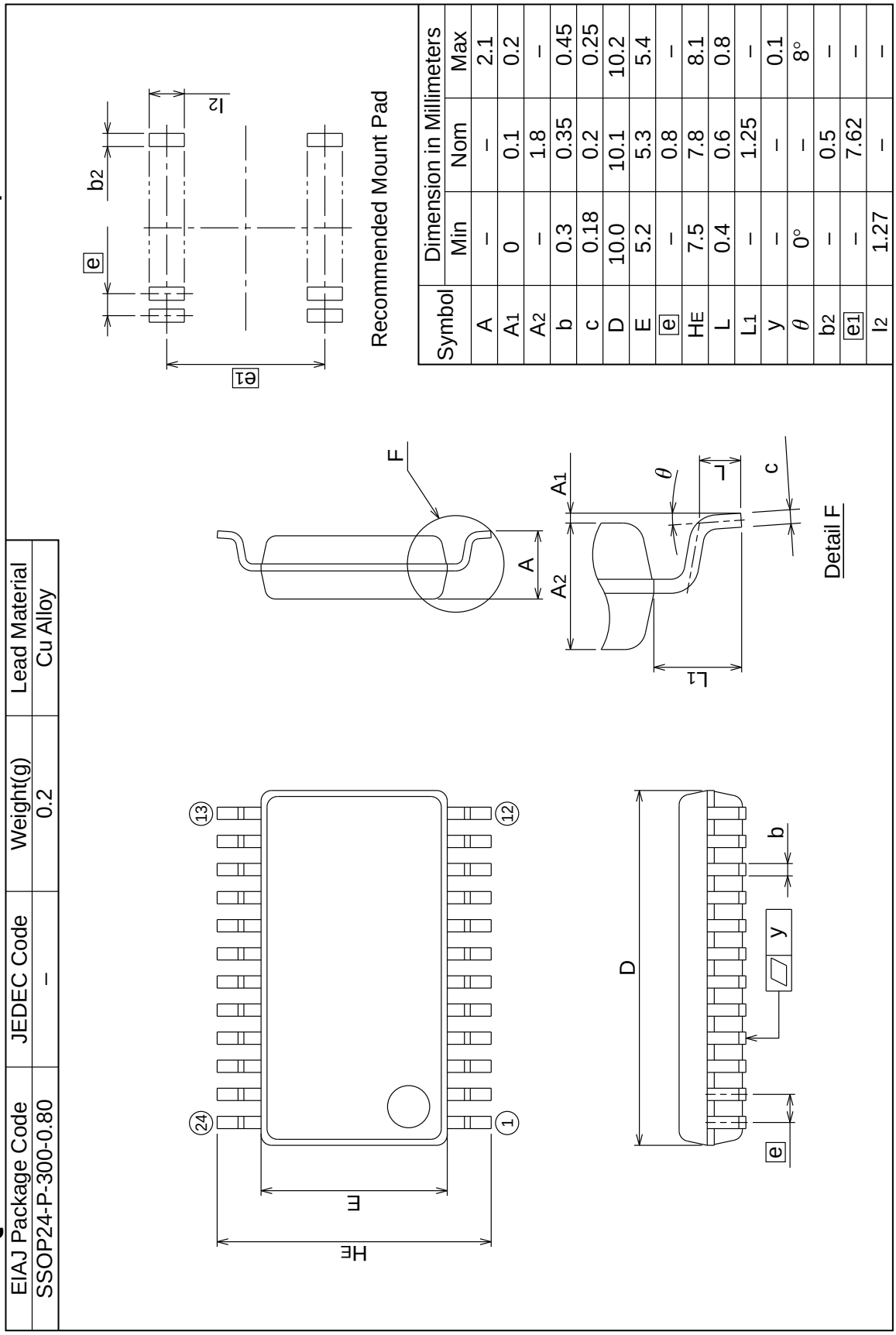


Both the external coil and capacitor determine the frequency response of EQ output.
The series connected resistor is for damping.



DETAILED DIAGRAM OF PACKAGE OUTLINE

Plastic 24pin 300mil SSOP



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A1	0	0.1	0.2
A2	–	1.8	–
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	0.8	–
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	–	1.25	–
y	–	–	0.1
θ	0°	–	8°
b2	–	0.5	–
e1	–	7.62	–
l2	1.27	–	–

24P2Q-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-300-0.80	–	0.2	Cu Alloy

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