SGS-THOMSON MICROELECTRONICS

# M54HC165
# M74HC165

## 8-BIT PISO SHIFT REGISTER

- HIGH SPEED
  $t_{PD}$ = 21 ns (TYP.) at $V_{CC}$ = 5V
- LOW POWER DISSIPATION
  $I_{CC}$ = 4 $\mu$A (MAX.) at $T_A$ = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH}$ = $V_{NIL}$ = 28% $V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = $I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH}$ = $t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  $V_{CC}$ (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS165

**B1N**
Plastic Package

**F1**
Ceramic Frit Seal Package

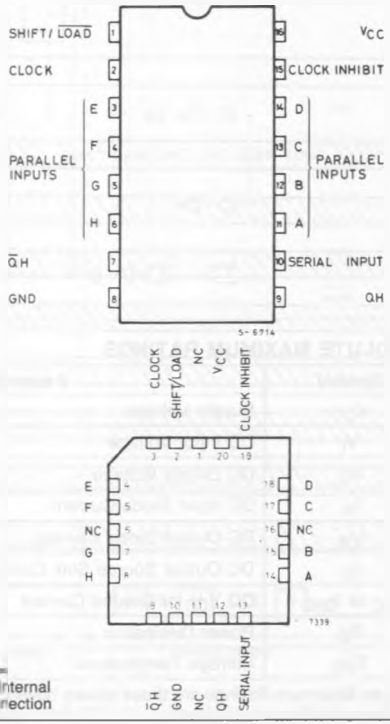
**M1**
Micro Package

**C1**
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC165 F1
M74HC165 B1N
M74HC165 F1
M74HC165 C1
M74HC165 M1

**PIN CONNECTIONS** (top view)




### DESCRIPTION

The M54/74HC165 is a high speed CMOS 8-BIT PISO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains eight clocked master-slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data enters when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock inputs perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

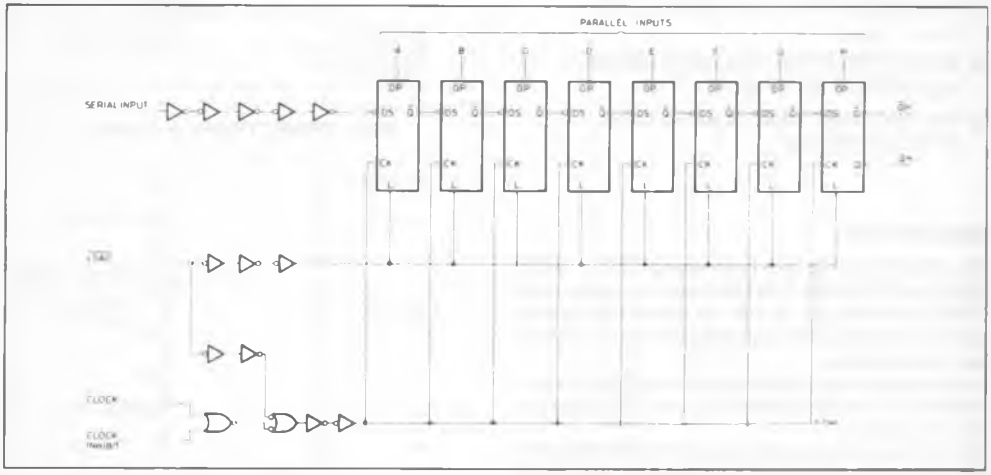
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

## TRUTH TABLE

| INPUTS | | | | | INTERNAL OUTPUTS | | OUTPUT |
|---|---|---|---|---|---|---|---|
| SHIFT/ LOAD | CLOCK INHIBIT | CLOCK | SERIAL IN | PARALLEL A.....H | QA | QB | QH |
| L | X | X | X | a.....h | a | b | h |
| H | L | ↑ | H | X | H | QAn | QGn |
| H | L | ↑ | L | X | L | QAn | QGn |
| H | ↓ | L | H | X | H | QAn | QGn |
| H | ↓ | L | L | X | L | QAn | QGn |
| H | X | H | X | X | NO CHANGE | | |
| H | H | X | X | X | NO CHANGE | | |

a.....h: THE LEVEL OF STEADY INPUT VOLTAGE AT INPUTS A THROUGH H RESPECTIVELY
QAn...QGn: THE LEVEL OF QA – QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

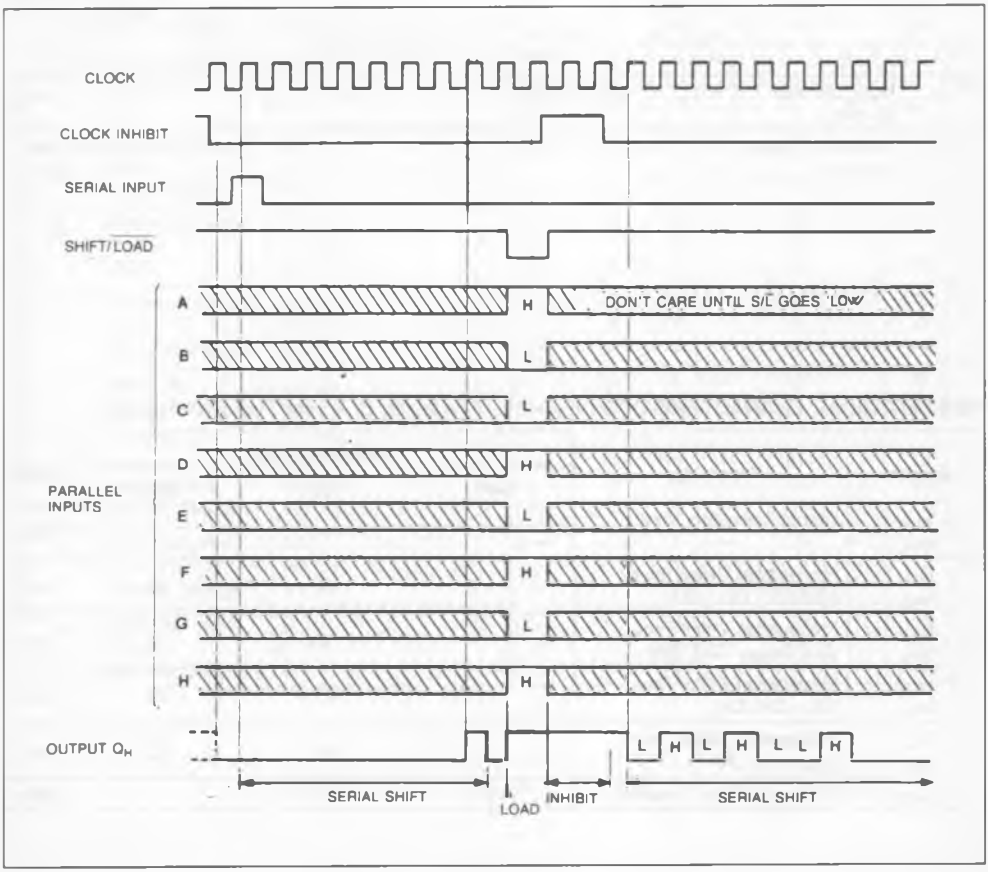
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | – 0.5 to 7 | V |
| $V_I$ | DC Input Voltage | – 0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Source Sink Current Per Output Pin | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | – 65 to 150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. (*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 to 6 | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_A$ | Operating Temperature 74HC Series<br>54HC Series | −40 to 85<br>−55 to 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2 V: 0 to 1000<br>$V_{CC}$ = 4.5V: 0 to 500<br>$V_{CC}$ = 6 V: 0 to 400 | ns |

## TIMING CHART



## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ | Test Condition | | $T_A = 25°C$ 54HC and 74HC | | | − 40 to 85°C 74HC | | − 55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | | 1.5 | — | — | 1.5 | — | 1.5 | — | V |
| | | 4.5 | | | 3.15 | — | — | 3.15 | — | 3.15 | — | |
| | | 6.0 | | | 4.2 | — | — | 4.2 | — | 4.2 | — | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | — | — | 0.5 | — | 0.5 | — | 0.5 | V |
| | | 4.5 | | | — | — | 1.35 | — | 1.35 | — | 1.35 | |
| | | 6.0 | | | — | — | 1.8 | — | 1.8 | — | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $V_I$ | $I_O$ | 1.9 | 2.0 | — | 1.9 | — | 1.9 | — | V |
| | | 4.5 | $V_{IH}$ or $V_{IL}$ | − 20 μA | 4.4 | 4.5 | — | 4.4 | — | 4.4 | — | |
| | | 6.0 | | | 5.9 | 6.0 | — | 5.9 | — | 5.9 | — | |
| | | 4.5 | | − 4.0 mA | 4.18 | 4.31 | — | 4.13 | — | 4.10 | — | |
| | | 6.0 | | − 5.2 mA | 5.68 | 5.8 | — | 5.63 | — | 5.60 | — | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $V_{IH}$ or $V_{IL}$ | 20 μA | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 4.5 | | | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 6.0 | | | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 4.5 | | 4.0 mA | — | 0.17 | 0.26 | — | 0.33 | — | 0.40 | |
| | | 6.0 | | 5.2 mA | — | 0.18 | 0.26 | — | 0.33 | — | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I = V_{CC}$ or GND | | — | — | ±0.1 | — | ±1.0 | — | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I = V_{CC}$ or GND | | — | — | 4 | — | 40 | — | 80 | μA |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

| Symbol | Parameter | 54HC and 74HC | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | | 4 | 8 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLOCK - QH - $\overline{QH}$) | | 21 | 33 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($CLOCK_{INH}$ - QH, $\overline{QH}$) | | 21 | 33 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{S/L}$ - QH, $\overline{QH}$) | | 22 | 35 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($H_{IN}$ - QH, $\overline{QH}$) | | 20 | 32 | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 28 | 48 | | MHz |

**AC ELECTRICAL CHARACTERISTICS** ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | — | 30 | 75 | — | 95 | | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | 19 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CK-QH, $\overline{QH}$) | 2.0 | | — | 96 | 190 | — | 240 | | 285 | ns |
| | | 4.5 | | — | 24 | 38 | — | 48 | | 57 | |
| | | 6.0 | | — | 20 | 32 | — | 41 | | 48 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($CK_{INH}$ QH, $\overline{QH}$) | 2.0 | | — | 96 | 190 | — | 240 | | 285 | ns |
| | | 4.5 | | — | 24 | 38 | — | 48 | | 57 | |
| | | 6.0 | | — | 20 | 32 | — | 41 | | 48 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($S/\overline{L}$ - QH - $\overline{QH}$) | 2.0 | | — | 104 | 200 | — | 250 | — | 300 | ns |
| | | 4.5 | | — | 26 | 40 | — | 50 | — | 60 | |
| | | 6.0 | | — | 22 | 34 | — | 43 | — | 51 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (H - QH, $\overline{QH}$) | 2.0 | | — | 92 | 180 | — | 225 | — | 270 | ns |
| | | 4.5 | | — | 23 | 36 | — | 45 | — | 54 | |
| | | 6.0 | | — | 20 | 31 | — | 38 | — | 46 | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | | 5 | 11 | — | 4 | — | 3.4 | — | MHz |
| | | 4.5 | | 25 | 44 | — | 20 | — | 17 | — | |
| | | 6.0 | | 29 | 52 | — | 24 | — | 20 | — | |
| $t_{W(H)}$ $t_{W(L)}$ | Minimum Pulse Width (CK, $CK_{INH}$) | 2.0 | | — | 30 | 75 | — | 95 | | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | 19 | |
| $t_{W(L)}$ | Minimum Pulse Width ($S/\overline{L}$) | 2.0 | | — | 30 | 75 | — | 95 | | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | 19 | |
| $t_s$ | Minimum Set-up Time ($S/\overline{L}$-CK, $CK_{INH}$) | 2.0 | | — | 30 | 75 | — | 95 | — | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | — | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | — | 19 | |
| $t_s$ | Minimum Set-up Time (PI-$S/\overline{L}$) | 2.0 | | — | 15 | 50 | — | 65 | | 75 | ns |
| | | 4.5 | | — | 3 | 10 | — | 13 | | 15 | |
| | | 6.0 | | — | 3 | 9 | — | 11 | | 13 | |
| $t_s$ | Minimum Set-up Time (SI-CK, $CK_{INH}$) | 2.0 | | — | 10 | 50 | — | 65 | | 75 | ns |
| | | 4.5 | | — | 2 | 10 | — | 13 | | 15 | |
| | | 6.0 | | — | 2 | 9 | — | 11 | | 13 | |
| $t_h$ | Minimum Hold Time (PI-$S/\overline{L}$) (SI-CK, $CK_{INH}$) | 2.0 | | — | — | 5 | — | 5 | — | 5 | ns |
| | | 4.5 | | — | — | 5 | — | 5 | — | 5 | |
| | | 6.0 | | — | — | 5 | — | 5 | — | 5 | |
| $t_h$ | Minimum Hold Time (SI$\overline{L}$-CK, $CK_{INH}$) | 2.0 | | — | 30 | 75 | — | 95 | | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | 19 | |

## AC ELECTRICAL CHARACTERISTICS (Continued)

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{REM}$ | Minimum Removal Time ($CK_{INH}$-CK) (CK-$CK_{INH}$) | 2.0<br>4.5<br>6.0 | | —<br>—<br>— | 30<br>8<br>7 | 75<br>15<br>13 | —<br>—<br>— | 95<br>19<br>16 | —<br>—<br>— | 110<br>22<br>16 | ns |
| $C_{IN}$ | Input Capacitance | | | — | 5 | 10 | — | 10 | | 10 | pF |
| $C_{PD}$ (*) | Power Dissipation Capacitance | | | — | 95 | — | — | — | | | pF |

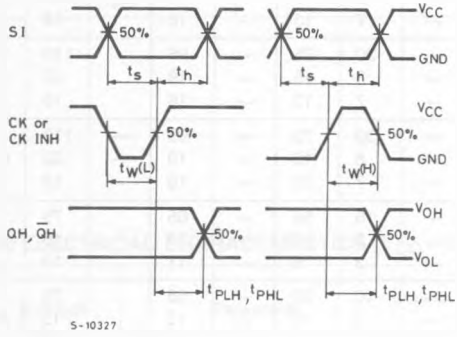
Note (*) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

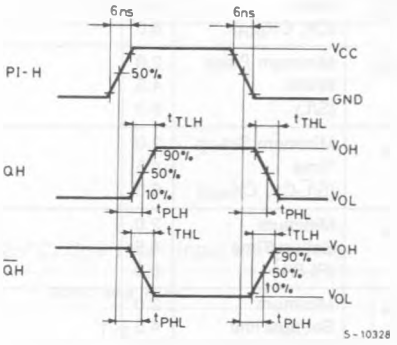
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

## SWITCHING CHARACTERISTICS TEST WAVEFORM

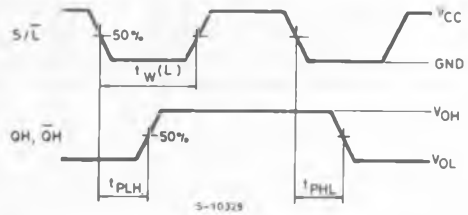
SERIAL MODE



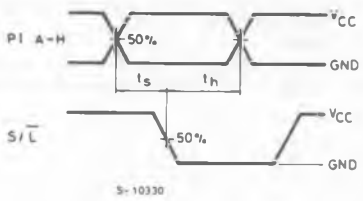

PARALLEL MODE




PARALLEL MODE

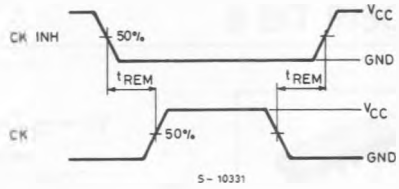



PARALLEL MODE

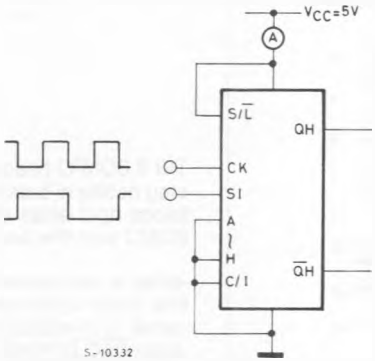


## SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

SERIAL MODE




## TEST CIRCUIT $I_{CC}$ (Opr.)




INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.