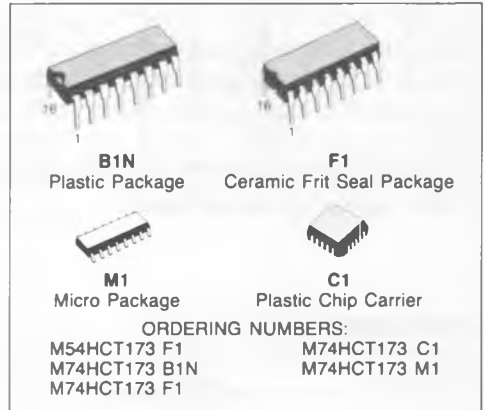


## QUAD D-TYPE REGISTER (3-STATE)

- **HIGH SPEED**  
 $f_{MAX} = 52 \text{ MHz (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (Min.)}$
- **OUTPUT DRIVE CAPABILITY**  
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH 54/74LS173



### DESCRIPTION

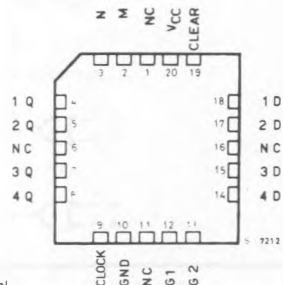
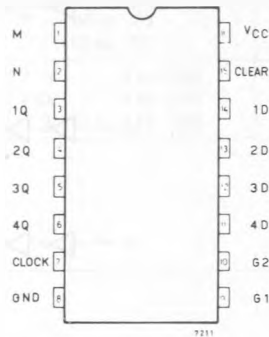
The M54/74HC173 is a high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated in silicon gate C<sup>2</sup>MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is composed of a four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D<sub>1</sub>-D<sub>4</sub>) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G<sub>1</sub> and G<sub>2</sub>) are held low.

The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTIONS (top view)



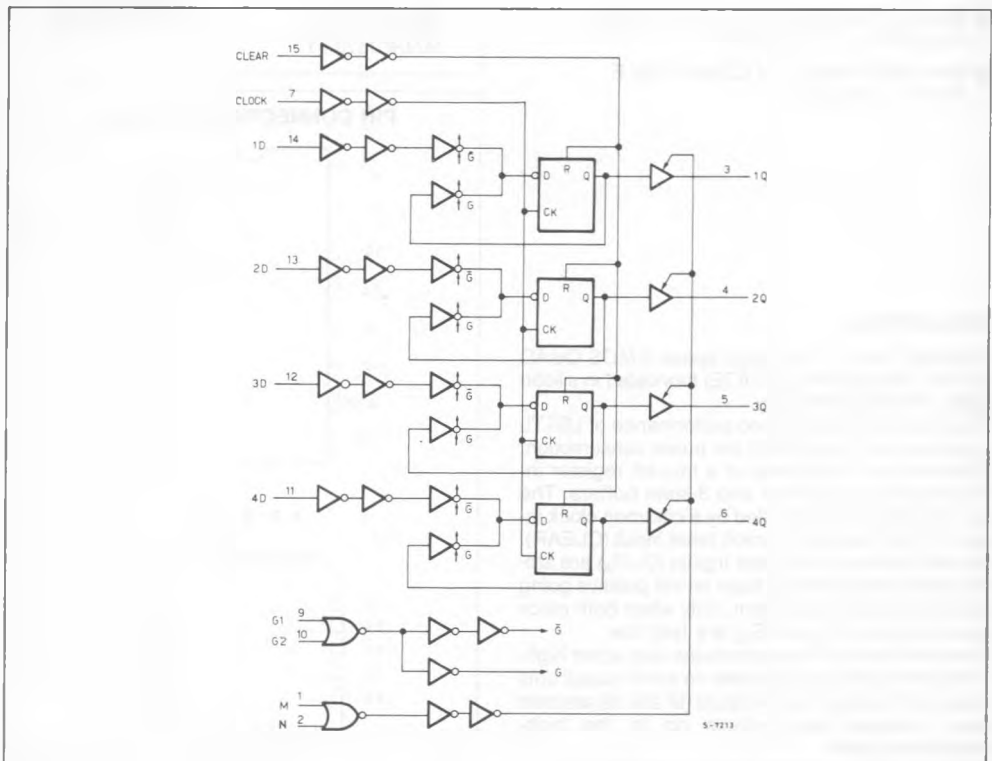
NC =  
No Internal  
Connection

## TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE		D <sub>n</sub>	OUTPUT CONTROL		Q <sub>n</sub>
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	$\overline{1}$	X	X	X	L	L	Q0
L	$\overline{0}$	H	X	X	L	L	Q0
L	$\overline{1}$	X	H	X	L	L	Q0
L	$\overline{0}$	L	L	H	L	L	H
L	$\overline{1}$	L	L	L	L	L	L

X: DON'T CARE Z: HIGH IMPEDANCE

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.5 to 7	V
$V_I$	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin	$\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	- 65 to 150	$^{\circ}C$

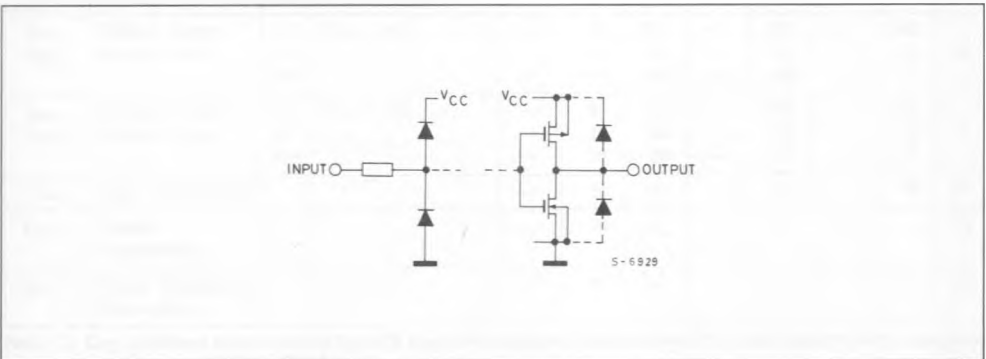
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW:  $\equiv 65^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$ :  $65^{\circ}C$  to  $85^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_A$	Operating Temperature	74HC Series 54HC Series	- 40 to 85 - 55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	$V_{CC}$ { 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V <sub>IH</sub>	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V	
V <sub>IL</sub>	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V <sub>I</sub>	I <sub>O</sub>	1.9	2.0	—	1.9	—	1.9	—	V
			V <sub>IH</sub> or V <sub>IL</sub>	-20 μA	4.4 5.9	4.5 6.0	— —	4.4 5.9	— —	4.4 5.9	— —	
				-6.0 mA -7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
				20 μA	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	
V <sub>OL</sub>	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.37 0.37	— —	0.40 0.40	V
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	±0.1	—	±1	—	±1	μA	
I <sub>OZ</sub>	3-State Output Off-State Current	6.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	—	—	±0.5	—	±5.0	—	±10	μA	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	4	—	40	—	80	μA	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

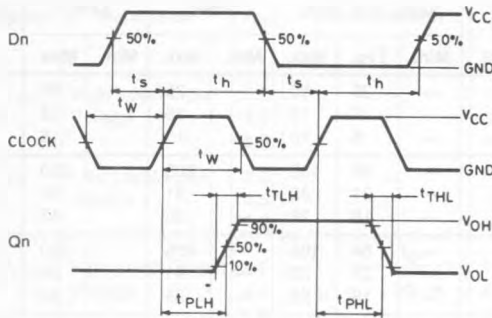
Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - Q)	2.0 4.5 6.0		— — —	84 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLEAR-Q)	2.0 4.5 6.0		— — —	84 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
$f_{MAX}$	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	12 50 59	— — —	4.8 24 28	— — —	4.0 20 24	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{REM}$	Minimum Removal Time (CLEAR)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
$t_S$	Minimum Set-up Time ( $G_1, G_2$ )	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
$t_S$	Minimum Set-up Time (D)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_h$ $t_h$	Minimum Hold Time ( $G_1, G_2, D$ )	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
$t_{PZL}$ $t_{PZH}$	3-State Output Enable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	65 13 11	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
$t_{PLZ}$ $t_{PHZ}$	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	84 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
$C_{IN}$	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{OUT}$	Output Capacitance			—	10	—	—	—	—	—	ns
$C_{PD} (*)$	Power Dissipation Capacitance			—	35	—	—	—	—	—	pF

Note (\*)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

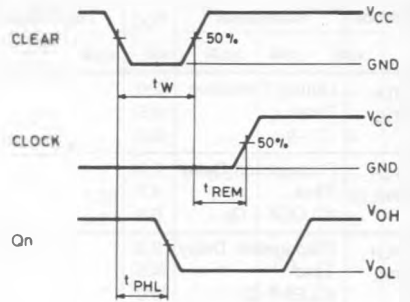
$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



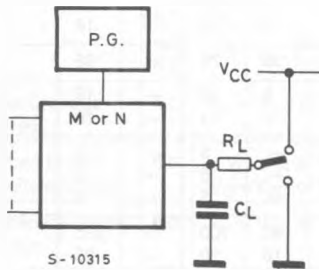
S-10668

CLEAR = "H"

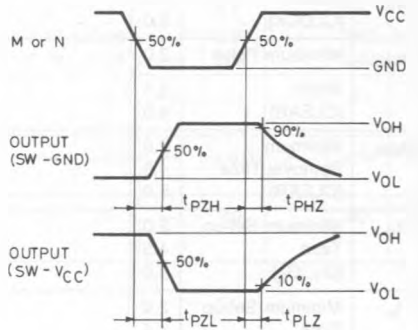


S-10669

DN = "H"



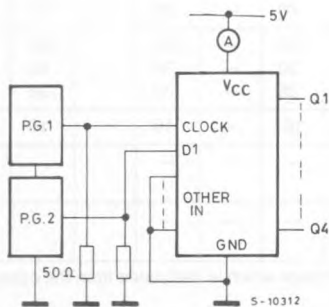
S-10315



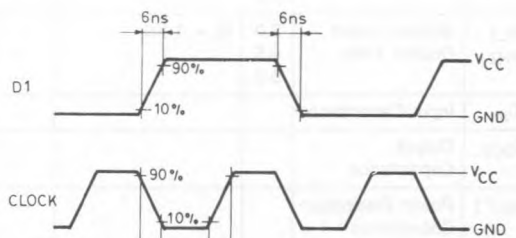
S-10314

EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO  $V_{CC}$  LINE.

TEST CIRCUIT  $I_{CC}$  (Opr.)



S-10312



S-10313