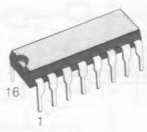
SGS-THOMSON MICROELECTRONICS

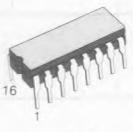
M54HC195
M74HC195

4 BIT PIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC}(MIN)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS195



B1N
Plastic Package



F1
Ceramic Frit Seal Package

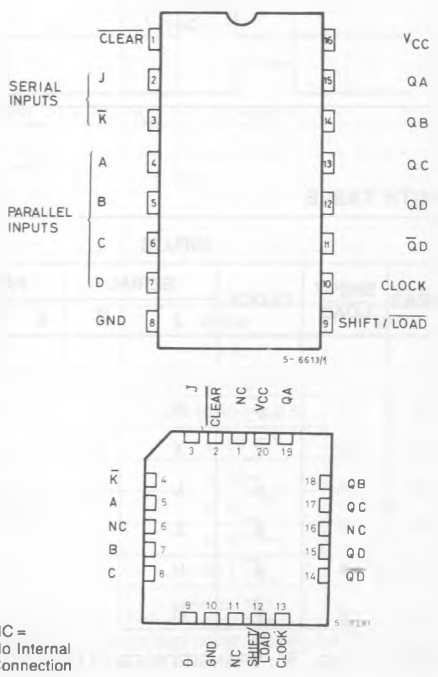
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC195 F1
M74HC195 B1N
M74HC195 F1
M74HC195 C1
M74HC195 M1

PIN CONNECTIONS (top view)



DESCRIPTION

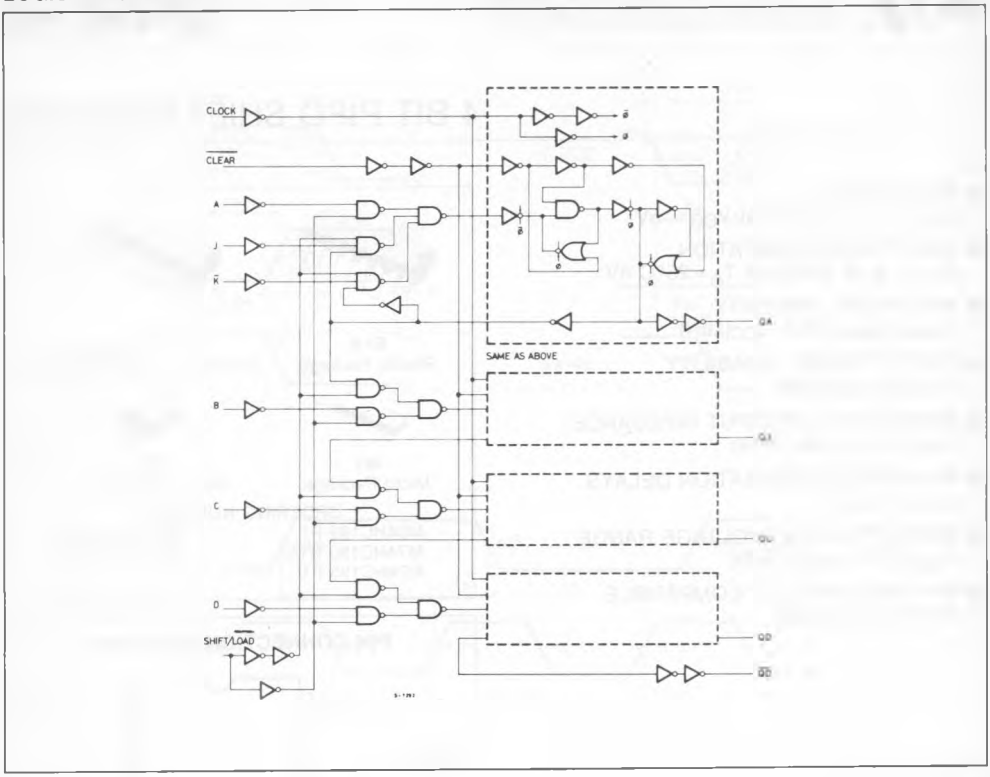
The M54/74HC195 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, a SHIFT/$\overline{\text{LOAD}}$ control input, and a direct overriding $\overline{\text{CLEAR}}$. This shift register can operate in two modes: Parallel Load; Shift from QA towards QD.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/$\overline{\text{LOAD}}$ control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/$\overline{\text{LOAD}}$ control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

All inputs are equipped with protection circuits against static discharge transient excess voltage.

LOGIC DIAGRAM

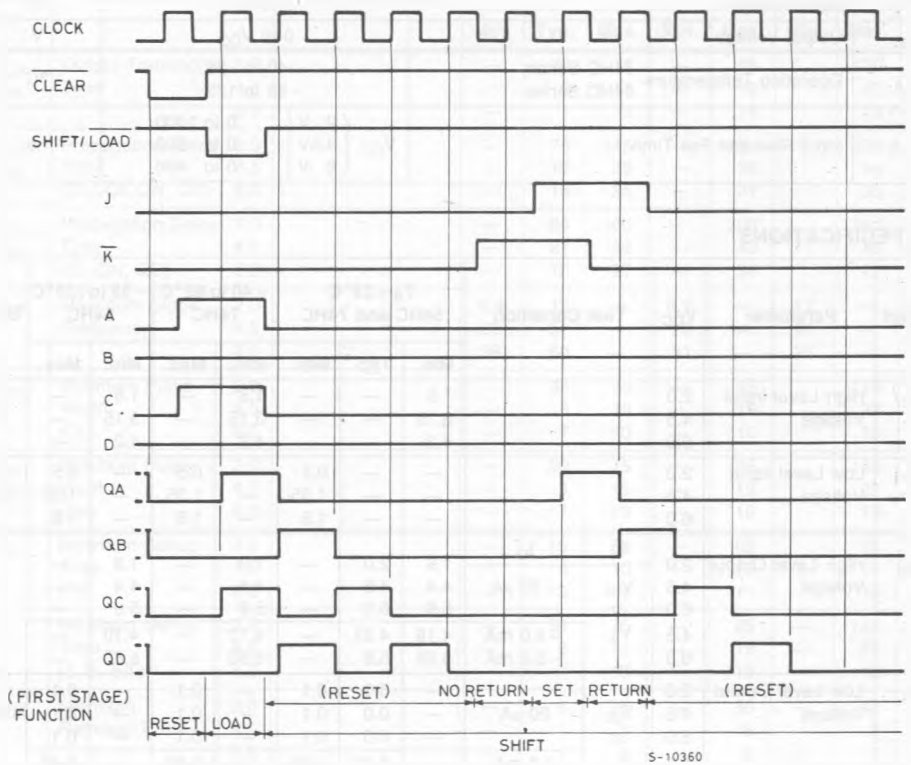


TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{QD}$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{QD0}$
H	H	↑	L	H	X	X	X	X	QA0	QA0	QBn	QCn	$\overline{QCn}$
H	H	↑	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{QCn}$
H	H	↑	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{QCn}$
H	H	↑	H	L	X	X	X	X	$\overline{QAn}$	QAn	QBn	QCn	$\overline{QCn}$

X: DON'T CARE; ↓: TRANSITION FROM LOW TO HIGH LEVEL; ↑: TRANSITION FROM HIGH TO LOW LEVEL

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature: 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5 V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN, QD)		14	23	ns
t_{PHL}	Propagation Delay Time (CL-QN, $\overline{QD}$)		17	27	ns
f_{MAX}	Maximum Clock Frequency	35	56		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

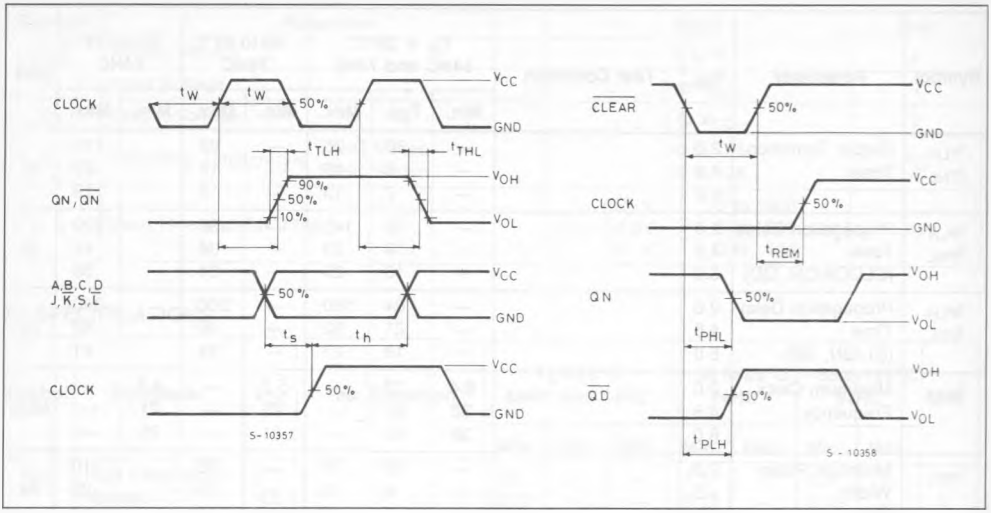
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN, $\overline{QD}$)	2.0 4.5 6.0		— — —	76 19 16	145 29 25	— — —	180 36 31		220 44 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CL-QN, QD)	2.0 4.5 6.0		— — —	84 21 18	160 32 27	— — —	200 40 34		240 48 41	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6.4 32 38	13 51 60	— — —	5.2 26 31	— — —	4.2 21 25	— — —	MHz
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (PI)	2.0 4.5 6.0		— — —	15 4 3	50 10 9	— — —	65 13 11		75 15 13	ns
t_s	Minimum Set-up Time (J, $\overline{K}$, S/$\overline{L}$)	2.0 4.5 6.0		— — —	36 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 1 1	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
t_h	Minimum Hold Time (PIN, SIN-CK)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_h	Minimum Hold Time (S/L-CK)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	126	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

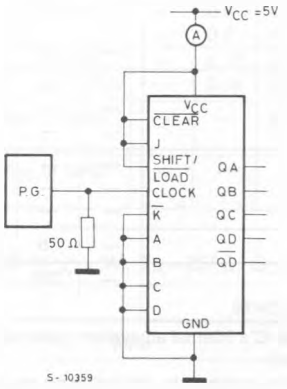
Average operating current can be obtained by the following equation

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.