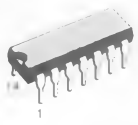
SGS-THOMSON MICROELECTRONICS

M54HC242/243
M74HC242/243

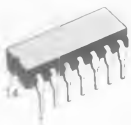
QUAD BUS TRANSCEIVER (3-STATE)

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN).
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS242/243



B1N
Plastic Package



F1
Ceramic Frit Seal Package

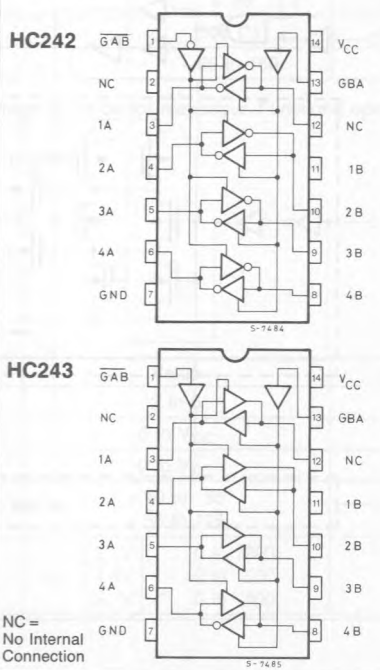
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)



DESCRIPTION

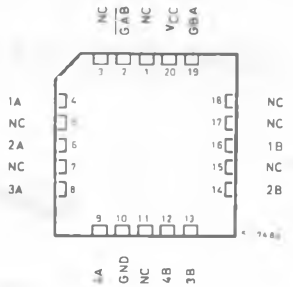
The M54/74HC242 and the M54/74HC243 are high speed CMOS QUAD BUS TRANSCEIVER (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/74HC242,243 are 3-STATE bi-directional inverting and non-inverting buffers and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances.

Each device has one active high enable (GBA), and one active low enable ($\overline{GAB}$). GBA enables the A outputs and $\overline{GAB}$ enables the B outputs.

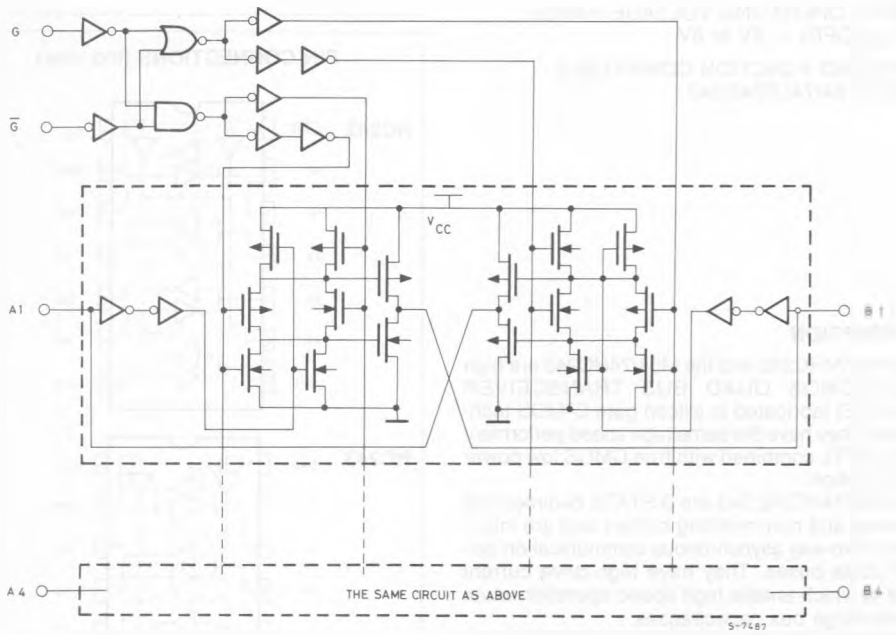
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GAB	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	$A = \overline{B}$	A = B
L	L	INPUT	OUTPUT	$B = \overline{A}$	B = A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

Z = HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

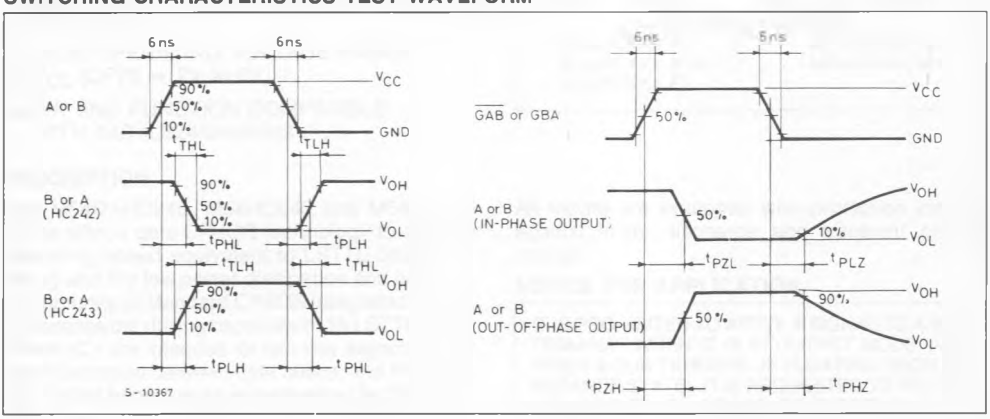
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Output	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (HC242)	2.0		—	48	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_{PLH} t_{PHL}	Propagation Delay Time (HC243)	2.0		—	44	90	—	115		135	ns
		4.5		—	11	18	—	23	—	27	
		6.0		—	9	15	—	20	—	23	
t_{PZH} t_{PZL}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

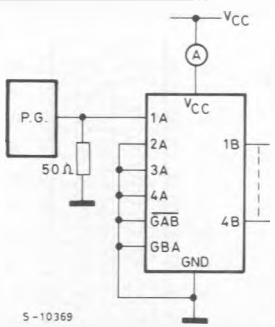
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PHZ} t_{PLZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance		$\overline{GAB}$, GBA	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Terminal Input Capacitance		An, Bn	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC242	—	42	—	—	—	—	—	pF
			M54/74HC243	—	36	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current