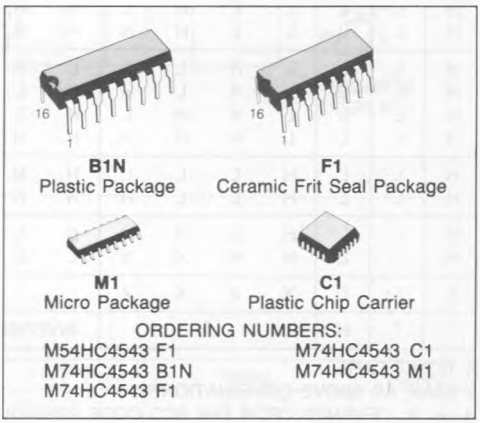
SGS-THOMSON MICROELECTRONICS

M54HC4543
M74HC4543

BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

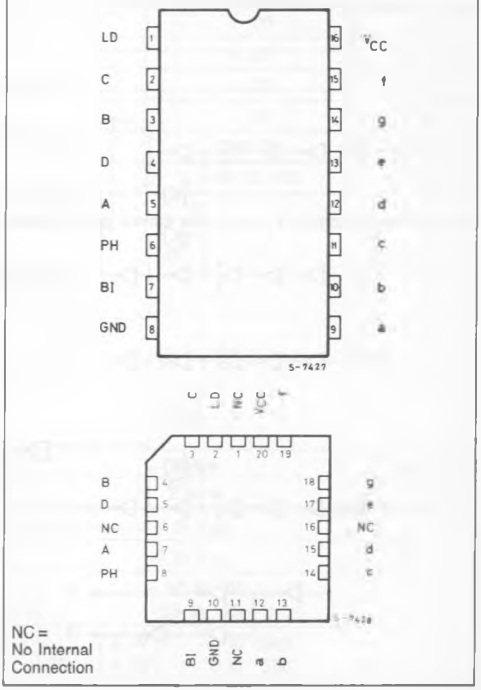
- HIGH SPEED
  t_{PD} = 44 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4543B



ORDERING NUMBERS:

M54HC4543 F1
M74HC4543 B1N
M74HC4543 F1
M74HC4543 C1
M74HC4543 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

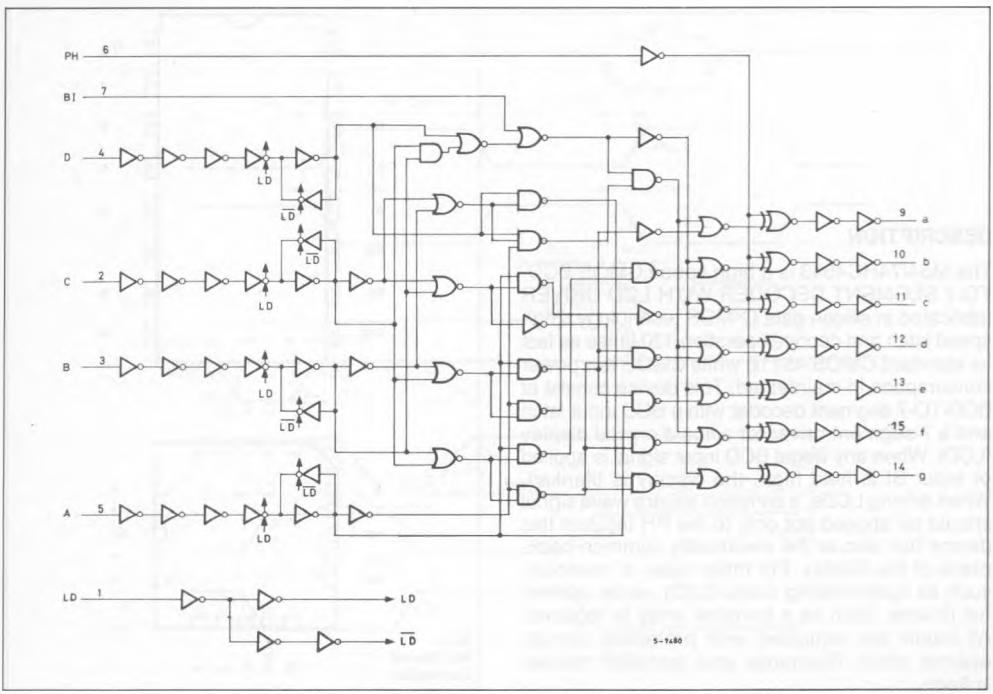
The M54/74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated in silicon gate C^2MOS technology. High speed latch and decode operation 120 times as fast as standard CMOS 4511B while CMOS low power consumption in maintained. This device consist of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for a liquid crystal display (LCD). When any illegal BCD input signal is applied or input BI is held high, the display is blanked. When driving LCDs, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common back-plane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as a transitor array is required. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

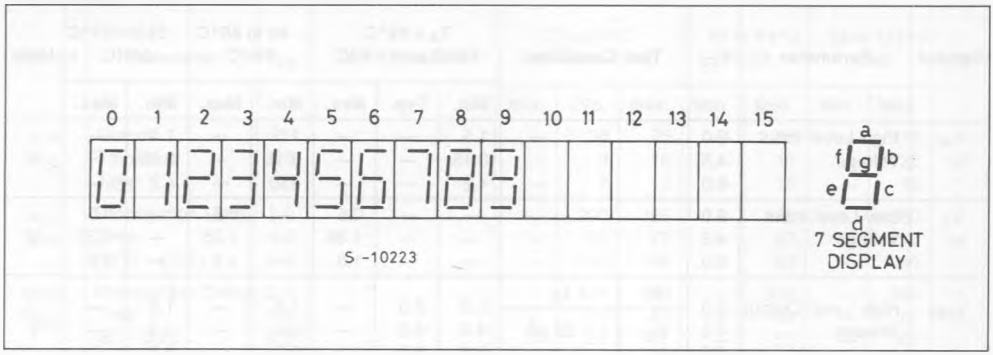
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X			#	#	#			# # #
↑	↑	H			↑		INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X: DON'T CARE
↑: SAME AS ABOVE COMBINATIONS
#: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD = 'H'

LOGIC DIAGRAM



DISPLAY MODE



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		V_{CC} 4.5V	0 to 500	
		V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - OUT)		44	68	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BI - OUT)		27	42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (PH - OUT)		19	30	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - OUT)	2.0		—	200	385	—	485	—	580	ns
		4.5		—	50	77	—	97	—	116	
		6.0		—	43	66	—	83	—	98	
t_{PLH} t_{PHL}	Propagation Delay Time (BI - OUT)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	36	41	—	51	—	61	
t_{PHL}	Propagation Delay Time (PH - OUT)	2.0		—	80	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
$t_{W(H)}$	Minimum Pulse Width (LD)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	30	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST WAVEFORM