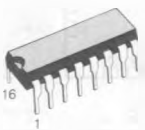
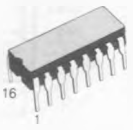
M54/74HC7292
M54/74HC7294

PROGRAMMABLE DIVIDER/TIMER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS292/294



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXXX F1
M74HCXXXX B1N
M74HCXXXX F1
M74HCXXXX C1
M74HCXXXX M1

DESCRIPTION

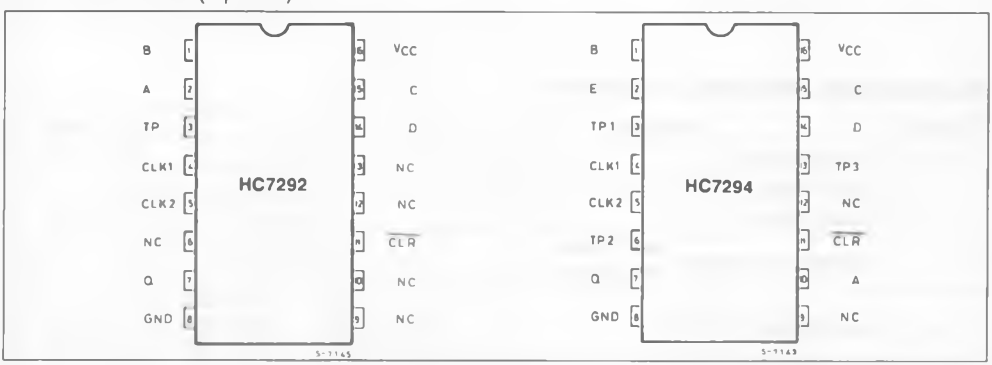
The 54/74HC7292 and 54/74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table). The HC7292 can divide from 2^2 to 2^{31}, and the HC7294 can divide from 2^2 to 2^{15}. Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the HC7292 and TP on the HC7294). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Note: HC7292 and HC7294 all have outputs "Totem pole"

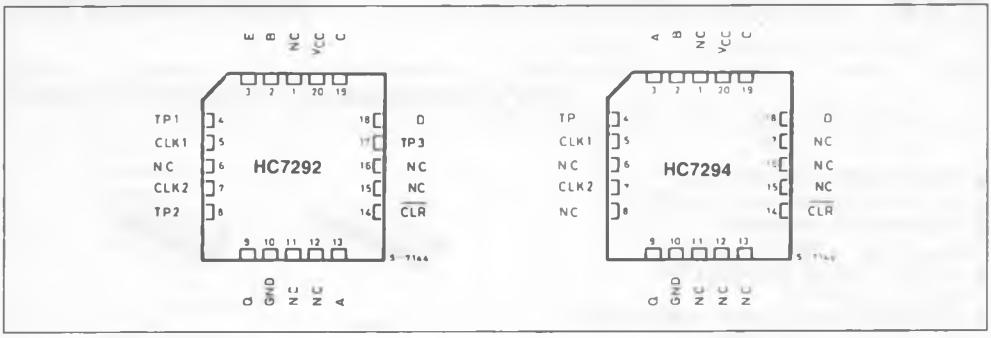
TRUTH TABLE

$\overline{CLEAR}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	CLEARED TO L
H		L	UP COUNT
H	L		
H	H	X	NO CHANGE
H	X	H	

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

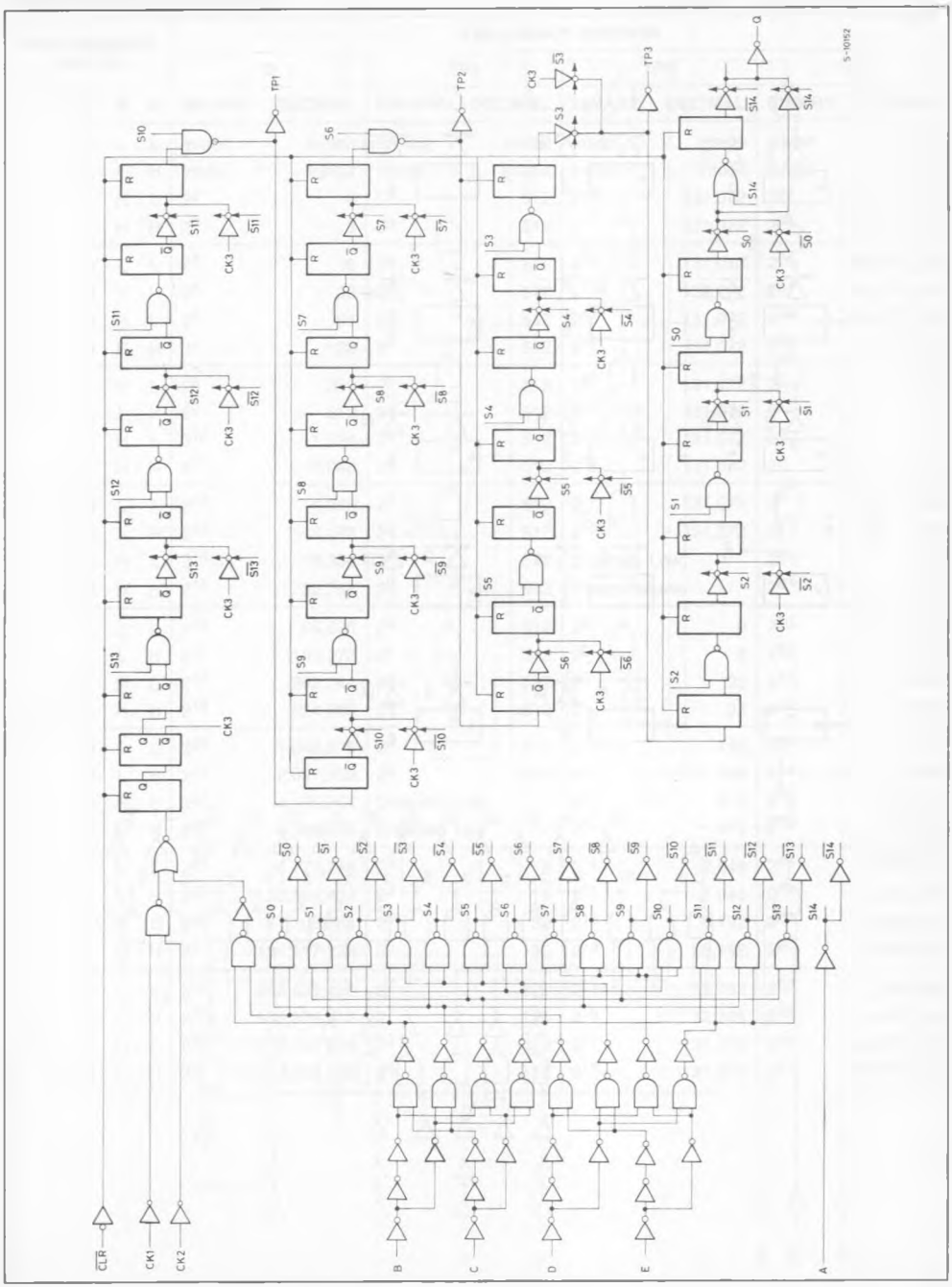
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

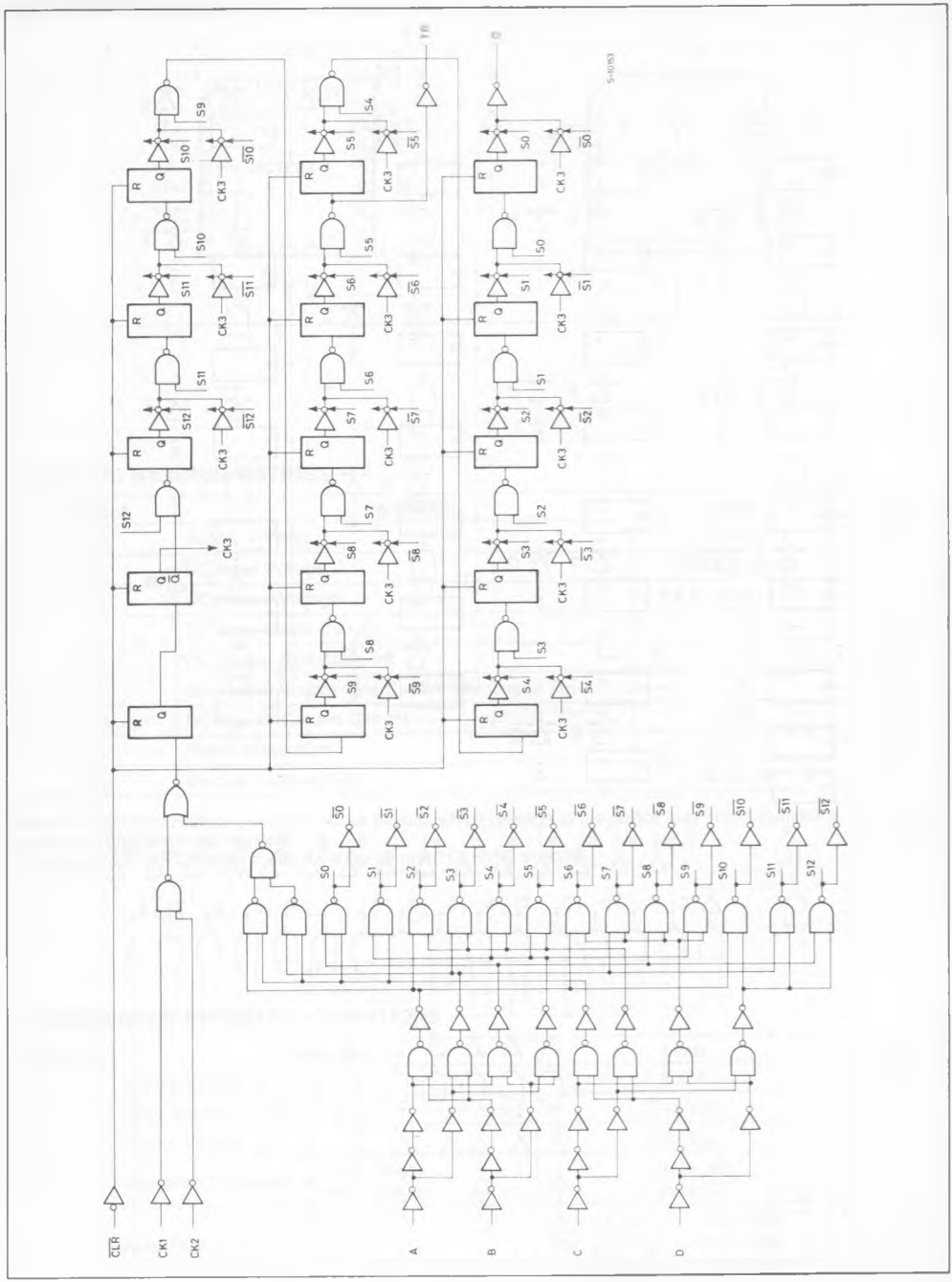
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

LOGIC DIAGRAM (HC7292)



LOGIC DIAGRAM (HC7294)



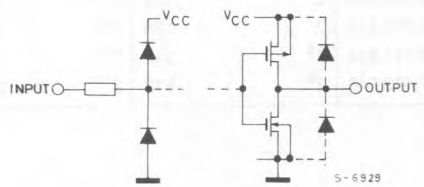
FUNCTION TABLE (HC7292)

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^2	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

FUNCTION TABLE (HC7294)

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter		54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT			4	8	ns
t_{TLH} t_{THL}	Output Transition Time TP OUTPUTS			29	45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	HC7292		58	89	ns
		HC7294		53	81	
t_{PHL}	Propagation Delay Time (CLEAR-Q)	HC7292		49	75	ns
		HC7294		45	69	
f_{MAX}	Maximum Clock Frequency	HC7292	28	56		MHz
		HC7294	35	61		

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

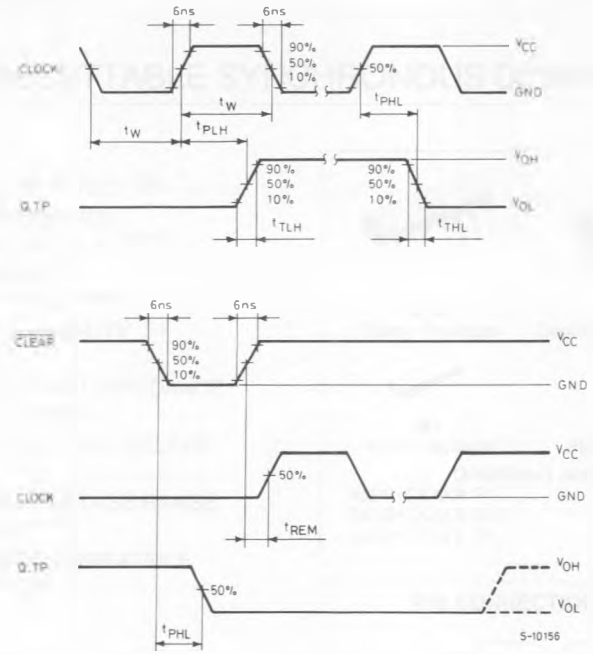
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{TLH} t_{THL}	Output Transition Time TP OUTPUT	2.0		—	132	255	—	320		385	ns
		4.5		—	33	51	—	64		77	
		6.0		—	28	43	—	55		65	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)*	2.0	B = "H"	—	264	500	—	635		750	ns
		4.5		—	66	100	—	127		150	
		6.0	A = C = D = E = "L"	—	56	85	—	110		127	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)**	2.0	B = "H"	—	236	455	—	571		676	ns
		4.5		—	59	91	—	115		136	
		6.0	A = C = D = E = "L"	—	50	77	—	100		115	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)*	2.0		—	224	425	—	535		640	ns
		4.5		—	56	85	—	107		128	
		6.0		—	48	73	—	92		109	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$-Q)**	2.0		—	204	390	—	490		585	ns
		4.5		—	51	78	—	98		117	
		6.0		—	43	67	—	84		99	
f_{MAX}	Maximum Clock Frequency*	2.0		5	13	—	4	—	3.4	—	MHz
		4.5		25	51	—	20	—	17	—	
		6.0		29	60	—	24	—	20	—	
f_{MAX}	Maximum Clock Frequency**	2.0		6	14	—	5	—	4.2	—	MHz
		4.5		32	55	—	26	—	21	—	
		6.0		38	65	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width CK)	2.0		—	36	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
$t_{W(L)}$	Minimum Pulse Width CLEAR*	2.0		—	60	150	—	190		225	ns
		4.5		—	15	30	—	38		45	
		6.0		—	13	26	—	33		38	
$t_{W(L)}$	Minimum Pulse Width CLEAR**	2.0		—	72	175	—	220		265	ns
		4.5		—	18	35	—	44		53	
		6.0		—	15	30	—	37		45	
t_{REM}	Minimum Removal Time $\overline{CLEAR}$	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC7292	—	22	—	—	—			pF
			M54/74HC7294	—	23	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

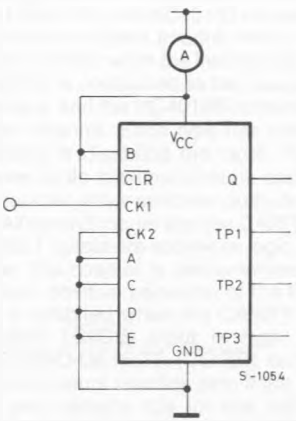
* M54/74HC7292
** M54/74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM

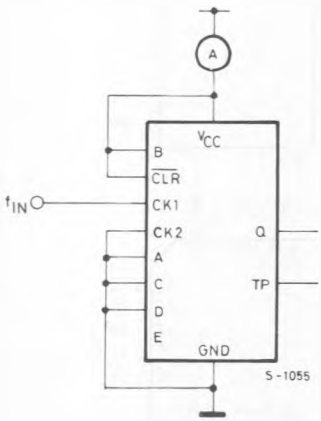


TEST CIRCUIT I_{CC} (Opr.)

HC792



HC794



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST