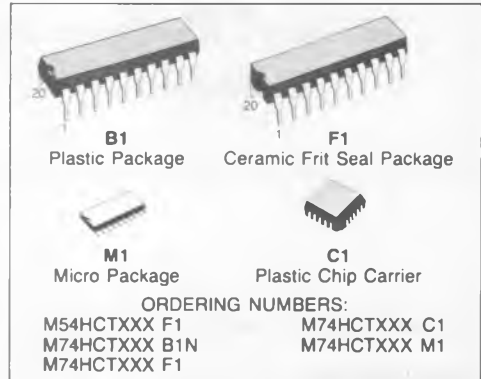


**OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT**  
**HCT563 INVERTING - HCT573 NON-INVERTING**

- **HIGH SPEED**  
 $t_{PD} = 20 \text{ ns (TYP.) at } V_{CC} = 5 \text{ V}$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**  
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = I_{OL} = 6 \text{ mA (Min.)}$
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH 54/74LS563/573


**DESCRIPTION**

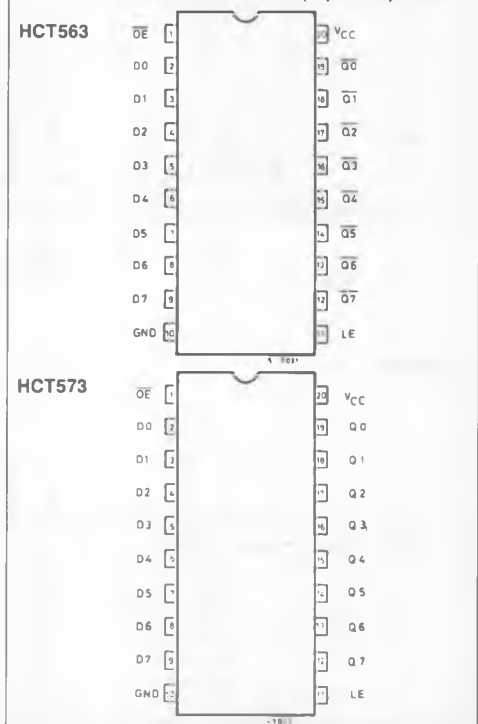
These devices are high speed C<sup>2</sup>MOS OCTAL LATCHES with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ). While the LE input is held high, the Q outputs will follow the data input precisely or inversely. The Q outputs will be latched precisely or inversely at the logic level of D input data the instant LE is taken low.

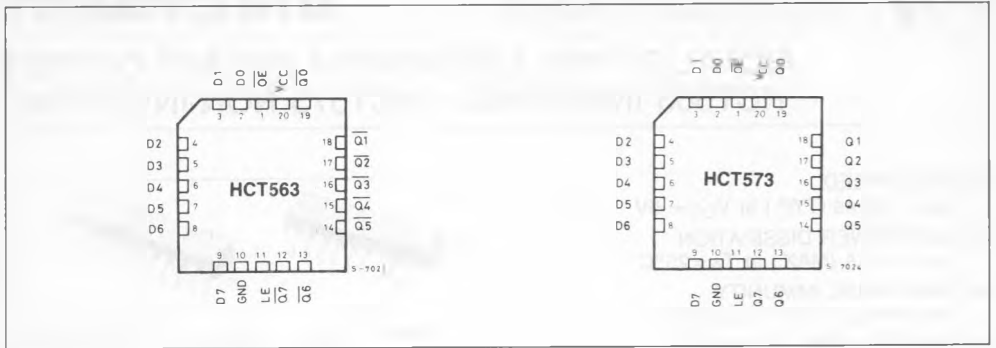
When the  $\overline{OE}$  input is low, the eight outputs will be in a normal logic state (high or low logic level) and when high the outputs will be in a high impedance state.

The application designer has a choice of a combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

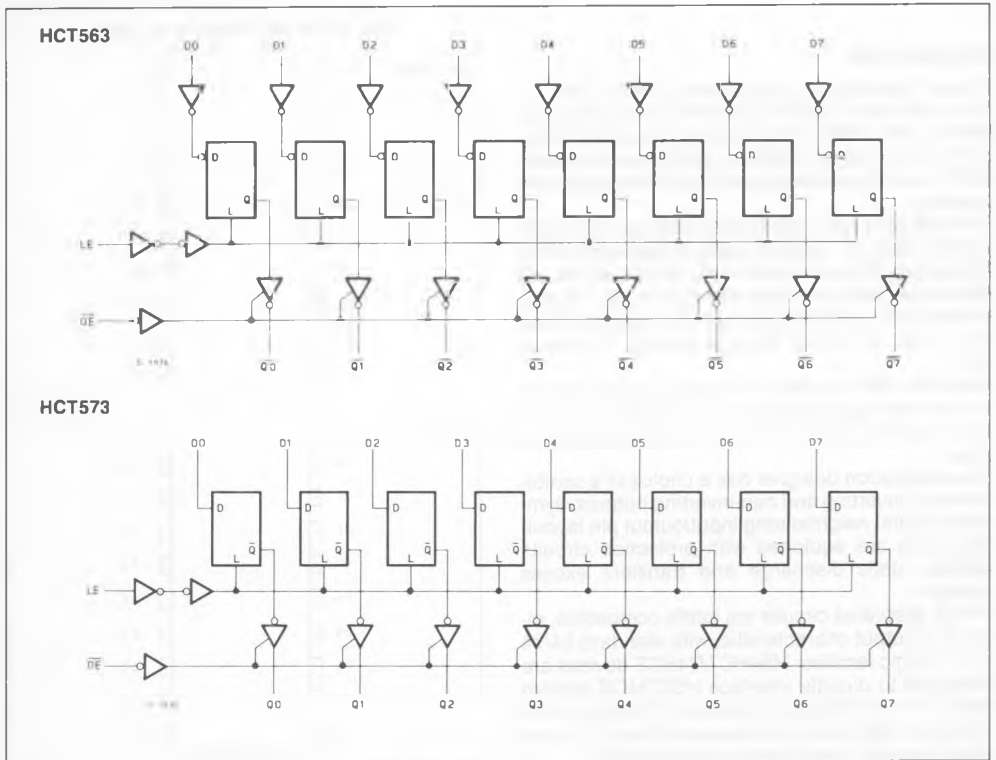
These integrated circuits are totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families. M54HCT/74HCT devices are designed to directly interface HSC<sup>2</sup>MOS system with TTL and NMOS components. These components are also plug in replacements for LSTTL devices but with lower power consumption.

**PIN CONNECTIONS (top view)**


CHIP CARRIER



LOGIC DIAGRAM



## TRUTH TABLE

INPUTS			OUTPUTS	
OE	LE	D	Q (HCT573)	$\bar{Q}$ (HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	Qn
L	H	L	L	H
L	H	H	H	L

Qn: Q/ $\bar{Q}$  OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

X: DON'T CARE HZ = HIGH IMPEDANCE

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	- 0.5 to 7	V
V <sub>I</sub>	DC Input Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 35	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 70	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(\*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

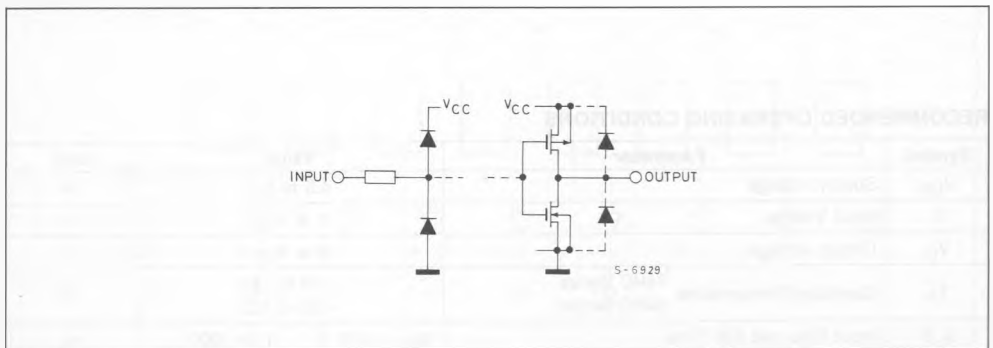
## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply Voltage	4.5 to 5.5	V	
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V	
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature	74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> 4.5V	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition		T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2	—	V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	V <sub>I</sub>	I <sub>O</sub>								V
			V <sub>IH</sub> or V <sub>IL</sub>	- 20 μA	4.4		—	4.4	—	4.4	—	
		4.5		- 6.0 mA	4.18	4.31	—	4.13	—	4.1		
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>IH</sub> or V <sub>IL</sub>	20 μA	—		0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.32	—	0.37	—	0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I <sub>OZ</sub>	3 State Output Current	5.5			—	—	± 0.5	—	± 5.0	—	± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



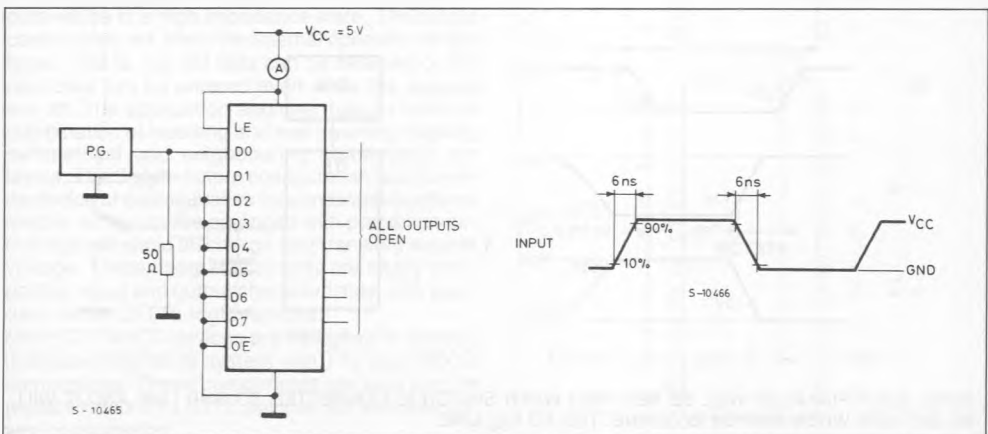
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	4.5		—	7	12	—	15		18	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (LE-Q, $\bar{Q}$ )	4.5		—	24	35	—	44		53	ns
$t_{PLH}$	Propagation Delay Time (D-Q, $\bar{Q}$ )	4.5		—	22	35	—	44		53	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	4.5		—	8	15	—	19		22	ns
$t_s$	Minimum Set-up Time	4.5		—	2	10	—	13		15	ns
$t_h$	Minimum Hold Time	4.5		—	—	5	—	5		5	ns
$t_{PZL}$ $t_{PZH}$	3-State Output Enable Time	4.5	$R_L = 1\text{K}\Omega$	—	18	35	—	44		53	ns
$t_{PLZ}$ $t_{PHZ}$	3-State Output Disable Time	4.5	$R_L = 1\text{K}\Omega$	—	26	37	—	46		56	ns
$C_{IN}$	Input Capacitance			—	5	10	—	10		10	pF
$C_{OUT}$	Output Capacitance			—	10	—	—	—	—	—	
$C_{PD} (*)$	Power Dissipation Capacitance			—	41	—	—	—	—	—	

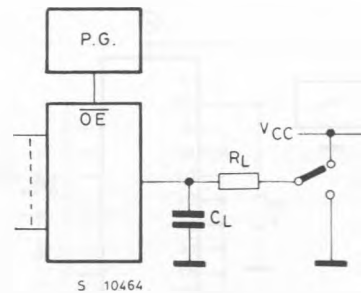
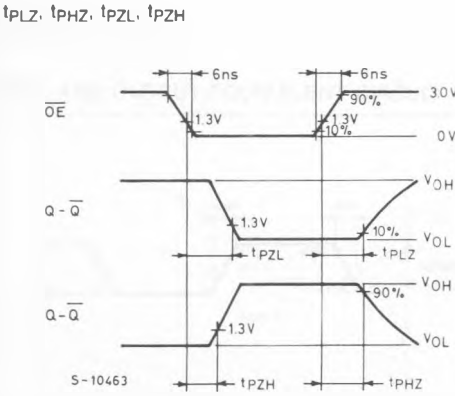
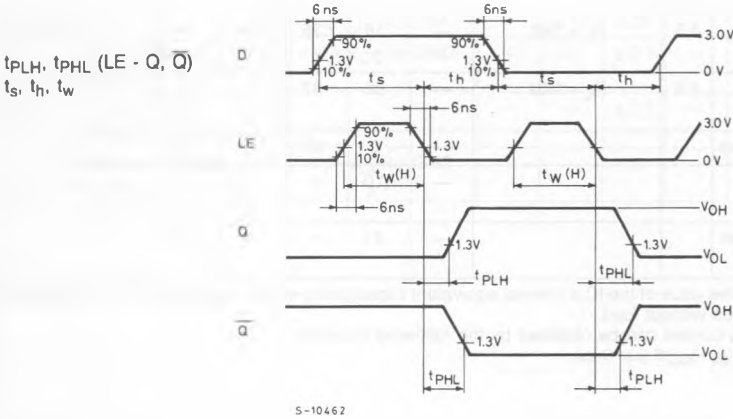
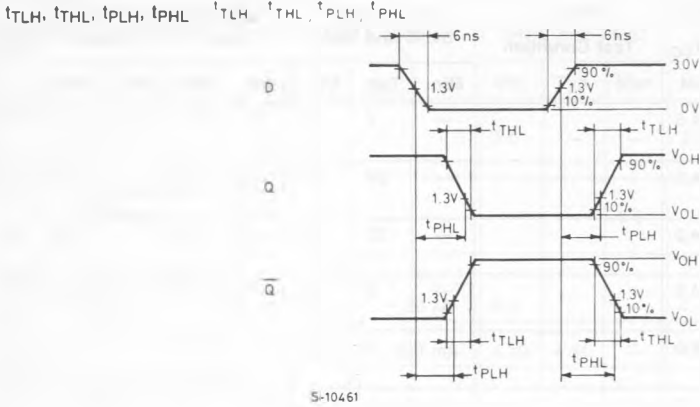
Note (\*)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$$I_{CC(\text{opr})} = C_{PD} V_{CC} f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

TEST CIRCUIT  $I_{CC}$  (Opr.)

SWITCHING CHARACTERISTICS TEST WAVEFORM



NOTE: EACH FLIP-FLOP WILL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT WILL BE SET LOW WHEN SWITCH IS CONNECTED TO  $V_{CC}$  LINE.