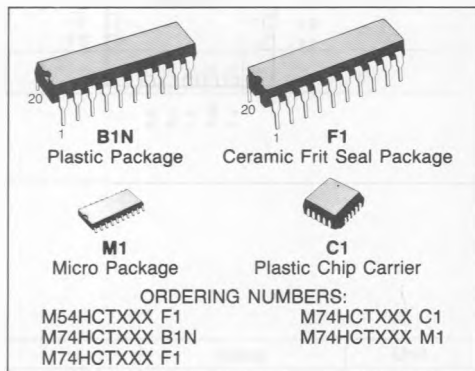


## OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

### HCT564 INVERTING - HCT574 NON-INVERTING

- **HIGH SPEED**  
 $f_{MAX} = 45 \text{ MHz (TYP) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**  
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH 54/74LS564/574

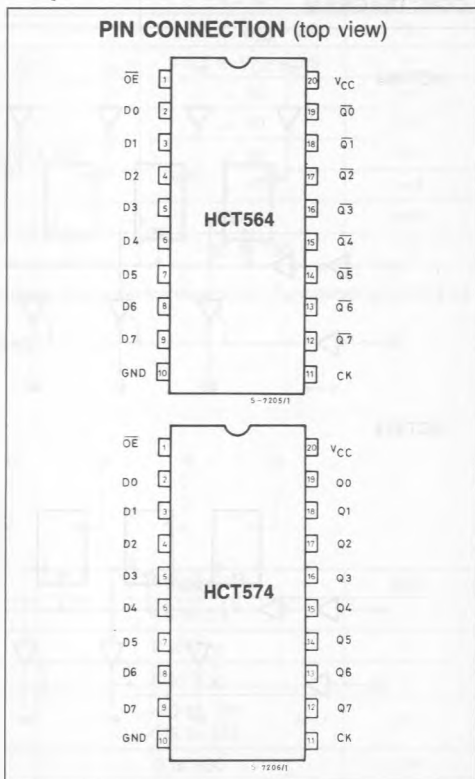


#### DESCRIPTION

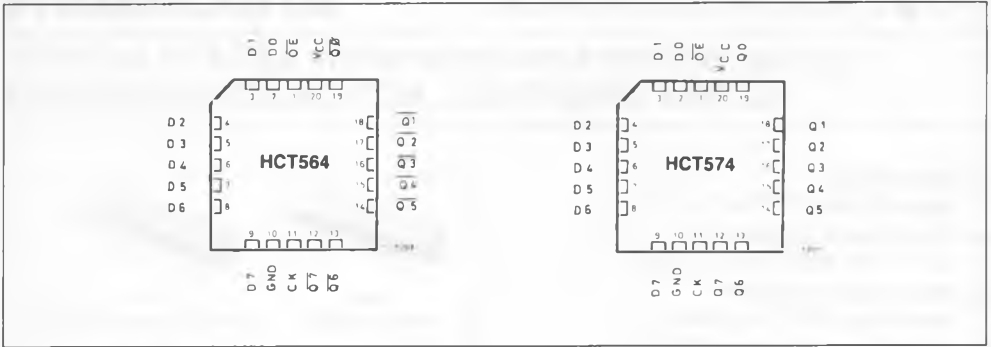
The M54/74HCT564 and M54/74HCT574 are high speed CMOS OCTAL FLIP-FLOPS with 3-STATE OUTPUTS fabricated with silicon gate C<sup>2</sup>MOS technology. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input (OE). On the positive transition of clock, the Q outputs will be set inversely to the logic state that were set-up at the D inputs. While the OE input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The 3-state output configuration and the wide choice of outline makes bus-organized systems simple. All inputs are equipped with protection circuit against static discharge and transient excess voltage. These integrated circuits are totally compatible, input and output characteristics, with standard 54/74 LSTTL logic families.

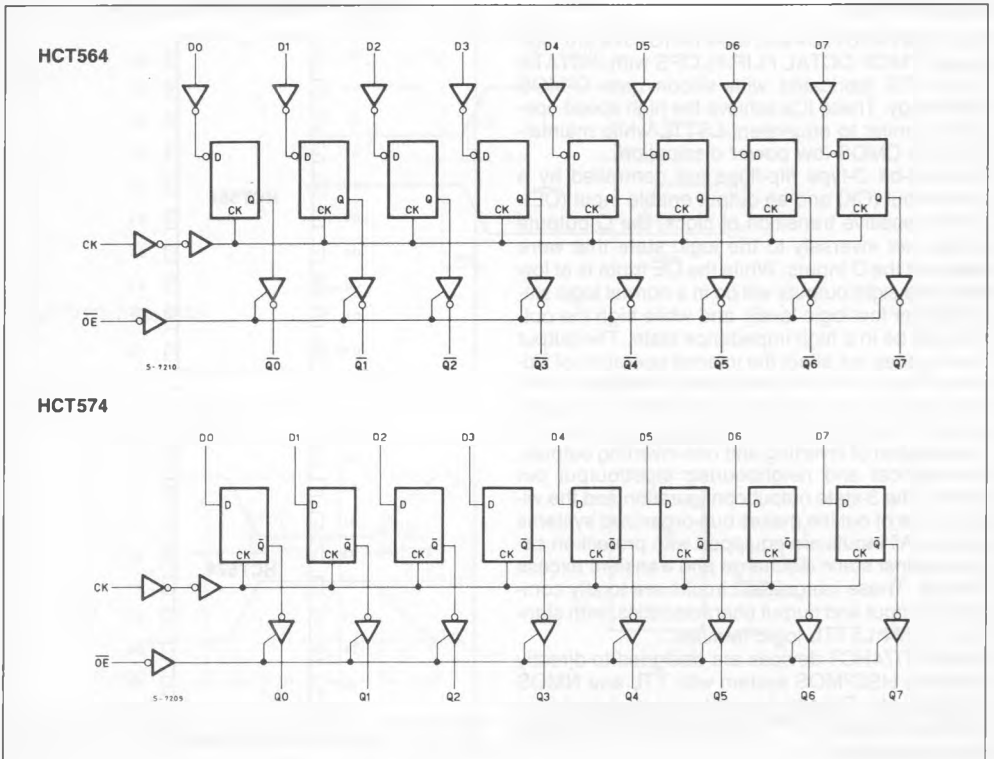
M54HCT/74HCT devices are designed to directly interface HSC<sup>2</sup>MOS system with TTL and NMOS components. These components are also plug in replacements for LSTTL devices but with low power consumption.



CHIP CARRIER



LOGIC DIAGRAM



## TRUTH TABLE

INPUTS			OUTPUTS	
OE	CK	D	Q (HCT 574)	$\bar{Q}$ (HCT 564)
H	X	X	Z	Z
L		X	NO CHANGE	NO CHANGE
L		L	L	H
L		H	H	L

X: DON'T CARE    Z: HIGH IMPEDANCE

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.5 to 7	V
$V_I$	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin	$\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	- 65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(\*) 500 mW:  $\equiv$  65 $^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$  to 85 $^{\circ}C$ .

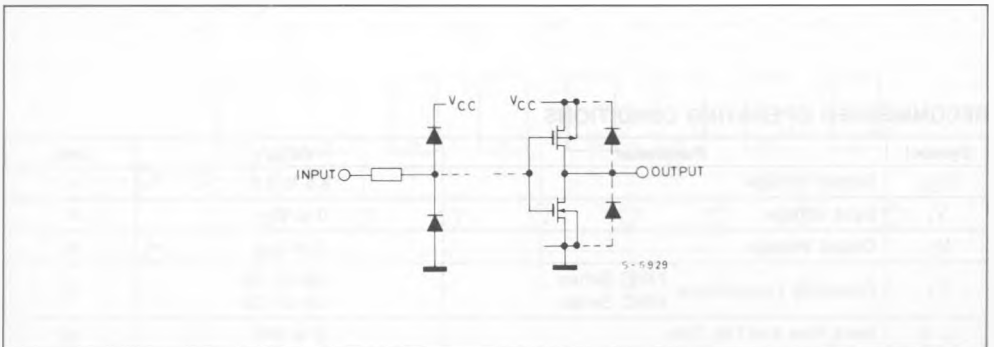
## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_A$	Operating Temperature	74HC Series - 40 to 85 54HC Series - 55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	0 to 500	ns

## DC SPECIFICATIONS

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
				$V_{IH}$	High Level Input Voltage	4.5 to 6.0		2.0 5.5	—	—		2.0
$V_{IL}$	Low Level Input Voltage	4.5 to 5.5		—	—	0.8	—	0.8	—	0.8	V	
$V_{OH}$	High Level Output Voltage	4.5	$V_I$	$I_O$								
			$V_{IH}$ or $V_{IL}$	$-20\ \mu\text{A}$	4.4	—	—	4.4	—	4.4	—	V
		4.5		$-6.0\ \text{mA}$	4.18	4.31	—	4.13	—	4.1		
$V_{OL}$	Low Level Output Voltage	4.5	$V_I$ or $V_{IL}$	$20\ \mu\text{A}$	—	—	0.1	—	0.1	—	0.1	V
				$6.0\ \text{mA}$	—	0.17	0.32	—	0.37	—	0.40	
$I_I$	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	$\pm 0.1$	—	$\pm 1.0$	—	$\pm 1.0$	$\mu\text{A}$	
$I_{OZ}$	3 State Output Current	5.5		—	—	$\pm 0.5$	—	$\pm 5.0$	—	$\pm 10$	$\mu\text{A}$	
$I_{CC}$	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	4	—	40	—	80	$\mu\text{A}$	

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



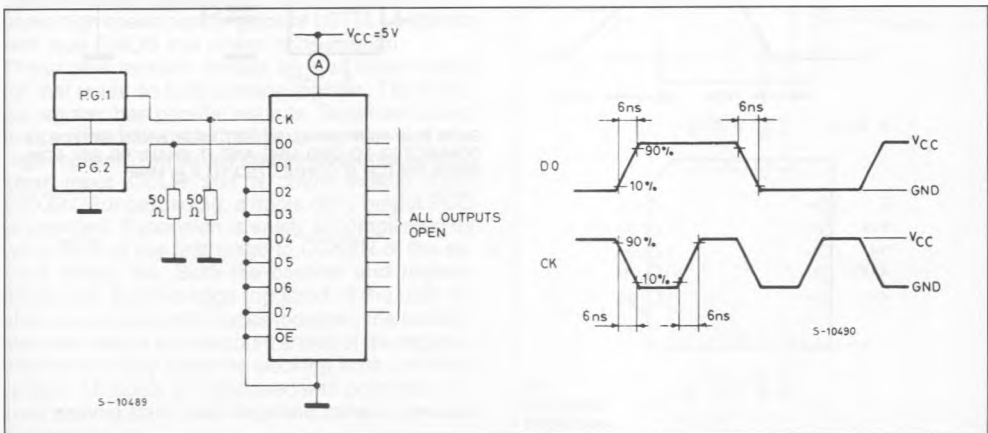
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	4.5		—	7	12	—	15	18	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CK-Q)	4.5		—	26	41	—	51	62	ns	
$f_{MAX}$	Maximum Clock Frequency	4.5		25	38	—	20	—	17	—	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	4.5		—	8	15	—	19	—	22	ns
$t_s$	Minimum Set-up Time	4.5		—	1	10	—	13	15	ns	
$t_h$	Minimum Hold Time	4.5		—	—	5	—	5	5	ns	
$t_{PZL}$ $t_{PZH}$	3-State Output Enable Time	4.5	$R_L = 1\text{K}\Omega$	—	18	35	—	44	53	ns	
$t_{PLZ}$ $t_{PHZ}$	3-State Output Disable Time	4.5	$R_L = 1\text{K}\Omega$	—	26	37	—	46	56	ns	
$C_{IN}$	Input Capacitance			—	5	10	—	10	10	pF	
$C_{OUT}$	Output Capacitance			—	10	—	—	—	—		
$C_{PD} (*)$	Power Dissipation Capacitance		HCT564 HCT574	—	60 57	—	—	—	—		

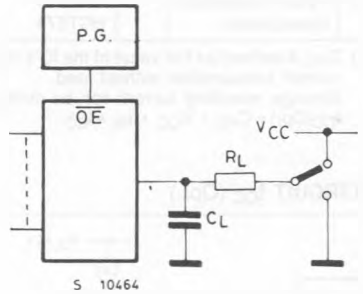
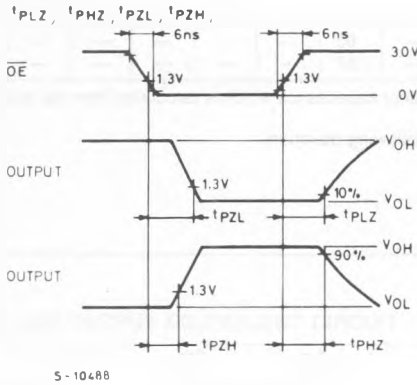
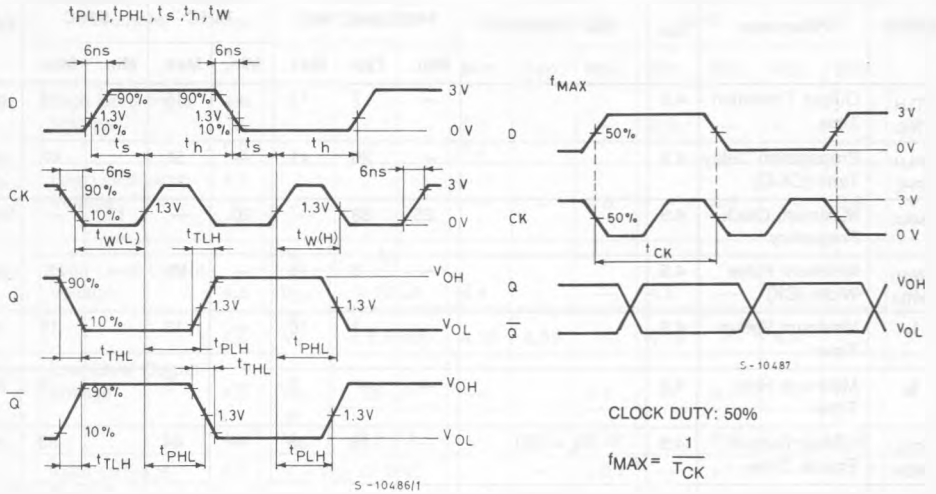
Note (\*)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$$I_{CC(Oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TEST CIRCUIT  $I_{CC}$  (Opr.)

SWITCHING CHARACTERISTICS TEST WAVEFORM



EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V<sub>CC</sub> LINE.