Description

The M65580MAP-XXXFP are semiconductor integrated circuits designed with CMOS silicon gate technology for NTSC television system, include 8bit MCU(M37272MA core) with a closed caption decoder and circuits needed for TV baseband signals(Video and Chroma) processor and Deflection in a chip. PCB area and EMI noise can be reduced by one chip and 80QFP, and internal connection of OSD signals. And it can realize a adjustment free system by built-in MCU and get a high performance adaptive YC separation by 1 line memory. The above technology makes its performance more stable and better.

Feature

- Y/C processor : 8bit Input, 10bit Output digital processing
- Deflection processor : optimized system by conventional analog and digital mixed solution
- ADC&DAC : 8bit high speed video ADC & 10bit high speed video DAC

[MCU Block]

MCU(single microcomputer) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass-production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O.
It has a OSD, data slicer , and I^2C-BUS interface. So it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

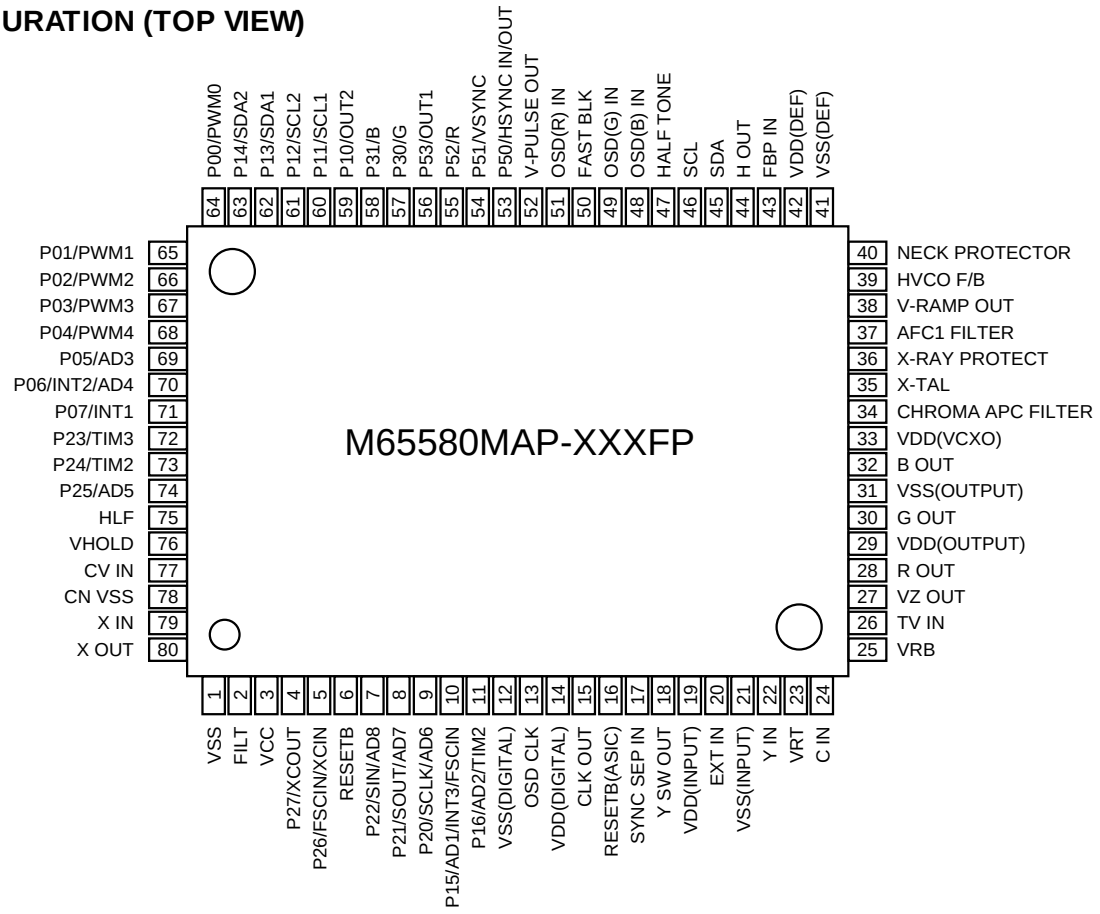
[ASIC Block]

ASIC block consists of the following blocks.
(1) Analog frontend block ; Analog SW(2 CVBS(TV&EXT) inputs, Y/C signals to one signal, 2 channels 8 bit high speed video ADCs, and ACC amplifiers
(2) Video and Chroma block ; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance blackstretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.
(3) Deflection block ; A high performance sync separation by analog and digital mixed solution
(4) Analog backend block ; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

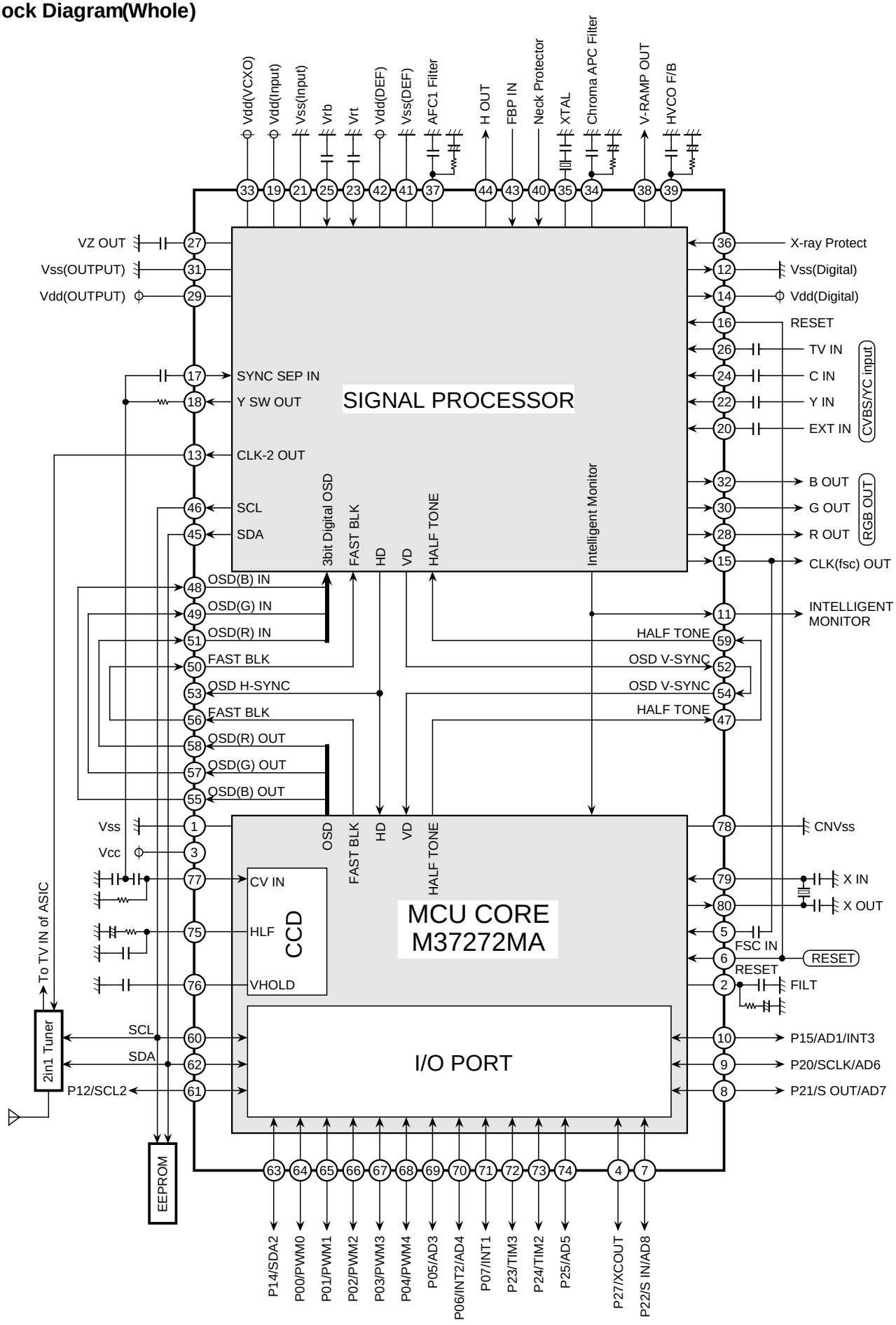
Application

NTSC TV with a closed caption decoder

PIN CONFIGURATION (TOP VIEW)



Block Diagram(Whole)



Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD} (MCU)	Supply voltage (MCU)	All voltage are based on Vss.Output transistors are cut off.	-0.3 to 6.0	V
V_{DD} (ASIC5V)	Supply voltage (ASIC5V)		-0.3 to 6.0	V
V_{DD} (ASIC3.3V)	Supply voltage (ASIC3.3V)		-0.3 to 4.0	V
V_I (MCU)	Input Voltage (MCU)		-0.3 to Vcc+0.3	V
V_O (MCU)	Output Voltage (MCU)		-0.3 to Vcc+0.3	V
I_{OH} (MCU)	Circuit current (MCU)		0 to 1 (See note 1)	mA
I_{OL1} (MCU)	Circuit current ($P0_0$-$P0_7$, $P1_0$, $P1_5$, $P1_6$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P5_2$, $P5_3$)		0 to 2 (See note 2)	mA
I_{OL2} (MCU)	Circuit current ($P1_1$-$P1_4$)		0 to 6 (See note 2)	mA
V_{ID} (ASIC)	Digital input voltage		-0.3 to Vcc+0.3	V
I_{OUT} (ASIC)	Analog output current		-30	mA
Pd	Power dissipation		1460	mW
Kt	Thermal derating		14.6	mW/˚C
Topr	Operating temperature		-20 to 65	˚C
Tstg	Storage temperature		-40 to 125	˚C

Recommended operating condition

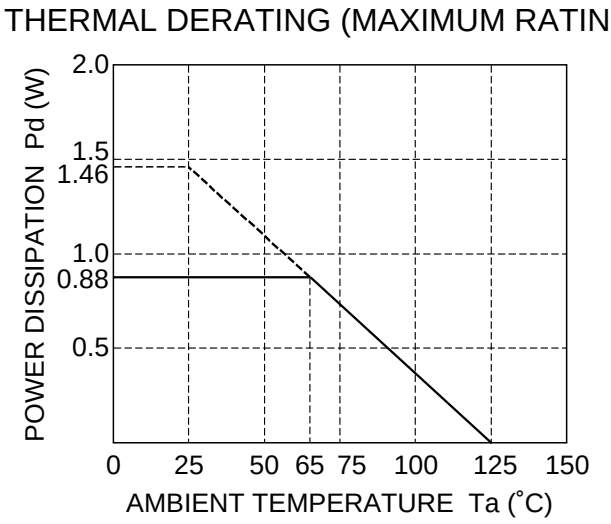
(Ta=-20 to 65 ˚C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD} (MCU)	Supply voltage (MCU) (See note 3)	4.75	5.0	5.25	V
V_{DD} (Digital)	Supply voltage (Digital)	4.75	5.0	5.25	V
V_{DD} (Input)	Supply voltage (Input)	3.13	3.3	3.47	V
V_{DD} (Output)	Supply voltage (Output)	3.13	3.3	3.47	V
V_{DD} (VCXO)	Supply voltage (VCXO)	4.75	5.0	5.25	V
V_{DD} (DEF)	Supply voltage (DEF)	4.75	5.0	5.25	V
V_{IH1} (MCU)	High Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_6$, $P2_0$-$P2_7$, $P5_0$, $P5_1$, RESETB, X_{IN}	0.8Vcc		Vcc	V
V_{IH2} (MCU)	High Input voltage SCL1, SCL2, SDA1, SDA2 (When using I^2C-Bus)	0.7Vcc		Vcc	V
V_{IH3} (ASIC)	High Input voltage RESETB, FBP IN, HALF TONE, OSD(R/G/B) IN, FAST BLK	0.8Vcc		Vcc	V
V_{IL1} (MCU)	Low Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_6$, $P2_0$-$P2_7$	0		0.4Vcc	V
V_{IL2} (MCU)	Low Input voltage SCL1, SCL2, SDA1, SDA2 (When using I^2C-Bus)	0		0.3Vcc	V
V_{IL3} (MCU)	Low Input voltage (See note 4) $P5_0$, $P5_1$, RESETB, X_{IN}, TIM2, TIM3, INT1, INT2, INT3, S_{IN}, S_{CLK}	0		0.2Vcc	V
V_{IL4} (ASIC)	Low Input voltage RESETB, FBP IN, HALF TONE, OSD(R/G/B) IN, FAST BLK	0		0.2Vcc	V
I_{OH} (MCU)	High average output current (See note 1) $P1_0$-$P1_6$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P5_2$, $P5_3$			1	mA

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
I_{OL1} (MCU)	Low average output current (See note 2) P0$_0$-P0$_7$, P1$_0$, P1$_5$, P1$_6$, P2$_0$-P2$_7$, P3$_0$, P3$_1$, P5$_2$, P5$_3$			2	mA
I_{OL2} (MCU)	Low average output current (See note 2) P1$_1$-P1$_4$			6	mA
f(X_{IN}) (MCU)	Oscillation frequency (for CPU operation) X_{IN} (See note 5)	7.9	8.0	8.1	MHz
f(X_{CIN}) (MCU)	Oscillation frequency (for sub-clock operation) X_{CIN}	29	32	35	kHz
FSC_{IN} (MCU)	Oscillation frequency (for OSD standard clock) FSC_{IN}	——	3.58	——	MHz
f_{hs1} (MCU)	Input frequency TIM2, TIM3, INT1, INT2, INT3			100	kHz
f_{hs2} (MCU)	Input frequency S_{CLK}			1	MHz
f_{hs3} (MCU)	Input frequency SCL1, SCL2			400	kHz
V_I (MCU)	Input amplitude video signal CV_{IN}	1.5	2.0	2.5	V

Note 1: The total current that flows out the MCU must be 20mA or less.
2: The total input current to MCU (I_{OL1}+I_{OL2}) must be 30mA or less.
3: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8MHz.
4: Pin name in each parameter is described pin names.
(1) Dedicated pins: dedicated pin name.
(2) Double-/Triple-function ports.
When the same limits: I/O port name.
When the limits of function except ports are different from I/O port limits; function pin name.
5: P0$_6$, P0$_7$, P1$_5$, P2$_3$, P2$_4$ have the hysteresis when these pins are used as interrupt input pins or timer pins.
P1$_1$-P1$_4$ have the hysteresis when these pins are used as multi-master I^2C-Bus interface ports.
P2$_0$-P2$_2$ have the hysteresis when these pins are used as serial I/O pins.

Thermal derating



[MCU Block(M37272MA)]

Description

MCU(single microcomputers) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass-production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O.
It has a OSD, data slicer , and I^2C-BUS interface, so it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

Features

- Number of basic instructions -------- 71
- Memory size
  - ROM -------- 40Kbytes
  - RAM -------- 1152bytes
    (ROM correction memory:64bytes included)
- minimum instruction execution time --------- 0.5µs
  (at 8 MHz oscillation frequency)
- Power source voltage -------- 5V±10%
- Subroutine nesting -------- 128 levels(max.)
- Interrupts -------- 17bytes 16vector
- 8-bit timers -------- 6
- Programmable I/O ports(Ports P0,P1,P2) -------- 23
- Input ports(Ports P50,P51) -------- 2
- Output ports(Ports P30,P31,P52,P53) -------- 4
- Serial I/O -------- 8-bit x 1channel
- Multi-master I^2C-BUS interface -------- 1(2 systems)
- A-D comparator (7-bit resolution) -------- 8 channels
- PWM output circuit -------- 8-bit x 5
- ROM correction function -------- 32 bytes x 2

Power dissipation -------- 165mW
(at Vcc=5.5V, 8MHz oscillation frequency, OSD on, and Data slicer on)

- Closed caption data slicer
- OSD function

Display characters -------- 32 characters x 2 lines(possible to display 3 lines or more by software)
Kinds of characters 254 kinds
Character display area CC mode : 16x26 dots
OSD mode : 16x20 dots
Kinds of character sizes CC mode : 1 kind
OSD mode : 8 kinds
Kinds of character colors 8 colors(R,G,B) (coloring unit: a character)
Kinds of background colors CC mode : 1 kind(black)
OSD mode : 8 kinds(possible to select color in character unit)
Display position horizontal : 128 levels Vertical : 512 levels
Attribute CC mode : smooth italic, underline, flash, automatic solid space
OSD mode : border(black)
Kinds of raster colors 8 kinds
Smooth roll-up
Window function

[ASIC Block]

Description

CVBS(TV/EXT) signals or Y/C signals input to this IC are converted to 8 bit digital signal by 2 channels high speed video ADCs. These signals are input to digital section to obtain high performance R/G/B signals. First, CVBS signals are separated to high quality Y/C signals by 2 dimensional adaptive YC separation circuit, and then Y/C signals are converted to R-Y&B-Y signals by digital chroma decoder, after that, to R/G/B signals by RGB matrix circuit. These signals are mixed with OSD signals come from MCU block, are converted to analog R/G/B signals by 3 channel 10 bit high speed video DACs. In deflection block, to get a better Horizontal & Vertical signals, a conventional analog solution by analog CMOS technology is used.

ASIC block consists of the followings blocks.

(1) Analog frontend block ; Analog SW(2 CVBS(TV&EXT) inputs, Y/C signals to one signal), 2 channels 8 bit high speed video ADCs , and ACC amplifiers

(2) Video and Chroma block ; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance blackstretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.

(3) Deflection block ; A high performance sync separation by analog and digital mixed solution

(4) Analog backend block ; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

Features

[Video/Chroma Block]

- Built-in 1 Video SW for TV/EXT signal input
- 2 additional pins for S(Y/C) input
- YUV input signal available (T.B.D)
- 2 channel 8 bit Video ADCs for CVBS(TV&EXT) or Y/C signal inputs
- Built-in adaptive 2 line comb filter(2DYCS) => Few dot crawl&crosscolor, and clear color transition
- Built-in a high performance Blackstretch => Dynamic & detailed picture
- Digital Luminance delay circuit => stable Y/C timing adjustment
- Built-in VCXO circuit(4fsc)
- High resolution R/G/B output => Built-in 10bit high speed Video DACs
- Internal connection of 8 color digital OSD (R/G/B, F.B, H.T)
- Reference CLK output for tuner (fsc or 4MHz)
- Built-in YNR (about fsc±1MHz)
- Gamma correction(for R/G/B signals)

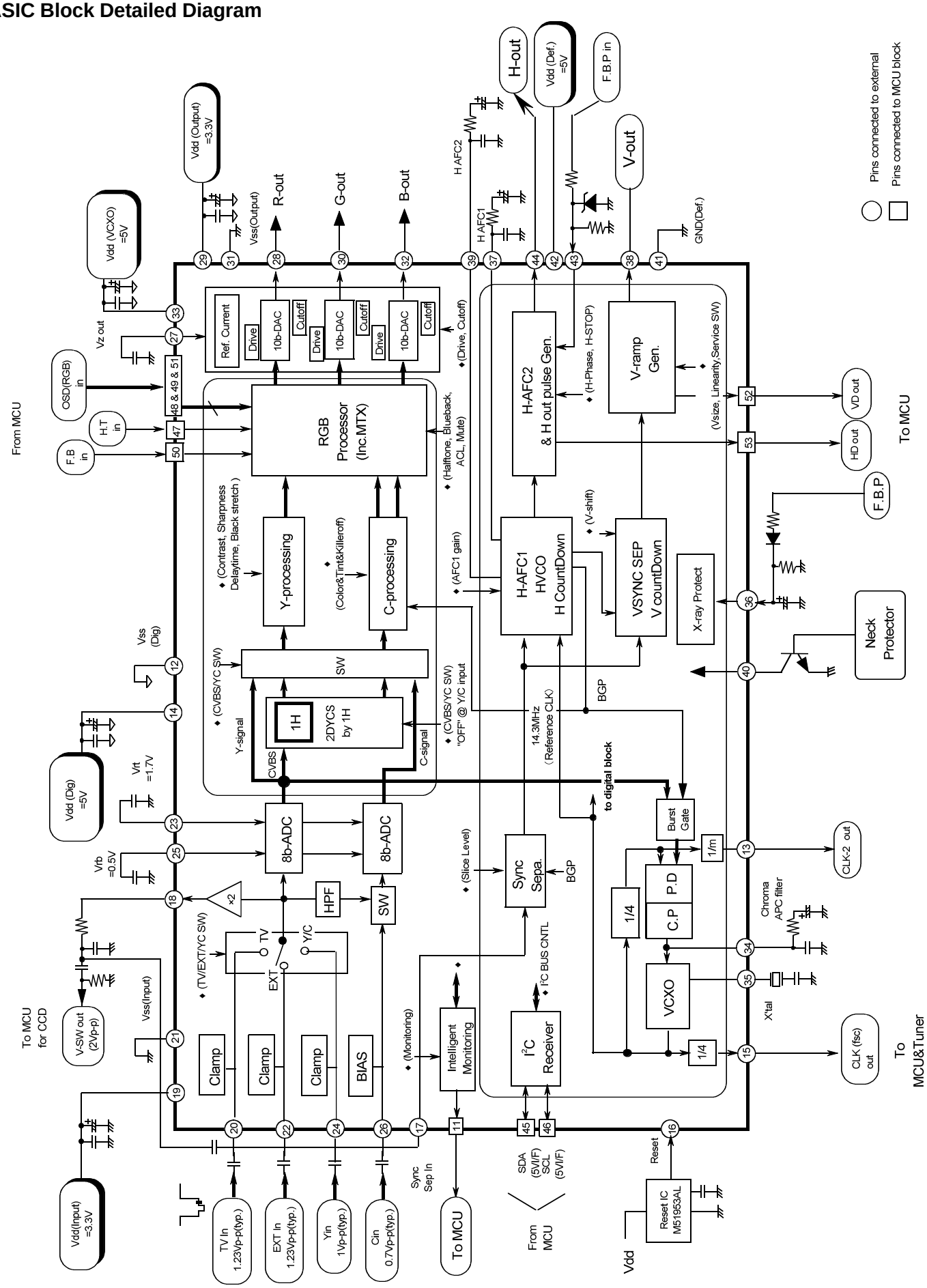
[Deflection Block]

- Analog(conventional) sync separation => Better performance by abundant experience
- Double AFC Circuit => Stable Horizontal scanning
- Built-in Horizontal reference Oscillator => No ceramic resonator and Adjustment free
- HD and VD pulse by Countdown => Stable HD&VD
- Built-in digital Vramp generator

[List of main I²C bus controllable Items]

- Chip : Power-down mode
- Analog Input Stage : CVBS/Y&C Input SW
- Luminance Processing : Sharpness, Blackstretch
- Chroma Processing : Color, Tint, Killer level
- RGB Matrix : ACL, OSD Input Level, Contrast, Brightness
- Analog Output Stage : Drive adj.(R/G/B), Cutoff adj.(R/G/B)
- Deflection Block : H-Phase, V-size, V-shift, V-Linearity

ASIC Block Detailed Diagram



Function and Outline of ASIC Block

Chip

Power down mode : 3 modes [PD0 & PD1 & PD2]
Service SW : stop of Vertical(Vramp) output (For cutoff adjustment)

Analog Block

• Input stage => CVBS&Y/C input signals
Input level (CVBS) : 1.23Vp-p (173IRE) @max. / 1.0Vp-p @typ.
Input level (Y/C) : Y:1.00Vp-p (140IRE) @typ./ C:0.7Vp-p @typ.
• Output stage => RGB output signals
Output level : 0.7 Vp-p (typ.)
Drive(R&G&B) : -3 to +4 dB by 7bit (White Balance)
Cutoff(R&G&B) : 0.5 V by 9bit (Start lighting point)

Digital Block

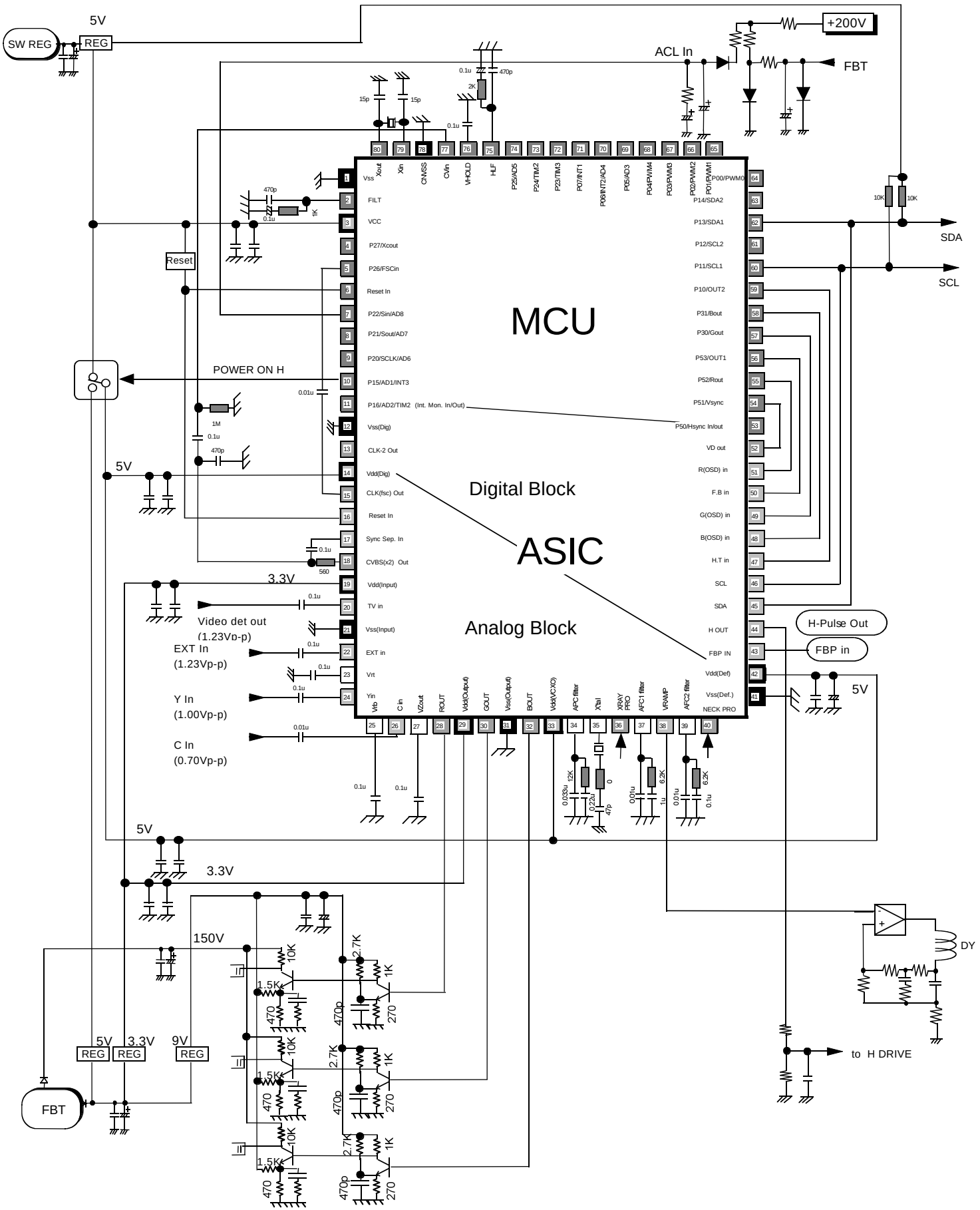
• 2DYCS
Adaptive YC separation by using of 1H line memory and original algorithm
• Luminance processing
Contrast : 0 to 200 LSB by 7bit
Brightness : -20 to 20 LSB by 8bit (Pedestal DC level)
Sharpness : 0 to 3 dB by 5bit (by 0, 70, 140, 210ns)
Delay adjustment : 0 to 210 ns by 2bit(70ns step) to Chroma signal
Blackstretch : 3 selectable stretch point
[Stretch areas (0 to 25/30/40IRE), Through areas (25/30/40IRE ~)]
4 selectable blackstretch curves (1/4, 2/4, 3/4, 4/4)
• Chroma processing
Tint : -45 to 45 degree by 7bit => about 0.7 degree
: Variable demodulator (R-Y) axis
(-22.5 to +22.5 degree by 6bit => about 0.7 degree)
Color : 0 to 200 % by 7bit

• RGB matrix
: Matrix(R-Y signal) ratio selectable (12/8, 13/8, 14/8)
ACL : Automatic Contrast Limiter by MCU port(ADC) and I^2C bus
EXT/RGB : clip to 7LSB @ data < 0Fh
BlueBack : ON/OFF selectable
Mute : ON/OFF of R/G/B output
Neck Protector : R/G/B output to zero(no signal)

Deflection Block

• Horizontal Output
AFC2 phase : +5 to -5µs by 5bit
Hold => Shut down : fh@Hold-down : in about 16.5KHz => fh@Shutdown : H-STOP
AFC1 gain : Normal/High selectable for VTR skew
• Vertical Output
V position : 0 to 16 H by 3 bit => 2H unit(connected with BLK)
V size : 1.4 to 2.6 V by 7bit
Linearity : 0 to 30 % by 7bit

Application Examples



Electrical characteristics

(Ta=25ºC, Vdd=5.0V, 3.3V)

Symbol	Parameter	Input signal		Test point	Limits			Unit	Remarks
		Pins	SG		Min.	Typ.	Max.		
ICC	Standard conditions								
ICC50	5.0V supply current	-	-	3,14, 33,42	102	116	130	mA	Supply of MCU, Digital, VCXO and Deflection
ICC33	3.3V supply current	-	-	18, 29	47	56	65	mA	Supply of A/D and D/A
VIDEO	Standard conditions of video character	-	-	-	-	-	-	-	
2AGTV	Video SW output level (TV input)	26	SG.A	18	1.5	1.7	1.9	V_{pp}	
2AGEV	Video SW output level (External input)	20	SG.A	18	1.5	1.7	1.9	V_{pp}	
Vtyp	Video standard output	26	SG.A	28,30, 32	590	740	890	mV_{pp}	
FBY	Video frequency characteristics	26	SG.B	28,30, 32	-3	0	3	dB	f=5MHz
Y/C1	Y/C separation function 1	26	SG.E	28,30, 32	-	-30	-20	dB	feb=fec=fsc
Y/C2	Y/C separation function 2	26	SG.E	28,30, 32	-3	0	3	dB	feb=fsc, fec=fsc±1/2f_H
Y/C3	Y/C separation function 3	26	SG.E	28,30, 32	-	-30	-20	dB	feb=fsc, fec=fsc±f_H
YDL0	Y total delay time	26	SG.A	28,30, 32	2.4	3.0	3.6	µsec	
YDL1	Y delay time 1	26	SG.A	28,30, 32	50	70	90	nsec	YDL1=measure – YDL0
YDL2	Y delay time 2	26	SG.A	28,30, 32	50	70	90	nsec	YDL2=measure – YDL1
YDL3	Y delay time 3	26	SG.A	28,30, 32	50	70	90	nsec	YDL3=measure – YDL2
GTnor	Video tone control characteristic 1	26	SG.B	28,30, 32	640	800	960	mV	f=2.5MHz
GTmax	Video tone control characteristic 2	26	SG.B	28,30, 32	1	2.5	4	dB	f=2.5MHz
GTmin	Video tone control characteristic 3	26	SG.B	28,30, 32	-7	-4	-1	dB	f=2.5MHz
BLS	Black stretch characteristic	26	SG.D	28,30, 32	20	50	80	mV	Vy=0.18V, 45H=80h(BLS ON) / 00h(BLS OFF)
HT	Half Tone function	26	SG.A	28,30, 32	-9	-6	-3	dB	

Symbol	Parameter	Input signal		Test point	Limits			Unit	Remarks
		Pins	SG		Min.	Typ.	Max.		
CHROMA	Standard condition of chroma parameter	-	-	-	-	-	-	-	5DH=03h
CnorR	Chroma standard output (R-Y)	26	SG.E	28	155	180	205	mV	f_{eb}=f_{ec}+50kHz
CnorB	Chroma standard output (B-Y)	26	SG.E	32	275	310	345	mV	f_{eb}=f_{ec}+50kHz
ACC1	ACC characteristic 1	26	SG.E	28	-3	0	3	dB	V_{eb}, V_{ec} : +6dB of typical input level
ACC2	ACC characteristic 2	26	SG.E	28	-3	0	3	dB	V_{eb}, V_{ec} : -20dB of typical input level
VikN	Killer operation input level	26	SG.E	28	-40	-35	-30	dB	V_{eb}, V_{ec} : variable
KillP	Color residual at Killer on	26	SG.E	28	-	-40	-28	dB	V_{eb} = 0mV
APCU	APC pull-in range (upper)	26	SG.E	28	400	-	-	Hz	f_{eb}=f_{ec} : variable
APCL	APC pull-in range (lower)	26	SG.E	28	-	-	-400	Hz	f_{eb}=f_{ec} : variable
DEMR	Demodulated output ratio	26	SG.E	28,32	0.47	0.57	0.67	-	f_{eb}=f_{ec}+50kHz
DEMP	Demodulation phase angle	26	SG.F	28,32	85	90	95	deg	
Ccon 1	Color control characteristic 1	26	SG.E	28	160	200	240	%	f_{eb}=f_{ec}+50kHz
Ccon 2	Color control characteristic 2	26	SG.E	28	-	0	10	%	f_{eb}=f_{ec}+50kHz
TC1	TINT control characteristic 1	26	SG.F	28,32	30	45	60	deg	
TC2	TINT control characteristic 2	26	SG.F	28,32	-60	-45	-30	deg	
Fclk	CLK output frequency	26	SG.C	15	3.578	3.579	3.580	MHz	
Vclk	CLK output amplitude	26	SG.C	15	350	500	650	mV_{pp}	

Symbol	Parameter	Input signal		Test point	Limits			Unit	Remarks
		Pins	SG		Min.	Typ.	Max.		
RGB	Standard condition of RGB parameter	-	-	-	-	-	-	-	
VPED	Output Pedestal voltage	26	SG.D	28,30, 32	2.7	3.0	3.3	V	V_y = 0.0V
MTXRB	Matrix ratio R/B	26	SG.H	28,32	0.74	0.92	1.10	-	
MTXGB	Matrix ratio G/B	26	SG.H	30,32	0.24	0.33	0.42	-	
GYmax	Contrast control characteristic 1	26	SG.D	28,30, 32	160	200	240	%	Vy =0.286V
GYmin	Contrast control characteristic 2	26	SG.D	28,30, 32	-	0	10	%	Vy =0.286V
GYEclip	Contrast control characteristic 5	48,49, 51	SG.G	28,30, 32	250	300	350	mV	
Lum max	Brightness control characteristic 2	26	SG.D	28,30, 32	100	150	200	mV	
Lum min	Brightness control characteristic 3	26	SG.D	28,30, 32	-200	-150	-100	mV	Vy =0.286V
D(R)1	R Drive control characteristic 1	26	SG.D	28	1.5	3.5	5.5	dB	Vy =0.286V
D(G)1	G Drive control characteristic 1	26	SG.D	30	1.5	3.5	5.5	dB	Vy =0.286V
D(B)1	B Drive control characteristic 1	26	SG.D	32	1.5	3.5	5.5	dB	Vy =0.286V
D(R)2	R Drive control characteristic 2	26	SG.D	28	-4.6	-2.6	-0.6	dB	Vy =0.286V
D(G)2	G Drive control characteristic 2	26	SG.D	30	-4.6	-2.6	-0.6	dB	Vy =0.286V
D(B)2	B Drive control characteristic 2	26	SG.D	32	-4.6	-2.6	-0.6	dB	Vy =0.286V
C(R)1	R Cut off control characteristic 1	26	SG.D	28	210	260	310	mV	Vy =0.286V
C(G)1	G Cut off control characteristic 1	26	SG.D	30	210	260	310	mV	Vy =0.286V
C(B)1	B Cut off control characteristic 1	26	SG.D	32	210	260	310	mV	Vy =0.286V
C(R)2	R Cut off control characteristic 2	26	SG.D	28	-310	-260	-210	mV	Vy =0.286V
C(G)2	G Cut off control characteristic 2	26	SG.D	30	-310	-260	-210	mV	Vy =0.286V
C(B)2	B Cut off control characteristic 2	26	SG.D	32	-310	-260	-210	mV	Vy =0.286V
OSD(R)	OSD (R) output level	51	SG.G	28	500	600	700	mV_{pp}	
OSD(G)	OSD (G) output level	49	SG.G	30	500	600	700	mV_{pp}	
OSD(B)	OSD (B) output level	48	SG.G	32	500	600	700	mV_{pp}	
SOSD1	OSD speed characteristic 1	48,49, 51	SG.G	28,30, 32	-	100	200	nsec	
SOSD2	OSD speed characteristic 2	48,49, 51	SG.G	28,30, 32	-	100	200	nsec	
OFF(R)	Offset voltage between R and OSD(R)	-	-	-	-50	0	50	mV	Difference at pedestal level
OFF(G)	Offset voltage between G and OSD(G)	-	-	-	-50	0	50	mV	Difference at pedestal level
OFF(B)	Offset voltage between B and OSD(B)	-	-	-	-50	0	50	mV	Difference at pedestal level
NECK	Neck protector function threshold voltage	26	SG.A	40	1.0	1.3	1.6	V	while monitoring at pins 28, 30, 32

Symbol	Parameter	Input signal		Test point	Limits			Unit	Remarks
		Pins	SG		Min.	Typ.	Max.		
DEF	Standard condition of defrection parameter	-	-	-	-	-	-	-	
fH1	Horizontal free-running frequency 1	-	-	44	15.53	15.73	15.93	kHz	
fH2	Horizontal free-running frequency 2	-	-	44	13.72	14.32	14.92	kHz	
fH3	Horizontal free-running frequency 3	-	-	44	17.25	17.85	18.45	kHz	
FPHU	Horizontal pull-in range (upper)	17	SG.I	44	250	500	-	Hz	Vary frequency of input signal.
FPHL	Horizontal pull-in range (lower)	17	SG.I	44	-	-500	-250	Hz	Vary frequency of input signal.
HPV	Horizontal pulse amplitude	26	SG.A	44	4.0	4.5	5.0	V	
HPTW	Horizontal pulse width	26	SG.A	44	19.3	22.3	25.3	µsec	
HPD	Horizontal pulse duty cycle	26	SG.A	44	30	35	40	%	
HPT1	Horizontal pulse timing 1	26	SG.A	44	8.7	10.7	12.7	µsec	
HPT2	Horizontal pulse timing 2	26	SG.A	44	2.2	4.2	6.2	µsec	
HPT3	Horizontal pulse timing variable range	26	SG.A	44	4.5	6.5	8.5	µsec	HPT2 – HPT1
HDOWN	Hold down function threshold voltage	26	SG.A	36	3.0	3.1	3.2	V	while monitoring at pin 44
SDOWN	Shut down function threshold voltage	26	SG.A	36	3.3	3.5	3.7	V	while monitoring at pin 44
fV	Vertical free-running frequency	-	-	38	55	60	65	Hz	
SVC	Service mode function	-	-	38	2.5	2.8	3.1	V	
FPVU	Vertical pull-in frequency (upper)	17	SG.J	38	-	-	63	Hz	Vary frequency of input signal.
FPVL	Vertical pull-in frequency (lower)	17	SG.J	38	57	-	-	Hz	Vary frequency of input signal.
VRsi 1	Vertical ramp size	26	SG.A	38	2.1	2.5	2.9	V_{pp}	
VRsc 1	Vertical ramp size control range 1	26	SG.A	38	20	27	35	%	
VRsc 2	Vertical ramp size control range 2	26	SG.A	38	-35	-27	-20	%	
VLin 1	Vertical ramp Linearity control range 1	26	SG.A	38	-5	0	5	%	
VLin 2	Vertical ramp Linearity control range 2	26	SG.A	38	19	24	29	%	
VRpo 1	Vertical ramp position control range 1	26	SG.A	38	0	50	200	µsec	
VRpo 2	Vertical ramp position control range 2	26	SG.A	38	790	940	1090	µsec	(Measured value) – (Vrpo 1)
VW	Vertical pulse width	26	SG.A	52	0.35	0.53	0.65	msec	
VBLKW	Vertical blanking width	26	SG.A	28,30, 32	1.52	1.64	1.76	msec	
WVSS	Minimum vertical sync detection width	26	SG.A	11	13	18	23	µsec	

Electrical characteristics (MCU part)

(Vcc=5V±10%, Vss = 0V, f(X_{IN})=8MHz, Ta=–20˚C to 65˚C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit	Test circuit
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	OSD OFF Data slicer OFF		15	30	mA	1
				OSD ON		30	45		
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32 kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = "0", CM6 = "1")			60	200	µA	
		Wait mode	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz			2	4	mA	
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32 kHz, Low-power dissipation mode set (CM5 = "0", CM6 = "1")			25	100	µA	
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 0			1	10		
V_{OH}	HIGH output voltage P1_0–P1_6, P2_0–P2_7, P3_0, P3_1, P5_2, P5_3		V_{CC} = 4.5 V, I_{OH} = –0.5 mA		2.4			V	2
V_{OL}	LOW output voltage P0_0–P0_7, P1_0, P1_5, P1_6, P2_0–P2_7, P3_0, P3_1, P5_2, P5_3		V_{CC} = 4.5 V, I_{OL} = 0.5 mA				0.4	V	
	LOW output voltage P1_1–P1_4		V_{CC} = 4.5 V	I_{OL} = 3 mA			0.4		
				I_{OL} = 6 mA			0.6		
$V_{T+} – V_{T–}$	Hysteresis (See note 1) $\overline{RESET}$, P5_0–P5_1, INT1, INT2, INT3, TIM2, TIM3, S_{IN}, S_{CLK}, SCL1, SCL2, SDA1, SDA2		V_{CC} = 5.0 V			0.5	1.3	V	3
I_{IZH}	HIGH input leak current P0_0–P0_7, P1_0–P1_6, P2_0–P2_7, P5_0, P5_1, $\overline{RESET}$		V_{CC} = 5.5 V, V_I = 5.5 V				5	µA	4
I_{IZL}	LOW input leak current P0_0–P0_7, P1_0–P1_6, P2_0–P2_7, P5_0, P5_1, $\overline{RESET}$		V_{CC} = 5.5 V, V_I = 0 V				5	µA	4
R_{BS}	I^2C-BUS • BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V_{CC} = 4.5 V				130	Ω	5

Notes 1: P0_6, P0_7, P1_5, P2_3, P2_4 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P1_1–P1_4 have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. P2_0–P2_2 have the hysteresis when these pins are used as serial I/O pins.

2: Connect 0.1µF or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise. Also connect 0.1µF or more capacitor externally between the pins V_{CC}–CNV_{SS}.

3: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

4: Pin names in each parameter is described as bellow.
(1) Dedicated pin: dedicated pin names.
(2) Double-/triple-function ports
• When the same limits: I/O port name.
• When the limits of functions except ports are different from I/O port limits: function pin name.

I²C Bus Table

SLAVE ADDRESS= BAH(WRITE), BBH(READ)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	1/0

WRITE TABLE(input bytes)

SUB ADDRESS		DATA								
HEX	BIN	D7	D6	D5	D4	D3	D2	D1	D0	INITIAL
		(not asigned)					Power Down Mode		H Stop	
00H	00000000	0	0	0	0	0	0	1	0	02H
		X-ray Enable	YUV input	Y/C input	EXT input	TV input	Y/C through	(for evaluation)		
01H	00000001	0	0	0	0	1	0	0	0	08H
		Ped Clamp	(not asigned)		VRT Voltage		Sync-tip Clamp			
02H	00000010	0	0	0	0	1	0	0	0	08H
		Sharpness Delay (Front)		Shrapness Gain (Front)						
04H	00000100	V1	V0	V1	V0	V0	V0	V0	V0	A0H
		Sharpness Delay (Rear)		Shrapness Gain (Rear)						
05H	00000101	V1	V0	V1	V0	V0	V0	V0	V0	A0H
		(not asigned)	Y DL Time Adj.		YNR SW	YNR Limitter Level				
06H	00000110	V0	V0	V0	V0	V0	V0	V0	V0	00H
		(not asigned)		Sharpness Limitter Level						
07H	00000111	V0	V0	V0	V1	V0	V1	V0	V1	15H
		(not asigned)	Tint Control							
08H	00001000	V0	V0	V1	V0	V1	V0	V0	V1	29H
		(not asigned)	Color Control							
09H	00001001	V0	V0	V1	V0	V1	V0	V0	V0	28H
		(not asigned)	Contrast Control							
0AH	00001010	V0	V0	V1	V1	V1	V0	V1	V1	3BH
		Half Tone		OSD Level (R)						
0BH	00001011	V0	V0	V0	V1	V1	V1	V1	V0	1EH
		RGB Matrix Ratio		OSD Level (G)						
0CH	00001100	V1	V0	V0	V1	V1	V1	V1	V0	5EH
		OSD Comp		OSD Level (B)						
0DH	00001101	V0	V0	V0	V1	V1	V1	V1	V0	0EH
		Brightness Control								
0EH	00001110	V1	V0	V0	V0	V0	V0	V0	V0	80H
		(not asigned)	H Free	AFC1 Gain	H Phase Control					
0FH	00001111	0	0	0	0	1	0	0	0	08H
		(not asigned)		(for evaluation)	2D Y/C	(for evaluation)				
10H	00010000	0	0	0	0	0	0	0	0	00H
		(not asigned)	Black Stre. SW	(for evaluation)						
11H	00010001	V0	V1	V0	V0	V0	V0	V0	V0	40H
		RGB Mute	(inhibited)			Gamma Control				
12H	00010010	1	0	0	0	0	0	0	0	80H
		Service SW	V-Shift			(inhibited)	Hold Down Level			
13H	00010011	0	0	0	1	0	0	0	0	10H
		V-Blanking Stop	V-Ramp Size							
14H	00010100	0	1	0	0	0	0	0	0	40H
		V-Ramp Invert	V-Ramp Linearity							
15H	00010101	1	1	1	1	1	1	1	1	FFH
		Cut Off (R)								
16H	00010110	V0	V0	V0	V0	V0	V0	V0	V0	00H
		CutOff(R) MSB	Drive (R)							
17H	00010111	V0	V0	V0	V0	V0	V0	V0	V0	00H
		Cut Off (G)								
18H	00011000	V0	V0	V0	V0	V0	V0	V0	V0	00H
		CutOff(G) MSB	Drive (G)							
19H	00011001	V0	V0	V0	V0	V0	V0	V0	V0	00H
		Cut Off (B)								
1AH	00011010	V0	V0	V0	V0	V0	V0	V0	V0	00H
		CutOff(B) MSB	Drive (B)							
1BH	00011011	V0	V0	V0	V0	V0	V0	V0	V0	00H
		(not asigned)				Intelligent Monitor (Analog)				
1CH	00011100	0	0	0	0	0	0	0	0	00H
		(not asigned)		I/M(D) Enable	Intelligent Monitor (Digital)					
1DH	00011101	0	0	0	0	0	0	0	0	00H
		H VCO Adjust								
51H	01010001	0	0	0	0	0	0	0	0	00H

NOTE: V0 / V1 ==> V- LATCH BIT

READ TABLE(output bytes)

SUB ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
60H	01100000	KILLER	H COINCI	V COINCI	B_W	IIC_STILL	MV_180	DET NZ	K_MONI
61H	01100001	B2 ROM							
62H	01100010	B2 ROM MSB	(not asigned)					C Gain	
63H	01100011	BLKDETV				(not asigned)			

Bus function

WRITE

FUNCTION	BIT	SUB ADD	DATA	DISCRIPTION	INITIAL	NOTE
H STOP	1	00H	D0	Horizontal output switch (0: H OUT, 1: H STOP)	0	
Power Down	2	00H	D1-D2	Power down mode control (0: normal, 1: PD0, 2: PD1, 3: PD2)	01	
Input Video SW	4	01H	D3-D6	Video SW Selector (1: TV, 2: EXT, 4: Y/C input, 9: YUV input)	0001	
X-ray Enable	1	01H	D7	X-ray protect function switch (0: X-ray Protect OFF, 1: X-ray Protect ON)	0	
Y/C through	1	01H	D2	Y/C separation input switch (0: Y/C Sep ON, 1: Y/C Sep. through)	0	
Sync-tip Clamp	3	02H	D0-D2	Sync-tip clamp switch (0: Clamp ON, 1: TV clamp OFF, 2: EXT clamp OFF, 4: Y clamp OFF)	000	
Ped Clamp	1	02H	D7	Pedestal clamp switch (0: Pedestal clamp OFF, 1: Pedestal clamp ON)	0	
VRT Voltage	2	02H	D3-D4	Reference voltage adjustment for A/D	01	
Sharpness Gain (Front)	6	04H	D0-D5	Over-shoot gain control by 6bit	100000	V Latch
Sharpness Delay (Front)	2	04H	D6-D7	Over-shoot width control (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns)	10	V Latch
Sharpness Gain (Rear)	6	05H	D0-D5	Pre-shoot gain control by 6bit	100000	V Latch
Sharpness Delay (Rear)	2	05H	D6-D7	Pre-shoot width control (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns)	10	V Latch
YNR SW	7	06H	D4	YNR control switch (0: YNR OFF, 1: YNR ON)	0	V Latch
YNR Limiter Level	1	06H	D0-D3	YNR limiter level control	0000	V Latch
Y DL Time Adj.	2	06H	D5-D6	Delay time adjustment of luminance signal (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns)	00	V Latch
Sharpness Limiter Level	6	07H	D0-D5	Maximum level control of sharpness	010101	V Latch
Tint Control	7	08H	D0-D6	Tint Control by 7bit	0101001	V Latch
Color Control	7	09H	D0-D6	Color Saturation control by 7bit	0101000	V Latch
Contrast Control	7	0AH	D0-D6	Contrast control by 7bit	0111011	V Latch
OSD Level (R)	6	0BH	D0-D5	Digital OSD (R) level adjustment by 6bit	011110	V Latch
Half Tone	2	0BH	D6-D7	Setting of Half Tone mode	00	V Latch
OSD Level (G)	6	0CH	D0-D5	Digital OSD (G) level adjustment by 6bit	011110	V Latch
RGB Matrix Ratio	2	0CH	D6-D7	RGB Matrix ratio control	10	V Latch
OSD Level (B)	6	0DH	D0-D5	Digital OSD (B) level adjustment by 6bit	011110	V Latch
OSD Comp	2	0DH	D6-D7	Digital OSD threshold voltage control of input signal	00	V Latch
Brightness Control	8	0EH	D0-D7	Brightness control by 8bit	10000000	V Latch
AFC2 H Phase	5	0FH	D0-D4	Horizontal phase adjustment by 5bit	01000	
AFC1 Gain	1	0FH	D5	Horizontal AFC gain switch (0: Low, 1: High)	0	
H-free	1	0FH	D6	Horizontal forced free-running mode switch (0: OFF, 1: Forced Free-running)	0	
2D Y/C	1	10H	D4	Y/C separation mode switch (0: Y/C Sep ON, 1: Y/C Sep. through)	0	
Black Stretch SW	1	11H	D6	Black Stretch function ON/OFF switch (0: OFF, 1: ON)	0	
Gamma Control	1	12H	D0-D3	RGB gamma threshold control (0:Gamma OFF)	0000	
RGB Mute	1	12H	D7	RGB signal mute ON/OFF switch (0: Mute 1: RGB output)	1	
Hold Down Level	3	13H	D0-D2	Hold Down level adjustment by 3bit	000	
V Shift	3	13H	D4-D6	V RAMP start timing adjustment 2Line/Step	001	
Service SW	1	13H	D3	Service mode switch (0: Vertical output ON, 1: Vertical output OFF)	0	
V-Ramp Size	7	14H	D0-D6	V-Ramp amplitude adjustment by 7bit	1000000	
Test	1	14H	D7	No use for customer (Test mode)	0	
V-Ramp Linearity	7	15H	D0-D6	V-Ramp linearity adjustment by 7bit	1111111	
V-Ramp Invert	1	15H	D7	V-Ramp polarity switch	1	
Cut Off(R)	9	16H	D0-D7	R OUT pedestal level adjustment by 9bit	00000000	V Latch
		17H	D7		0	
Drive(R)	7	17H	D0-D6	R OUT amplitude adjustment by 7bit	0000000	V Latch
Cut Off(G)	9	18H	D0-D7	G OUT pedestal level adjustment by 9bit	00000000	V Latch
		19H	D7		0	
Drive(G)	7	19H	D0-D6	G OUT amplitude adjustment by 7bit	0000000	V Latch
Cut Off(B)	9	1AH	D0-D7	B OUT pedestal level adjustment by 9bit	00000000	V Latch
		1BH	D7		0	
Drive(B)	7	1BH	D0-D6	B OUT amplitude adjustment by 7bit	0000000	V Latch
Intelligent Monitor (Analog)	4	1CH	D0-D3	Intelligent Monitor (Analog) mode selector	0000	
Intelligent Monitor (Digital)	5	1DH	D0-D4	Intelligent Monitor (Digital) mode selector	00000	
Intelligent Monitor(D) Enable	1	1DH	D5	Intelligent Monitor (Digital) function switch (0: OFF, 1: ON)	0	
H VCO Adj.	8	51H	D0-D7	H VCO free-running frequency adjustment by 8bit	00000000	

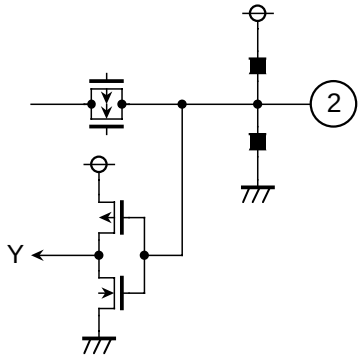
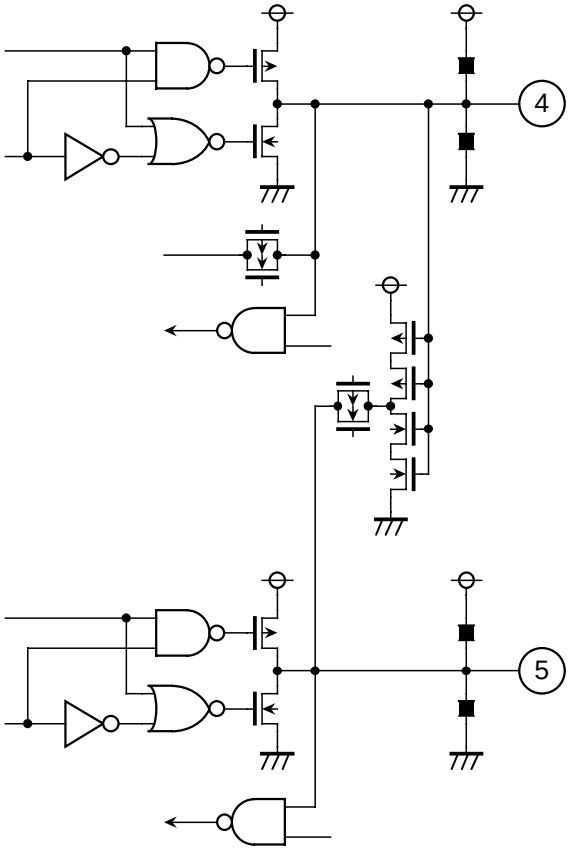
Read

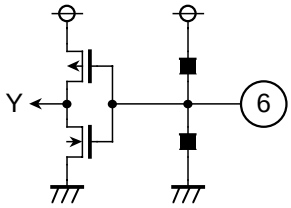
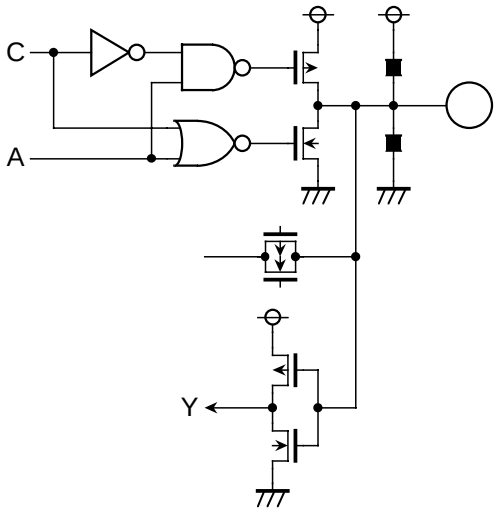
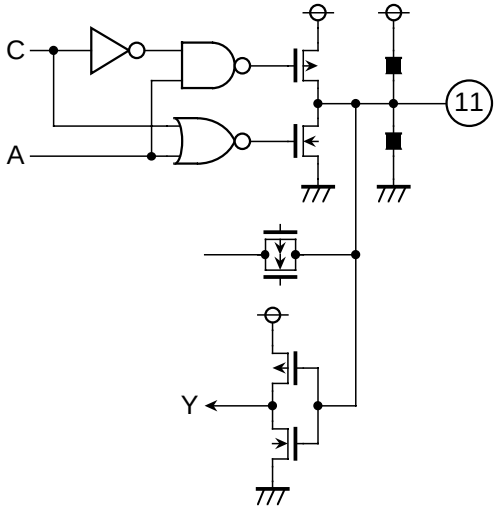
K_MONI	1	60H	D0	C-processor Killer det. output (1: C-pro Killer ON)
DET_NZ	1	60H	D1	Noise Killer det. output (1: Noise Killer ON)
MV_180	1	60H	D2	Reversed Burst signal (all reversed) det. output (1: Reversed Burst)
IIC_STILL	1	60H	D3	VCR Still mode det. output (1: Still mode)
B_W	1	60H	D4	PLL Killer (Chroma) det. output (1: PLL Killer ON)
V COINCI	1	60H	D5	Vertical Coincidence det. output (1: V Coincident)
H COINCI	1	60H	D6	Horizontal Coincidence det. output (1: H Coincident)
KILLER	1	60H	D7	Color/Killer condition (1: color output, 0: Killer (color off))
B2ROM	9	61H	D0-D7	B2ROM output
		62H	D7	
C Gain	2	62H	D0-D1	ACC amplifier status
BLKDETV	4	63H	D4-D7	Black det. output of Black Stretch circuit

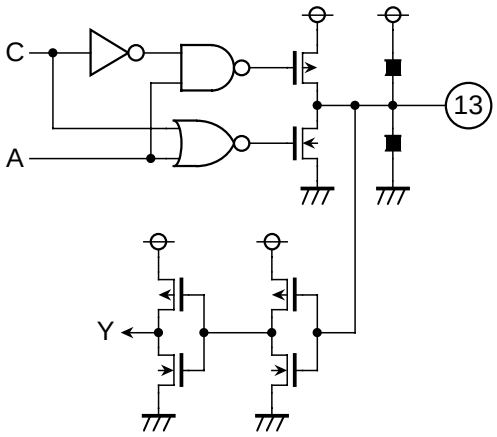
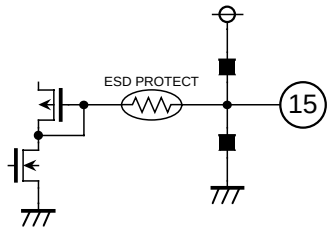
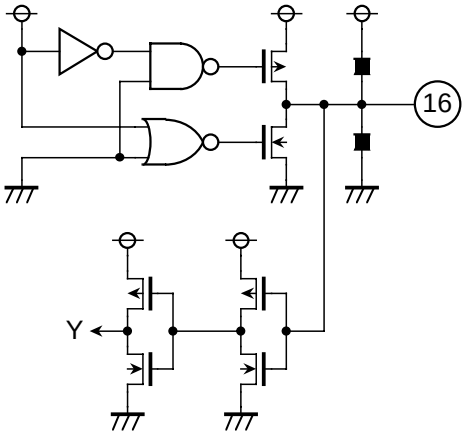
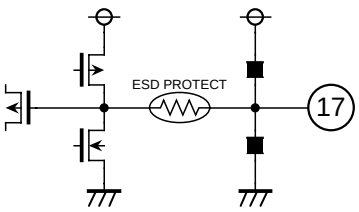
M65580MAP I^2C bus Standard data

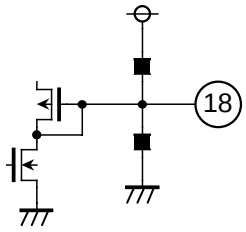
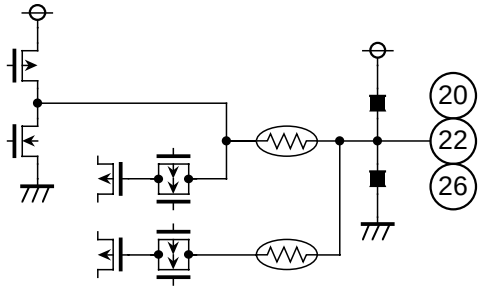
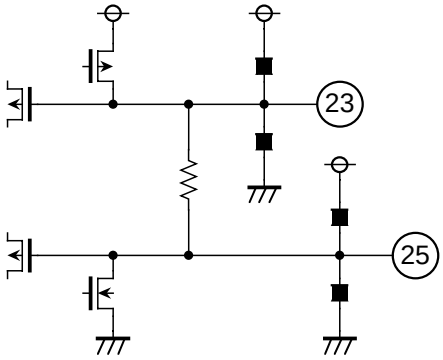
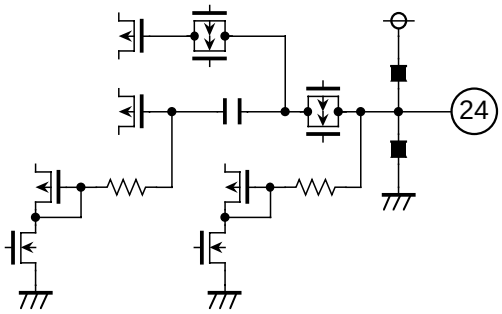
Sub address	data	Sub address	data	Sub address	data
00h	00	30h	20	50h	00
01h	08	31h	05	51h	00
02h	08	32h	04	52h	00
03h	21	33h	81	53h	35
04h	C0	34h	8D	54h	22
05h	C0	35h	63	55h	94
06h	00	36h	79	56h	14
07h	15	37h	50	57h	A6
08h	40	38h	55	58h	00
09h	40	39h	25	59h	A6
0Ah	40	3Ah	21	5Ah	00
0Bh	1E	3Bh	19	5Bh	00
0Ch	9E	3Ch	B3	5Ch	00
0Dh	1E	3Dh	0F	5Dh	80
0Eh	80	3Eh	06		
0Fh	10	3Fh	08		
10h	10	40h	00		
11h	4A	41h	01		
12h	8D	42h	C0		
13h	00	43h	04		
14h	40	44h	64		
15h	40	45h	3D		
16h	00	46h	15		
17h	C0	47h	00		
18h	00	48h	83		
19h	C0	49h	00		
1Ah	00	4Ah	A0		
1Bh	C0	4Bh	00		
1Ch	00	4Ch	15		
1Dh	00	4Dh	01		
		4Eh	6E		
		4Fh	38		

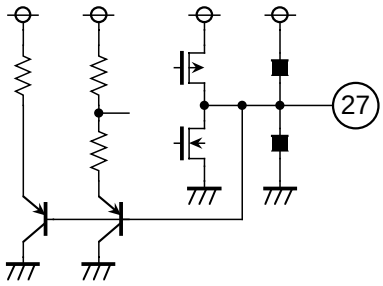
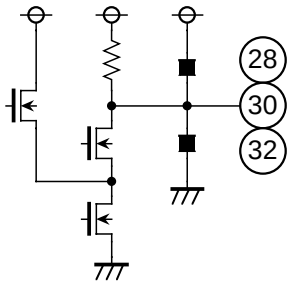
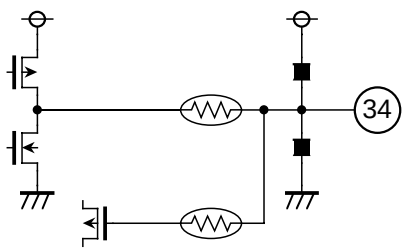
DESCRIPTION OF PIN

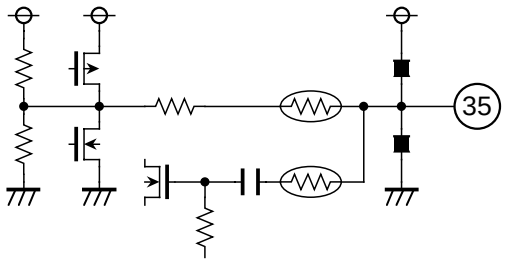
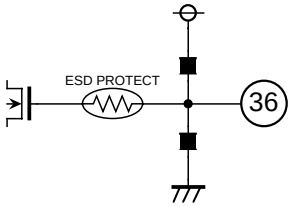
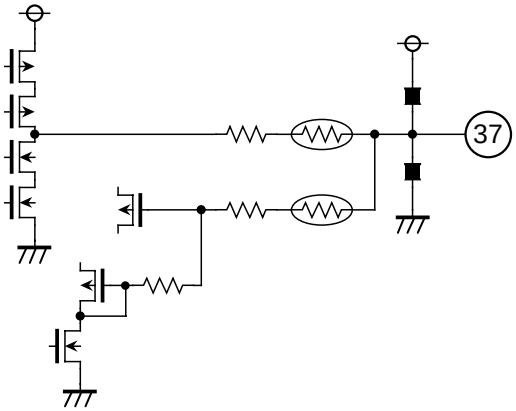
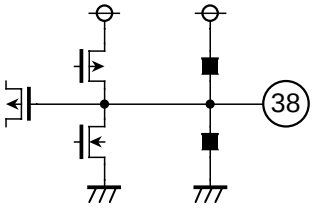
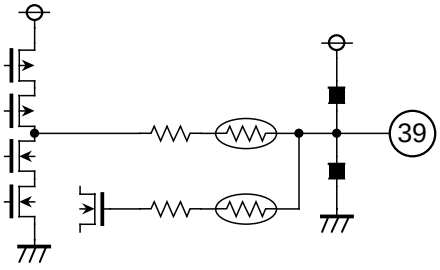
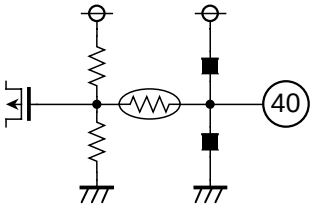
Pin No.	Name	Peripheral circuit of pins	Note
1	Vss (MCU)		Power source for MCU. 0V
2	FILT		
3	Vcc (MCU)		Power source for MCU. 5.0V ± 5%
4 5	P27/XCOUT P26/FSCIN/ XCIN		

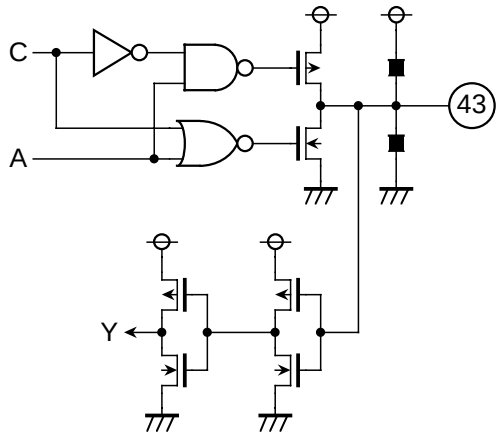
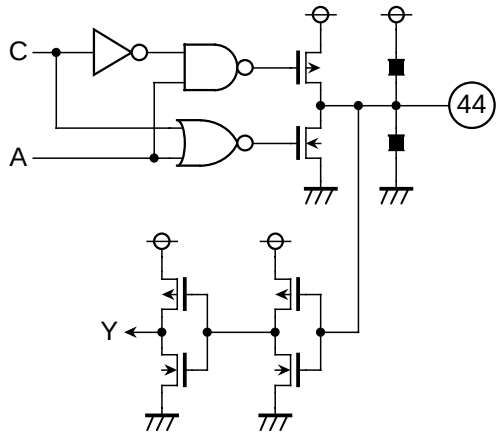
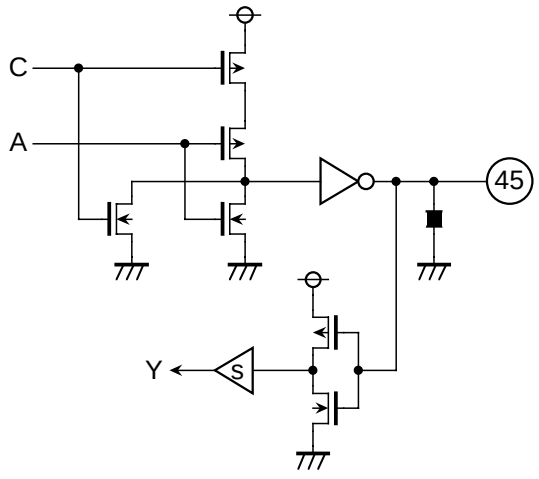
Pin No.	Name	Peripheral circuit of pins	Note
6	RESETB		CMOS INPUT (Impedance>100kΩ) V_{OL} = 0V : Reset state V_{OH} = 5V : Release from Reset state
7 8 9 10	P2$_2$/SIN/AD8 P2$_1$/SOUT/AD8 P2$_0$/SCLK/AD6 P1$_5$/AD1/ INT3/FSCIN		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance≈250Ω (output))
11	P1$_6$/AD2/TIM2		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance≈250Ω (output)) Intelligent monitor output (Analog/Digital)
12	Vss (Digital)	———————	0V

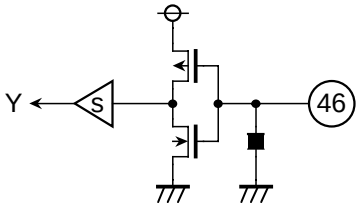
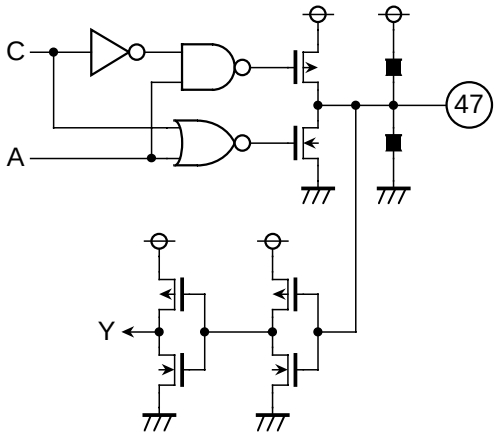
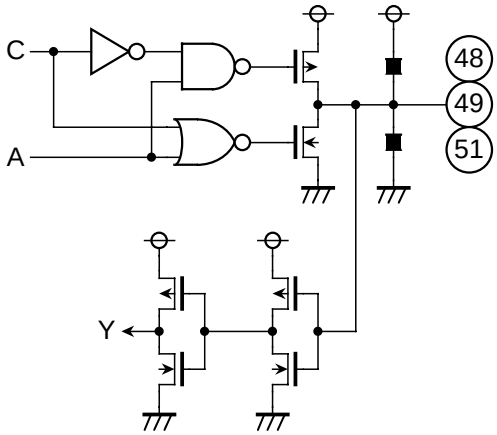
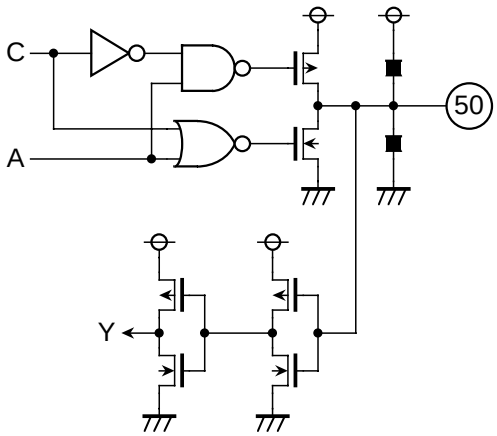
Pin No.	Name	Peripheral circuit of pins	Note
13	OSD CLK		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))
14	Vdd (Digital)	———	Power source for Digital block. 5.0V ± 5%
15	CLK OUT		Impedance≈400Ω
16	RESET		CMOS INPUT (Impedance>100kΩ) V_{IL} = 0V : Reset state V_{IH} = 5V : Release from Reset state
17	C.Sync IN		Sync Sep. input Impedance=N.A. DC 2.5V

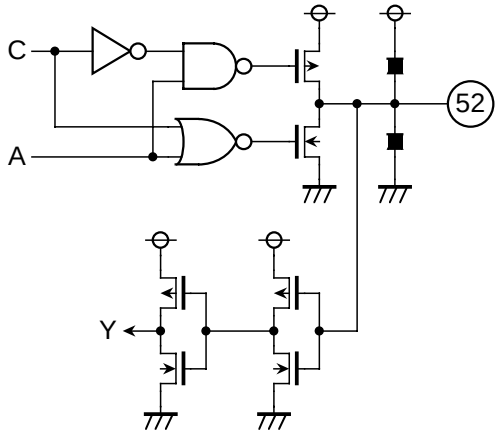
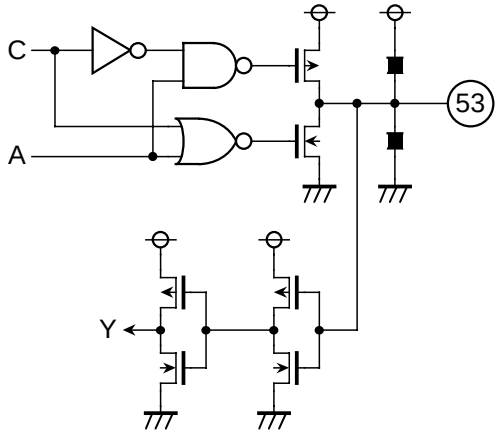
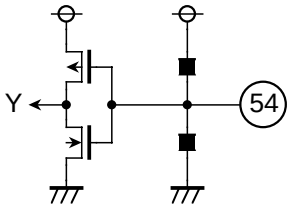
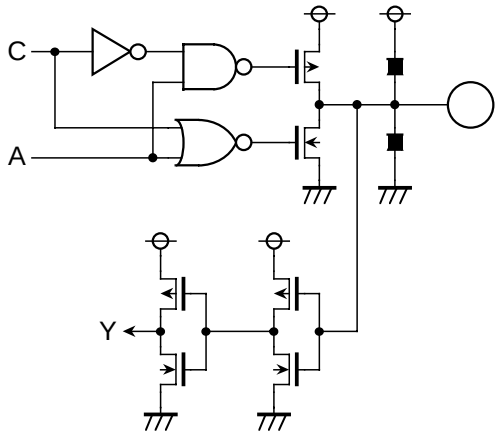
Pin No.	Name	Peripheral circuit of pins	Note
18	CVBS OUT		Impedance≈150Ω DC : 0.55V (sync) AC : 1.75V_{p-p} (typ.)
19	Vdd (Input)	———	Power source for A/D etc. 3.3V ± 5%
20 22 26	EXT(CVBS) IN Y IN TV(CVBS) IN		Impedance=N.A. DC : 0.5V (sync) AC : 1.0V_{p-p} (typ.)
21	Vss (Input)	———	Power source for A/D etc. 0V
23 25	VRT VRB		Impedance>50Ω DC : 1.7V (VRT) 0.5V (VRB)
24	C IN		Impedance≈7.5kΩ DC : 1.0V AC : 0.286V_{p-p} (burst)

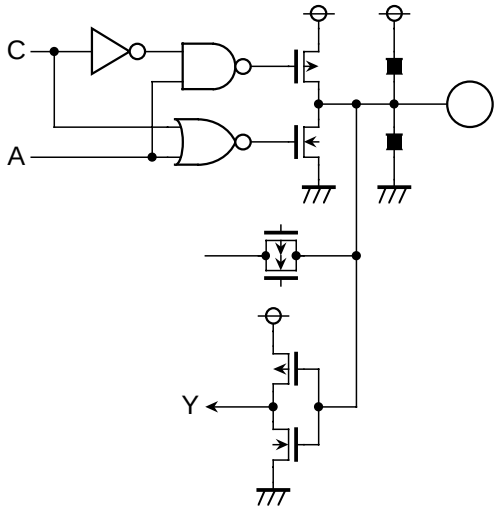
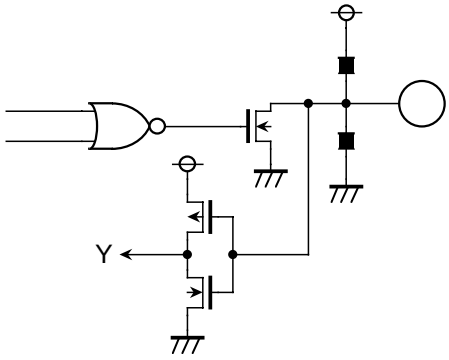
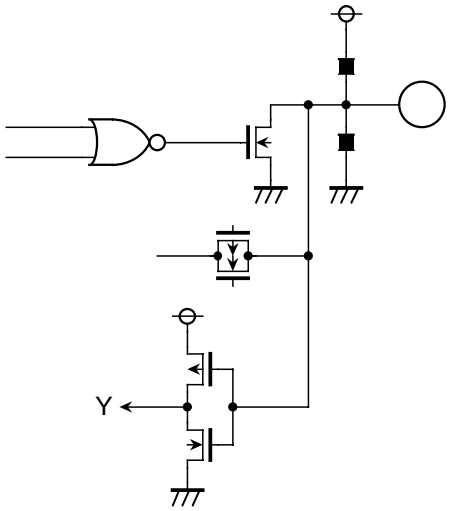
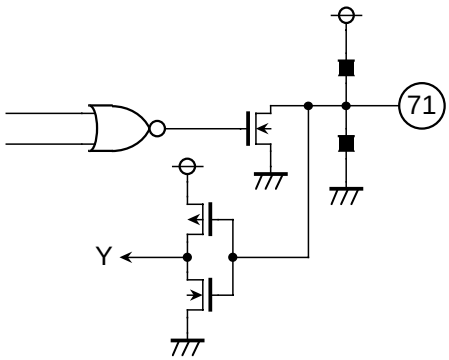
Pin No.	Name	Peripheral circuit of pins	Note
27	VZ OUT		Impedance≈400Ω DC : 2.05V
28 30 32	R OUT G OUT B OUT		Impedance≈1kΩ DC : 3V (blanking)
29	Vdd (Output)	———	Power source for D/A etc. 3.3V ± 5%
31	Vss (Output)	———	Power source for D/A etc. 0V
33	Vdd (VCXO)	———	Power source for VCXO etc. 5.0V ± 5%
34	APC Filter		Impedance=N.A. (Additional filter on PCB board) DC 2.9V

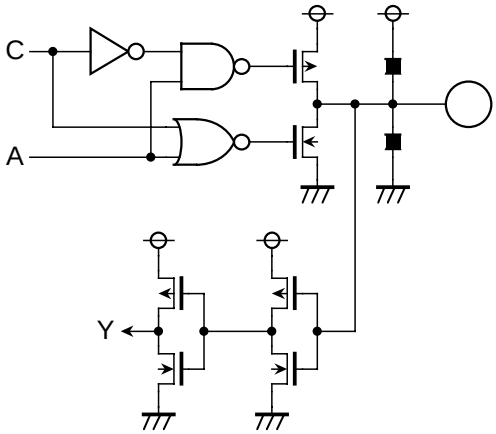
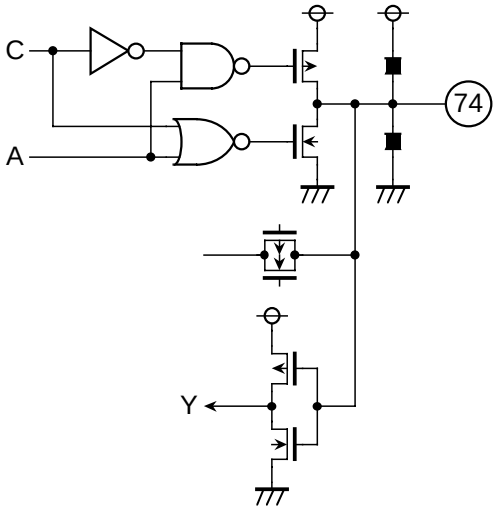
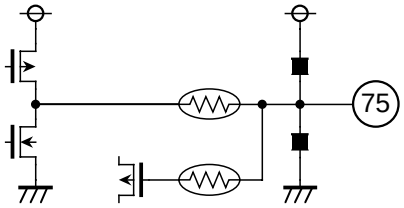
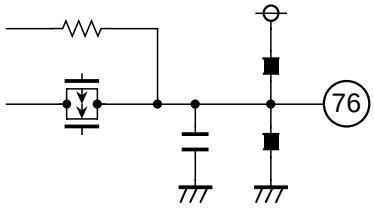
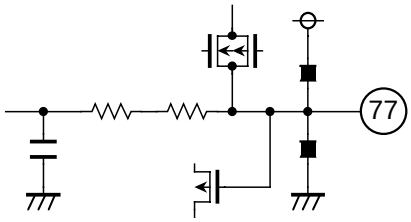
Pin No.	Name	Peripheral circuit of pins	Note
35	X'tal		Impedance≈1kΩ
36	X-ray Protector		Impedance>100kΩ 0.0-3.0 : Normal 3.2-3.3 : Hold down 3.7-5.0 : Shut down
37	AFC1 Filter		Impedance=N.A. (Additional filter on PCB board) DC 2.5V
38	V RAMP OUT		Impedance≈400Ω 2.5$V_{p\text{-}p}$ (typ.)
39	HVCO F/B		Impedance=N.A. (Additional filter on PCB board) DC 3.0V
40	Neck Protector		Impedance≈5kΩ 0.0-1.0 : RGB off 1.6-3.0 : Normal 4.0-5.0 : Test mode

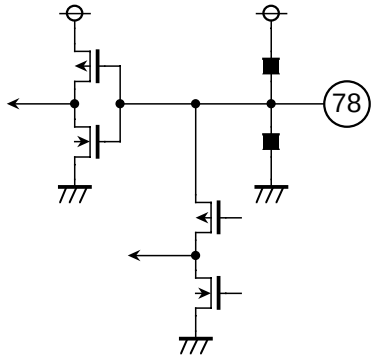
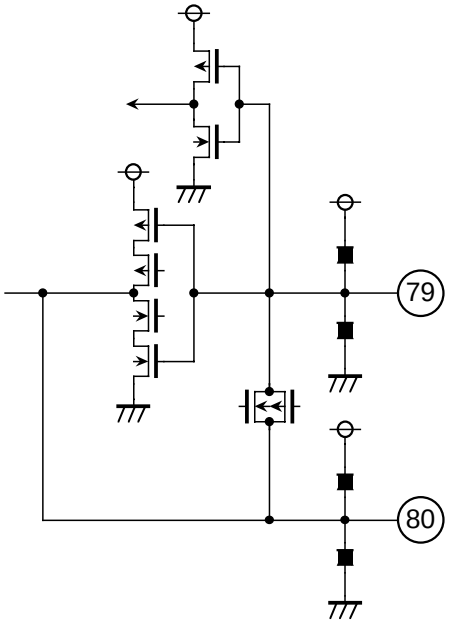
Pin No.	Name	Peripheral circuit of pins	Note
41	Vss (DEF)	———	Power source for Deflection block. 0V
42	Vdd (DEF)	———	Power source for Deflection block. 5.0V ± 5%
43	FBP IN		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output) V_{IL} = 0V : RGB output V_{IH} = 5V : Blanking
44	H OUT		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output) V_{OL} : 0V V_{OH} : 5V
45	SDA		CMOS IN/OUT 2 (Impedance>100kΩ (input) Impedance<100Ω (output) V_{IL} : 0V V_{IH} : 5V

Pin No.	Name	Peripheral circuit of pins	Note
46	SCL		CMOS Schmitt IN (Impedance>100kΩ) V_{IL} : 0V V_{IH} : 5V
47	Half Tone IN		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output) V_{IL} = 0V : RGB output V_{IH} = 5V : Half tone on
48 49 51	OSD(B) IN OSD(G) IN OSD(R) IN		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output) V_{IL} : 0V V_{IH} : 5V
50	Fast BLK IN		CMOS IN/OUT 1 Impedance>100kΩ (input) Impedance<100Ω (output) V_{IL} = 0V : RGB output V_{IH} = 5V : OSD output

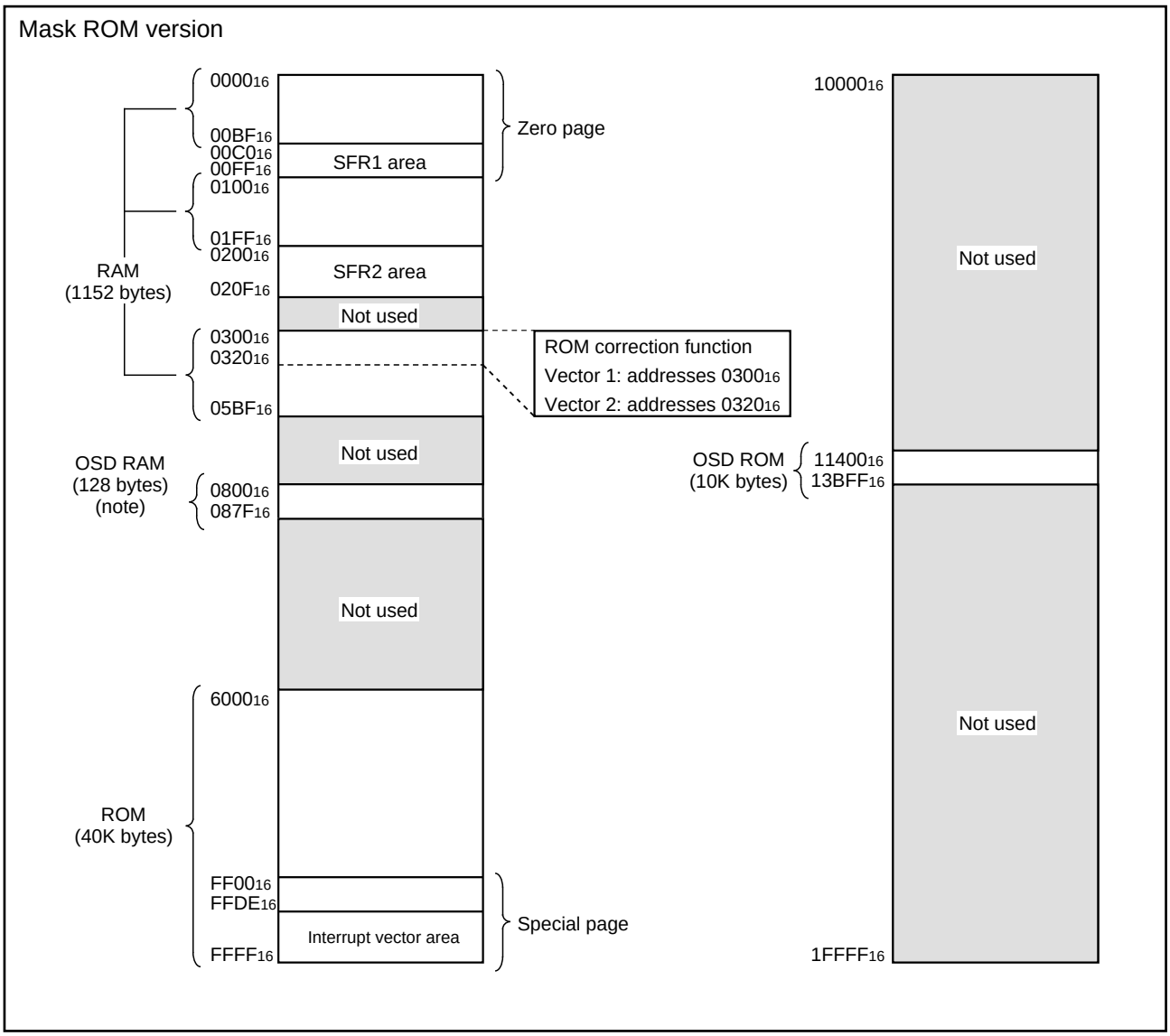
Pin No.	Name	Peripheral circuit of pins	Note
52	V sync OUT		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output)) VOL : 0V VOH : 5V
53	H sync OUT		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output)) VOL : 0V VOH : 5V
54	P5$_1$/VSYNC		CMOS INPUT (Impedance>100kΩ)
55 56 57 58 59	P5$_2$/R P5$_3$/OUT1 P3$_0$/G P3$_1$/B P1$_0$/OUT2		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))

Pin No.	Name	Peripheral circuit of pins	Note
60 61 62 63	P1$_1$/SCL1 P1$_2$/SCL2 P1$_3$/SDA1 P1$_4$/SDA2		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance≈250Ω (output))
64 65 66 67 68	P0$_0$/PWM0 P0$_1$/PWM1 P0$_2$/PWM2 P0$_3$/PWM3 P0$_4$/PWM4		CMOS IN/OUT (Impedance>100kΩ (input) Impedance≈250Ω (output))
69 70	P0$_5$/AD3 P0$_6$/INT2/AD4		CMOS IN/OUT (Impedance>100kΩ (input) Impedance≈250Ω (output))
71	P0$_7$/INT1		CMOS IN/OUT (Impedance>100kΩ (input) Impedance≈250Ω (output))

Pin No.	Name	Peripheral circuit of pins	Note
72 73	P2$_3$/TIM3 P2$_4$/TIM2		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))
74	P2$_5$/AD5		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance≈250Ω (output))
75	HLF		Impedance=N.A. (Additional filter on PCB board)
76	VHOLD		
77	CV IN		

Pin No.	Name	Peripheral circuit of pins	Note
78	CN VSS		CMOS IN/OUT (Impedance>100kΩ (input) Impedance≈250Ω (output))
79 80	X IN X OUT		

MEMORY MAP


Mask ROM version
0000₁₆
00BF₁₆
00C0₁₆
00FF₁₆
0100₁₆
01FF₁₆
0200₁₆
020F₁₆
0300₁₆
0320₁₆
05BF₁₆
0800₁₆
087F₁₆
6000₁₆
FF00₁₆
FFDE₁₆
FFFF₁₆
Zero page
SFR1 area
SFR2 area
Not used
ROM correction function
Vector 1: addresses 0300₁₆
Vector 2: addresses 0320₁₆
Not used
Not used
Interrupt vector area
Special page
RAM
(1152 bytes)
OSD RAM
(128 bytes)
(note)
ROM
(40K bytes)
10000₁₆
11400₁₆
13BFF₁₆
1FFFF₁₆
Not used
OSD ROM
(10K bytes)
Not used