Features

- **First-in First-out Dual Port Memory**
- **16384 bits x 9 Organization**
- **Fast Flag and Access Times: 15, 30 ns**
- **Wide Temperature Range: -55°C to +125°C**
- **Programmable Half Full Flag**
- **Fully Expandable by Word Width or Depth**
- **Asynchronous Read/Write Operations**
- **Empty, Full and Half Flags in Single Device Mode**
- **Retransmit Capability**
- **Bi-directional Applications**
- **Battery Back-up Operation: 2V Data Retention**
- **TTL Compatible**
- **Single 5V ± 10% Power Supply**
- **QML Q and V with SMD 5962-93177**

Description

The M672061F implements a first-in first-out algorithm, featuring asynchronous read/write operations. The FULL and EMPTY flags prevent data overflow and underflow. The Expansion logic allows unlimited expansion in word size and depth with no timing penalties. Twin address pointers automatically generate internal read and write addresses, and no external address information are required for the Atmel FIFOs. Address pointers are automatically incremented with the write pin and read pin. The 9 bits wide data are used in data communications applications where a parity bit for error checking is necessary. The Retransmit pin resets the Read pointer to zero without affecting the write pointer. This is very useful for retransmitting data when an error is detected in the system.

Using an array of eight transistors (8T) memory cell, the M672061F combines an extremely low standby supply current (typ = 0.1 µA) with a fast access time at 15 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 2 µW.

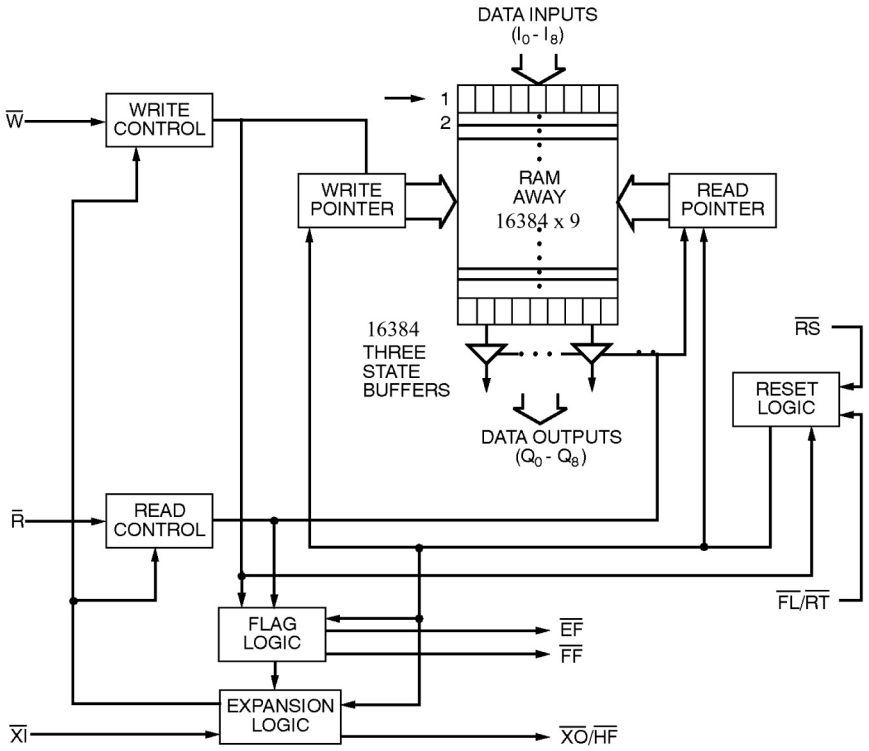
For military/space applications that demand superior levels of performance and reliability the M672061F is processed according to the methods of the latest revision of the MIL PRF 38535 (Q and V) or ESA SCC 9000.

Rad. Tolerant High Speed 16 Kb x 9 Parallel FIFO with Programmable Flag

M672061F

Rev. 4144F–AERO–06/02

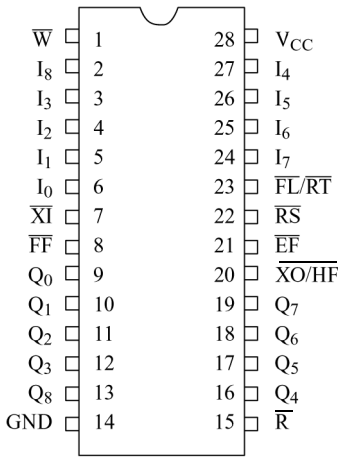
Block Diagram



Pin Configuration

DIL ceramic 28-pin 300 mils
FP 28-pin 400 mils

(top view)



Pin Description

Pin Name	Description
I0 - 8	Inputs
Q0 - 8	Outputs
W	Write Enable
R	Read Enable
RS	Reset
EF	Empty Flag
FF	Full Flag
XO/HF	Expansion Out/Half-Full Flag
XI	Expansion IN
FL/RT	First Load/Retransmit
VCC	Power Supply
GND	Ground

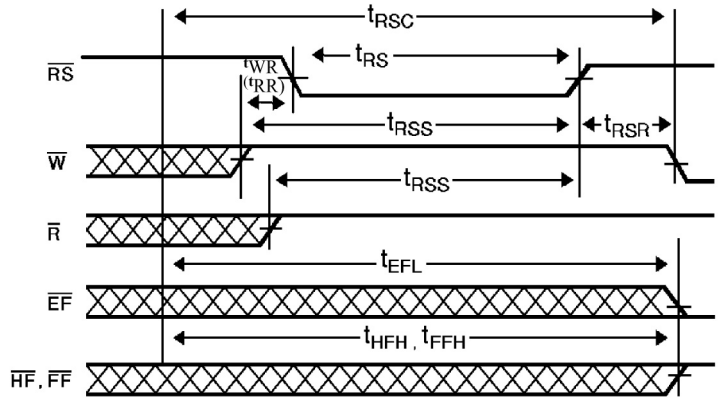
Data In (I_0 - I_8)

Data inputs for 9-bit data

Reset ($\overline{RS}$)

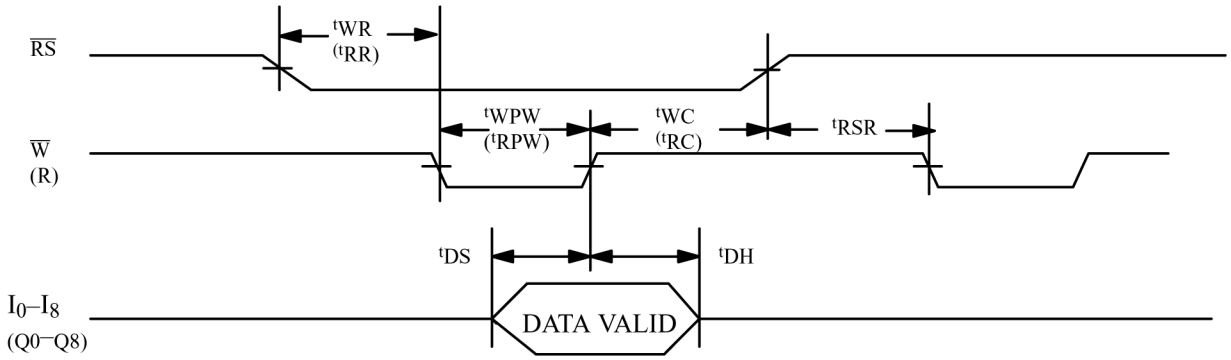
Reset occurs whenever the Reset ($\overline{RS}$) input is taken to a low state. Reset returns both internal read and write pointers to the first location. A reset is required after power-up before a write operation can be enabled. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the period shown in Figure 2 (i.e. t_{RSS} before the rising edge of RS) and should not change until tRSR after the rising edge of RS. Otherwise, pulse write (or read) low during the reset operation loads the Programmable Half Full Flag register from the data Inputs I0 - I8 (or data outputs Q0 - Q8) (shown in figure 2). In these two cases the Full Flag and the Programmable Half Full Flag are reseted to high and the Empty Flag to low.

Figure 1. Reset (no write to Programmable Half Full Flag register)



Notes: 1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of RS.

Figure 2. Reset (write (read) to Programmable Half Full Flag register)



Write Enable ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be maintained in the rise time of the leading edge of the Write Enable ($\overline{W}$). Data is stored sequentially in the Ram array, regardless of any current read operation.

Once half the memory is filled, and during the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and remain in this state until the difference between the write and read pointers is less than or equal to half of the total available memory in the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. On completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after TRFF, allowing a valid write to begin. When the FIFO stack is full, the internal write pointer is blocked from $\overline{W}$, so that external changes to $\overline{W}$ will have no effect on the full FIFO stack.

Read Enable ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided that the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a first in/first out basis, not including any current write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q0 - Q8) will return to a high impedance state until the next Read operation. When all the data in the FIFO stack has been read, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle, but inhibiting further read operations while the data outputs remain in a high impedance state. Once a valid write operation has been completed, the Empty Flag ($\overline{EF}$) will go high after tWEF and a valid read may then be initiated. When the FIFO stack is empty, the internal read pointer is blocked from $\overline{R}$, so that external changes to $\overline{R}$ will have no effect on the empty FIFO stack.

First Load/Retransmit (FL/RT)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is connected to ground to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by connecting the Expansion In ($\overline{XI}$) to ground.

The M672061F can be set to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read point to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. The retransmit feature is intended for use when a number of writes are equal to or less than the depth of the FIFO has occured since the last $\overline{RS}$ cycle. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), in accordance with the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is connected to GND to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain modes.

Full Flag ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 16384 writes.

Empty Flag ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations when the read pointer is equal to the write pointer, indicating that the device is empty.

Expansion Out/Half-full Flag (XO/HF)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is connected to ground, this output acts as an indication of a half-full memory.

The M672061F offers a variable offset for the Half Full condition. The offset is loaded into a register during a reset cycle. When $\overline{RS}$ is low, the Programmable Half Full Flag ($\overline{PHF}$) can be loaded from the DATA inputs I_0 - I_8 by pulsing $\overline{W}$ low or from the DATA outputs Q_0 - Q_8 by pulsing $\overline{R}$ low. The offset options are listed in table 1. If $\overline{PHF}$ is not loaded during the reset cycle, the default offset will be the half of the total memory of the device.

The Programmable Half-Full Flag ($\overline{PHF}$) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to the Programmable offset (if the Half Full Flag register has been loaded during the reset cycle) or the half of the total memory (if the Half Full register has not been loaded during the reset cycle).

After half the memory is filled and on the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last memory location.

Data Output (Q_0 - Q_8)

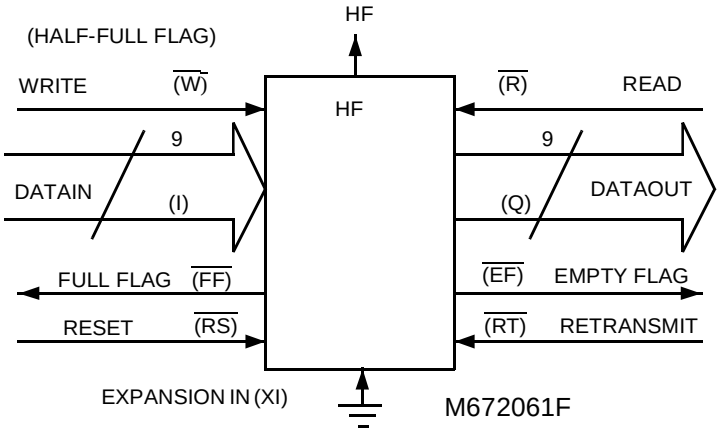
DATA output for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

Functional Description

Single Device Mode

A single M672061F may be used when the application requirements are for 16384 words or less. The M672061F is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 3). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

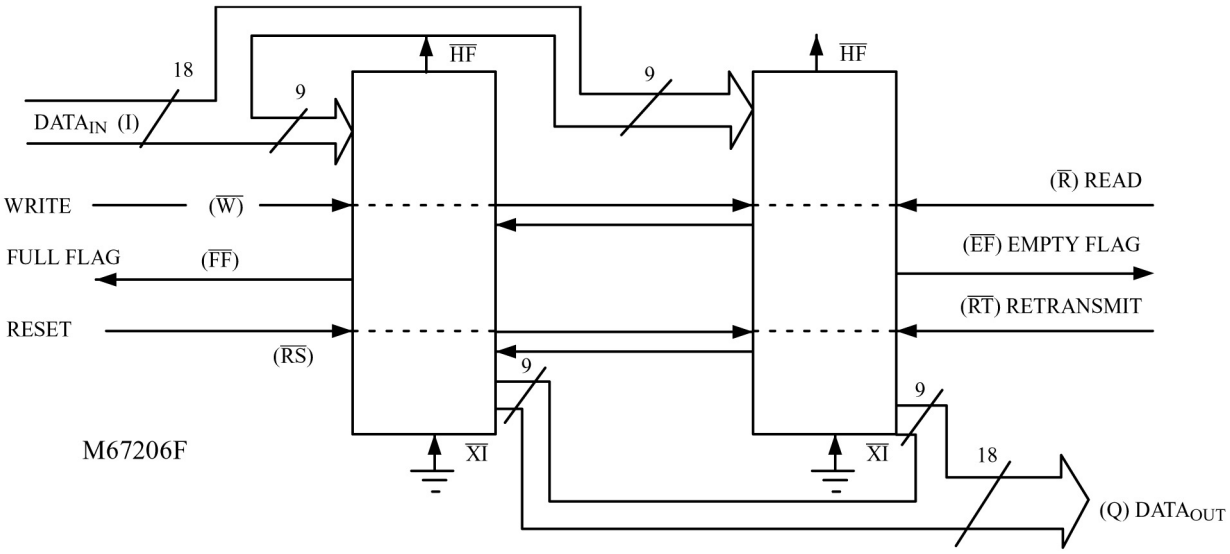
Figure 3. Block Diagram of Single 16384 × 9



Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any device. Figure 4 demonstrates an 18-bit word width by using two M672061F. Any word width can be attained by adding additional M672061F.

Figure 4. Block Diagram of 16384 bits x 18 FIFO Memory Used in Width Expansion Mode



Note: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Table 1. Programmable Half Full Flag Offset

I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Offset
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	32
0	0	0	0	0	0	0	1	0	64
...									
1	0	0	0	0	0	0	0	0	8192 (Half Full) Default Offset
...									
1	1	1	1	1	1	1	1	0	16384-64
1	1	1	1	1	1	1	1	1	16384-32

Table 2. Reset and Retransmit Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

Note: 1. Pointer will increment if flag is high.

Table 3. Reset and First Load Truth Table
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
See Figure 5.

Depth Expansion (Daisy Chain) Mode

The M672061F can be easily adapted for applications which require more than 16384 words. Figure 5 demonstrates Depth Expansion using three M672061F. Any depth can be achieved by adding additional 672061F.

The M672061F operates in the Depth Expansion configuration if the following conditions are met:

1. The first device must be designated by connecting the First Load ($\overline{FL}$) control input to ground.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be connected to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 5.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires that all $\overline{EF}$'s and all $\overline{FF}$s be ORed (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 5.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

Compound Expansion Module

It is quite simple to apply the two expansion techniques described above together to create large FIFO arrays (see Figure 6).

Bidirectional Mode

Applications which require data buffering between two systems (each system being capable of Read and Write operations) can be created by coupling M672061F as shown in Figure 7 Care must be taken to ensure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device on which $\overline{W}$ is in use; $\overline{EF}$ is monitored on the device on which $\overline{R}$ is in use). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow – Through Modes

Two types of flow-through modes are permitted: a read flow-through and a write flow-through mode. In the read flow-through mode (Figure 18) the FIFO stack allows a single word to be read after one word has been written to an empty FIFO stack. The data is enabled on the bus at (tWEF + tA) ns after the leading edge of $\overline{W}$ which is known as the first write edge and remains on the bus until the $\overline{R}$ line is raised from low to high, after which the bus will go into a three-state mode after tRHZ ns. The $\overline{EF}$ line will show a pulse indicating temporary reset and then will be set. In the interval in which $\overline{R}$ is low, more words may be written to the FIFO stack (the subsequent writes after the first write edge will reset the Empty Flag) ; however, the same word (written on the first write edge) presented to the output bus as the read pointer will not be incremented if $\overline{R}$ is low. On toggling $\overline{R}$, the remaining words written to the FIFO will appear on the output bus in accordance with the read cycle timings.

In the write flow-through mode (Figure 19), the FIFO stack allows a single word of data to be written immediately after a single word of data has been read from a full FIFO stack. The $\overline{R}$ line causes the $\overline{FF}$ to be reset, but the $\overline{W}$ line, being low, causes it to be set again in anticipation of a new data word. The new word is loaded into the FIFO stack on the leading edge of $\overline{W}$. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not set in order to write new data into the FIFO stack and to increment the write pointer.

Figure 5. Block Diagram of 49152 x 9 FIFO Memory (Depth Expansion)

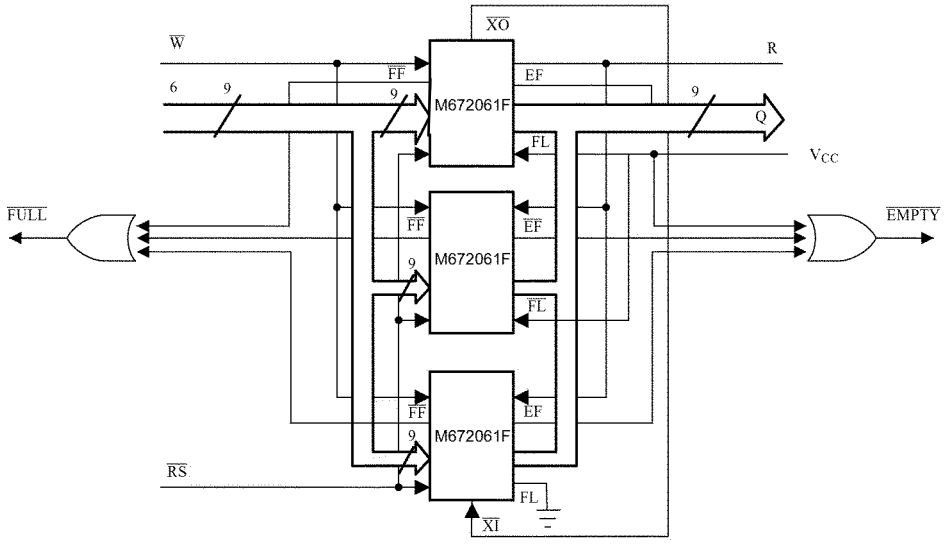
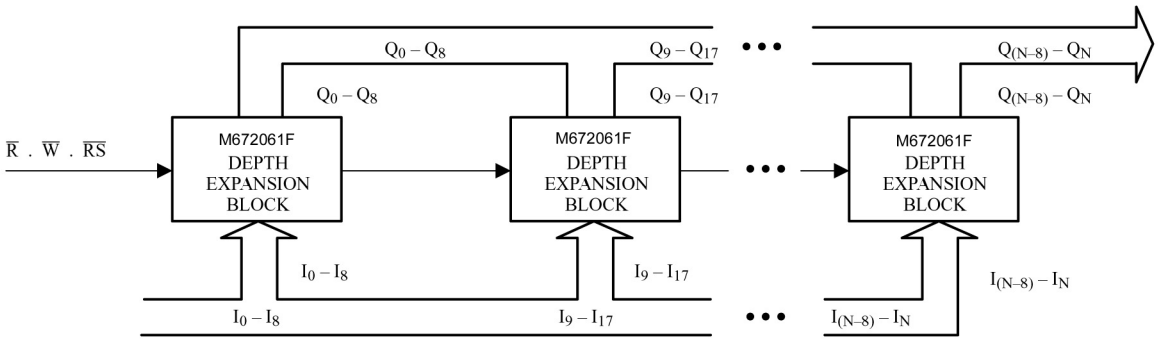
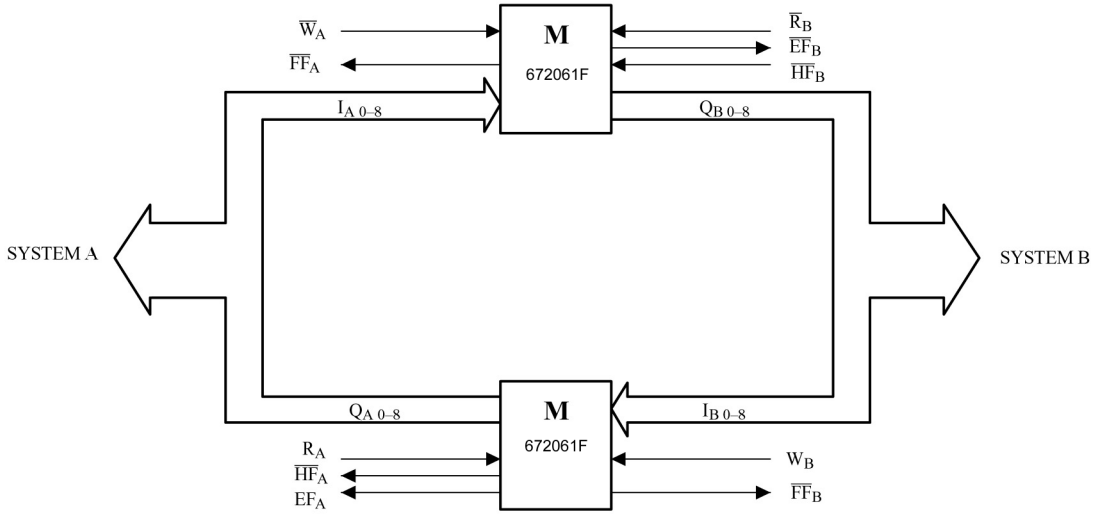


Figure 6. Compound FIFO Expansion



Notes: 1. For depth expansion block see section on Depth Expansion and Figure 4.
2. For Flag detection see section on Width Expansion and Figure 3

Figure 7. Bidirectional FIFO Mode



Electrical Characteristics

Absolute Maximum Ratings

Supply voltage (VCC - GND):	-0.5V to 7.0V
Input or Output voltage applied:	(GND -0.3V) to (Vcc +0.3V)
Storage temperature:	-65 °C to +150°C

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Parameters

Table 4. DC Test Conditions

TA = -55°C to +125°C; Vss = 0V; Vcc = 4.5V

Parameter	Description	M672061F-30	M672061F-15	Unit	Value
I_{CCOP} (1)	Operating supply current	110	120	mA	Max
I_{CCSB} (2)	Standby supply current	5	5	mA	Max
I_{CCPD} (3)	Power down current	400	400	µA	Max

Notes: 1. Icc measurements are made with outputs open.
2. $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = VIH.
3. All input = Vcc

Parameter	Description	M672061f	Unit	Value
ILI(1)	Input leakage current	± 1	µA	Max
ILO(2)	Output leakage current	± 1	µA	Max
VIL(3)	Input low voltage	0.8	V	Max
VIH(3)	Input high voltage	2.2	V	Min
VOL(4)	Output low voltage	0.4	V	Max
VOH(4)	Output high voltage	2.4	V	Min
C IN(5)	Input capacitance	8	pF	Max
C OUT(5)	Output capacitance	8	pF	Max

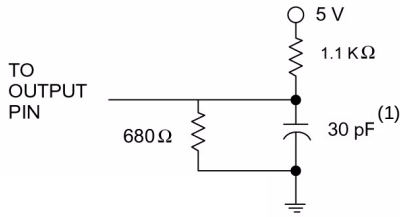
Notes: 1. 0.4 ≤ Vin ≤ Vcc.
2. $\overline{R}$ = VIH, 0.4 ≤ VOUT ≤ VCC.
3. VIH max = Vcc + 0.3V. VIL min = -0.3V or -1V pulse width 50 ns. For XI input, VIH= 2.8V
4. Vcc min, IOL = 8 mA, IOH = -2 mA
5. Guaranteed but not tested.

AC Parameters

AC Test Conditions

Input pulse levels: Gnd to 3.0V
Input rise/Fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure 8

Figure 8. Output Load



Note: 1. Includes jig and scope capacitance.

Table 5. AC Test Conditions

Symbol (1)	Symbol (2)	Parameter (3) (4)	M672061F- 30		M672061F- 15		Unit
			Min	Max	Min	Max	
Read Cycle							
TRLRL	tRC	Read cycle time	40	-	25	-	ns
TRLQV	tA	Access time	-	30	-	15	ns
TRHRL	tRR	Read recovery time	10	-	10	-	ns
TRLRH	tRPW	Read pulse width (5)	30	-	15	-	ns
TRLQX	tRLZ	Read low to data low Z (6)	5	-	0	-	ns
TWHQX	tWLZ	Write low to data low Z (6) (7)	5	-	3	-	ns
TRHQX	tDV	Data valid from read high	5	-	5	-	ns
TRHQZ	tRHZ	Read high to data high Z (6)	-	20	-	15	ns
Write Cycle							
TWLWL	tWC	Write cycle time	40	-	25	-	ns
TWLWH	tWPW	Write pulse width(5)	30	-	15	-	ns
TWHWL	tWR	Write recovery time	10	-	10	-	ns
TDVWH	tDS	Data set-up time	18	-	9	-	ns
TWHDX	tDH	Data hold time	0	-	0	-	ns
Reset Cycle							
TRSLWL	tRSC	Reset cycle time	40	-	25	-	ns
TRSLRSH	tRS	Reset pulse width (5)	30	-	15	-	ns
TWHRSH	tRSS	Reset set-up time	30	-	20	-	ns

Table 5. AC Test Conditions (Continued)

Symbol [1]	Symbol [2]	Parameter [3] [4]	M672061F- 30		M672061F- 15		Unit
			Min	Max	Min	Max	
TRSHWL	tRSR	Reset recovery time	10	–	10	–	ns
Retransmit Cycle							
TRTLWL	tRTC	Retransmit cycle time	40	–	25	–	ns
TRTLRTH	tRT	Retransmit pulse width[5]	30	–	15	–	ns
TWHRTH	tRTS	Retransmit set-up time[6]	30	–	15	–	ns
TRTHWL	tRTR	Retransmit recovery time	10	–	10	–	ns
Flags							
TRSLEFL	tEFL	Reset to EF low	–	30	–	25	ns
TRSLFFH	tHFH, tFFH	Reset to HF/FF high	–	30	–	25	ns
TRLEFL	tREF	Read low to EF low	–	30	–	15	ns
TRHFFH	tRFF	Read high to FF high	–	30	–	25	ns
TEFHRH	tRPE	Read width after EF high	30	–	15	–	ns
TWHEFH	tWEF	Write high to EF high	–	30	–	15	ns
TWLFFL	tWFF	Write low to FF low	–	30	–	20	ns
TWLHFL	tWHF	Write low to HF low	–	30	–	30	ns
TRHHFH	tRHF	Read high to HF high	–	30	–	30	ns
TFFHWH	tWPF	Write width after FF high	30	–	15	–	ns
Expansion							
TWLXOL	tXOL	Read/Write to XO low	–	30	–	15	ns
TWHXOH	tXOH	Read/Write to XO high	–	30	–	15	ns
TXILXIH	tXI	XI pulse width	30	–	15	–	ns
TXIHXIL	tXIR	XI recovery time	10	–	10	–	ns
TXILRL	tXIS	XI set-up time	10	–	10	–	ns

1. STD symbol.
2. ALT symbol.
3. Timings referenced as in ac test conditions.
4. All parameters tested only.
5. Pulse widths less than minimum value are not allowed.
6. Values guaranteed by design, not currently tested.
7. Only applies to read data flow-through mode.

Figure 9. Asynchronous Write and Read Operation

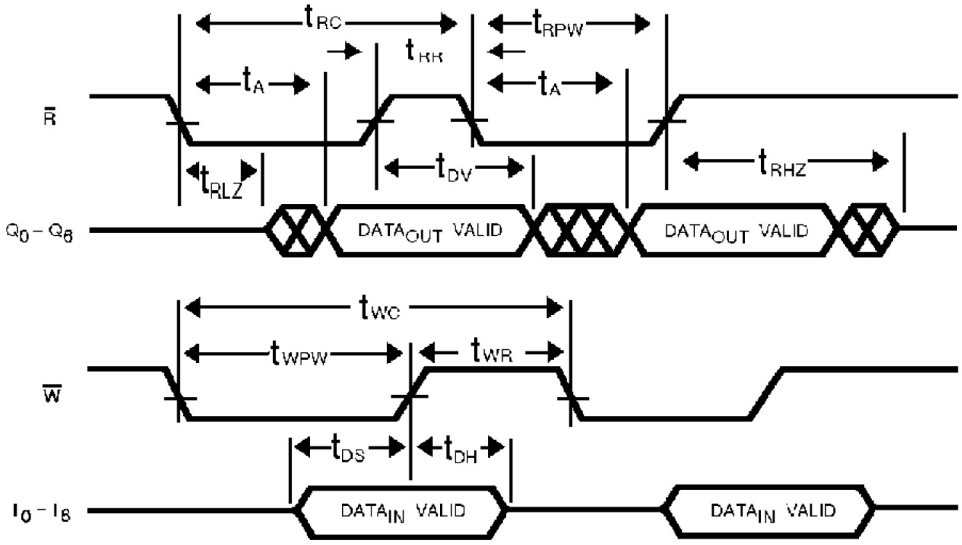


Figure 10. Full Flag from Last Write to First Read

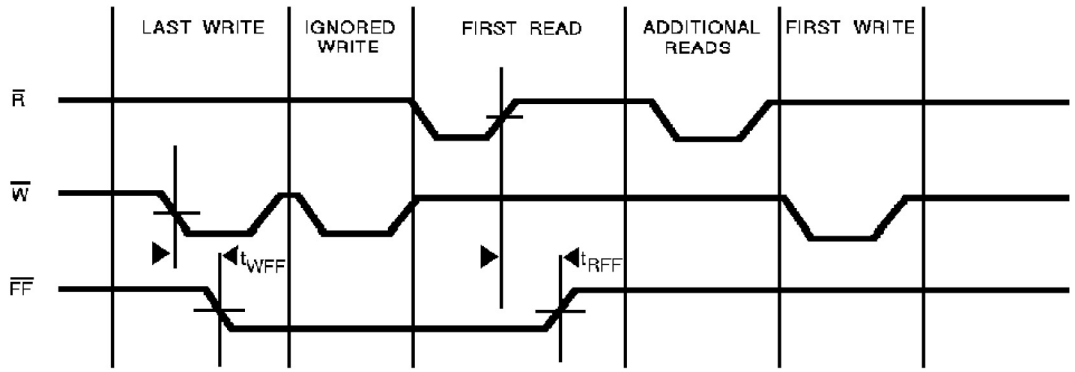


Figure 11. Empty Flag from Last Read to First Write

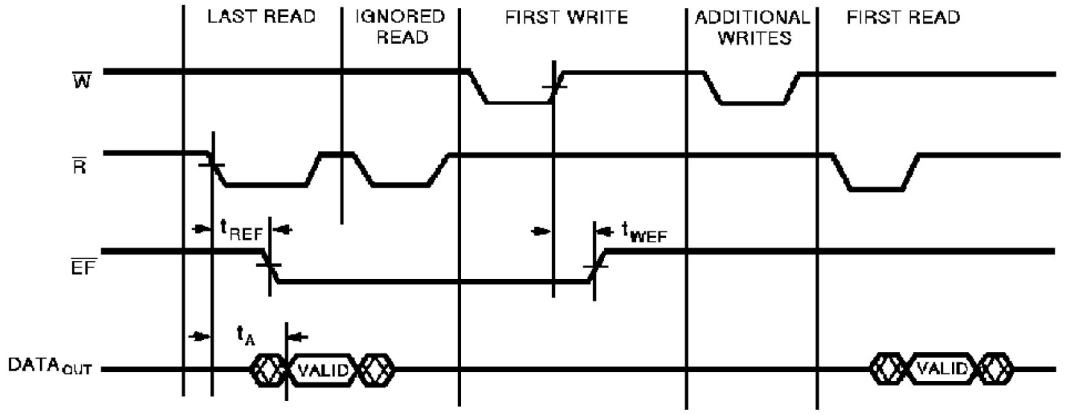
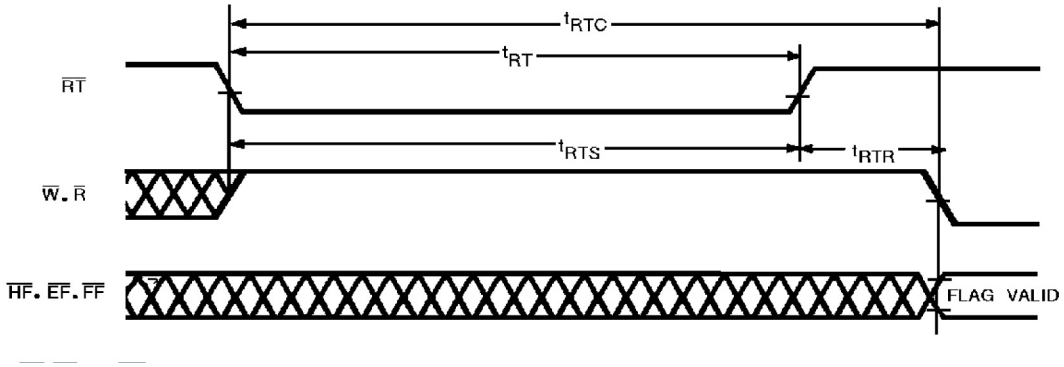


Figure 12. Retransmit



Note: 1. $\overline{EF}$, $\overline{FF}$ and $\overline{PHF}$ may change status during Retransmit, but flags will be valid at t_{RTC}

Figure 13. Empty Flag Timing

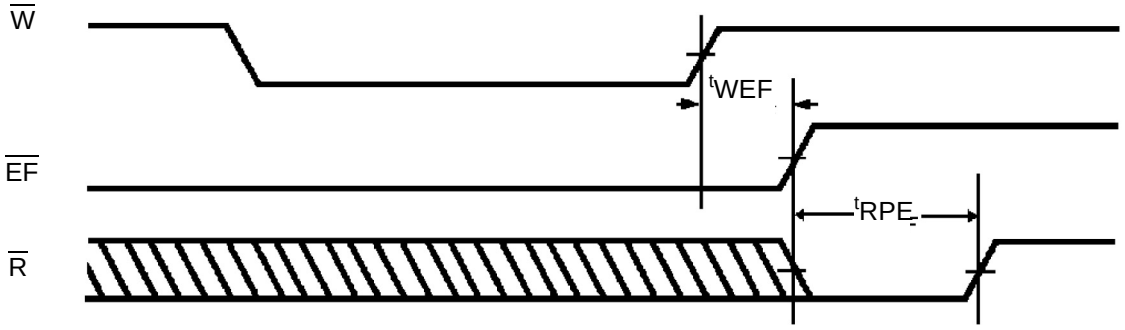


Figure 14. Full Flag Timing

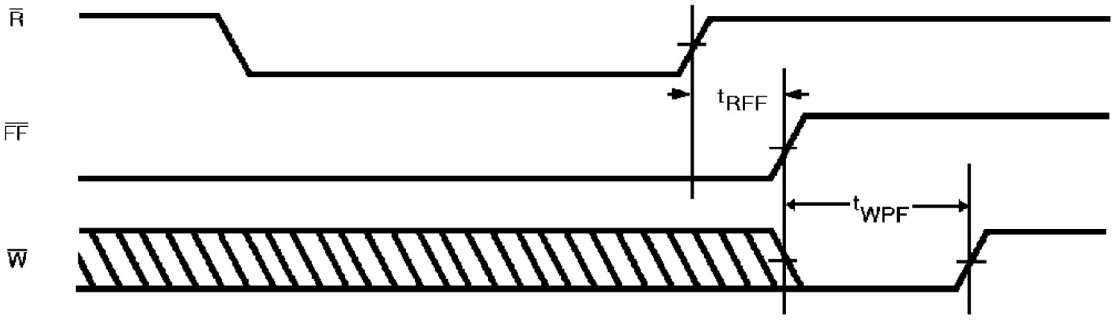


Figure 15. Programmable Half-Full Flag Timing

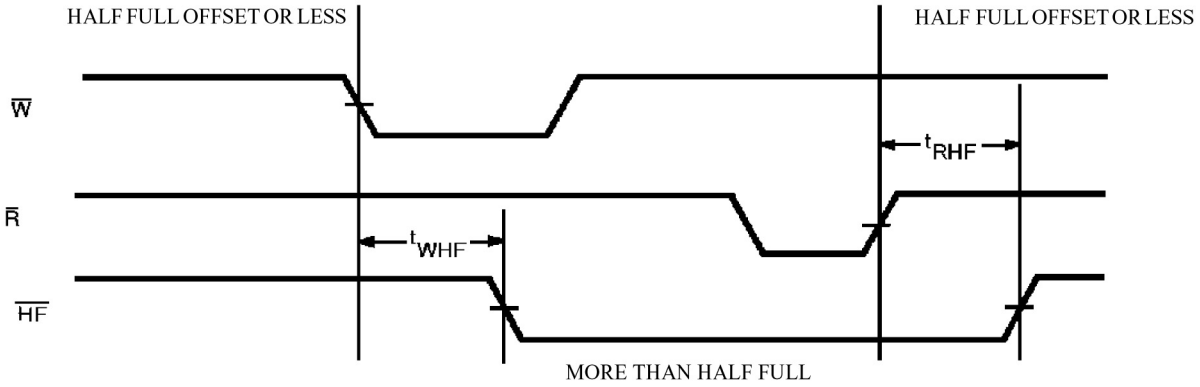


Figure 16. Expansion Out

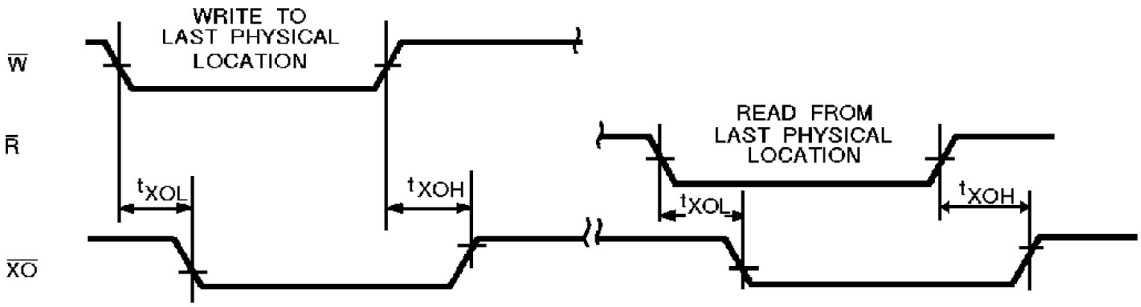


Figure 17. Expansion In

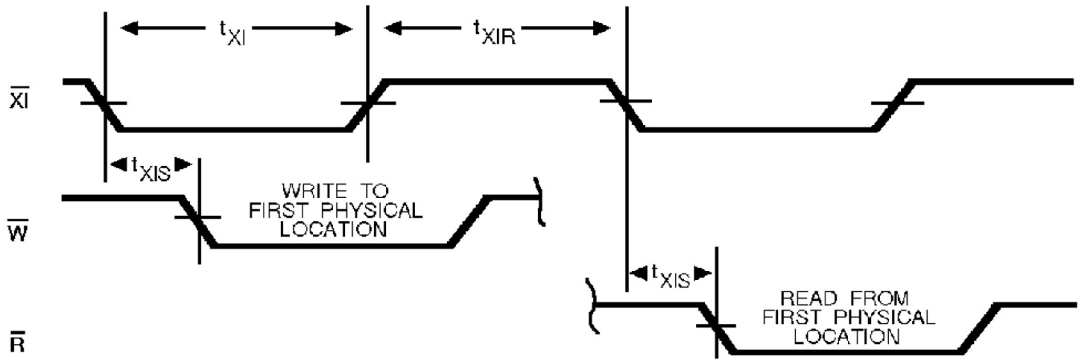


Figure 18. Read Data Flow - Through Mode

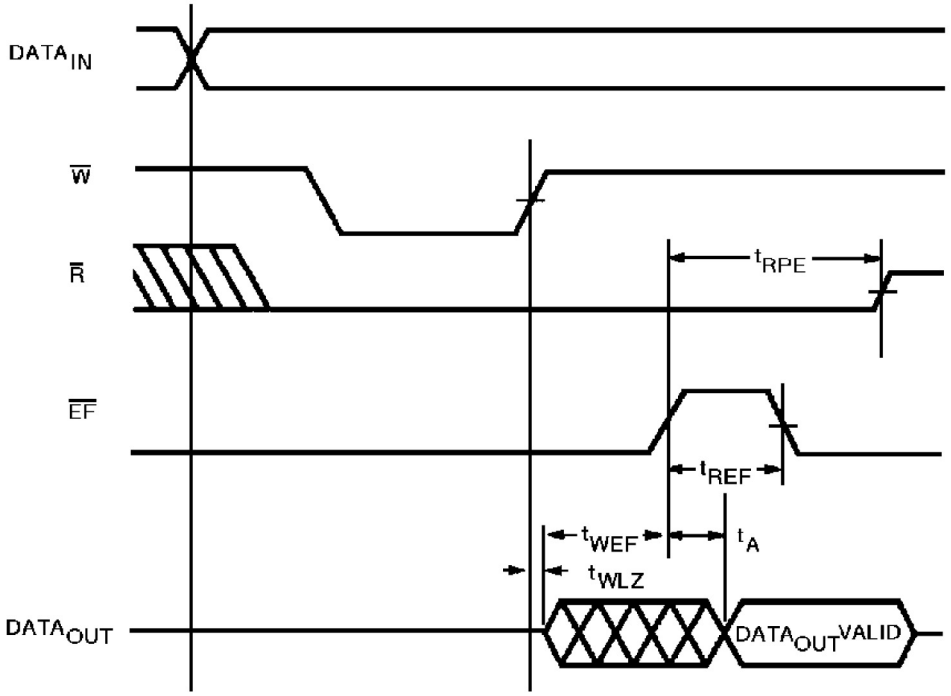
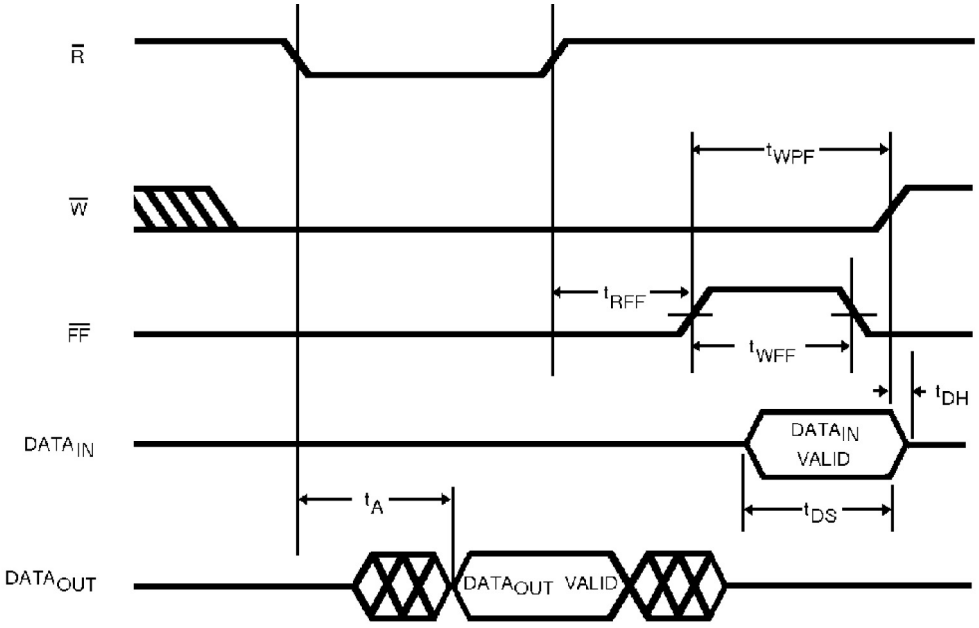


Figure 19. Write Data Flow - Through Mode



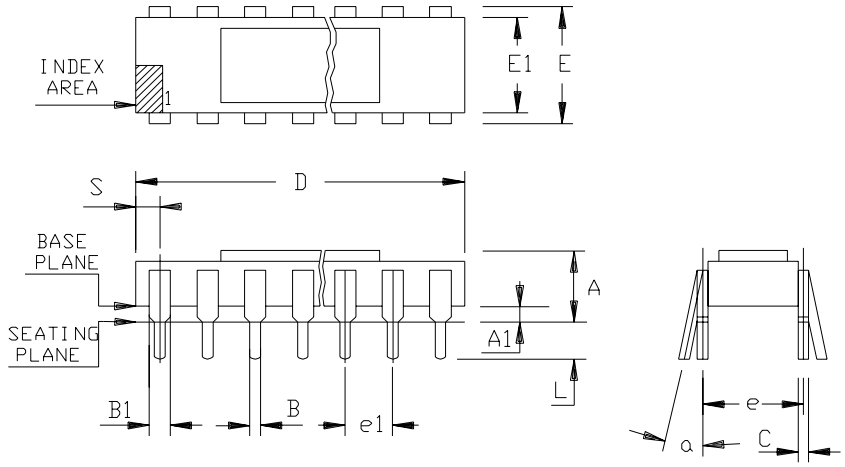
Ordering Information

Reference Number	Temperature Range	Speed	Package	Quality Flow
MMCP-672061FV-15-E[1]	25°C	15 ns	SB28.3	Engineering Samples
MMCP-672061FV-15	-55 to +125°C	15 ns	SB28.3	Mil.
MMCP-672061FV-30	-55 to +125°C	30 ns	SB28.3	Mil.
SMCP-672061FV-15SB	-55 to +125°C	15 ns	SB28.3	SCC B
SMCP-672061FV-30SB	-55 to +125°C	30 ns	SB28.3	SCC B
5962-9317706QTC	-55 to +125°C	15 ns	SB28.3	QML Q
5962-9317705QTC	-55 to +125°C	30 ns	SB28.3	QML Q
5962-9317706VTC	-55 to +125°C	15 ns	SB28.3	QML V
5962-9317705VTC	-55 to +125°C	30 ns	SB28.3	QML V
MMDP-672061FV-15-E	25°C	15 ns	FP28.4	Engineering Samples
MMDP-672061FV-15	-55 to +125°C	15 ns	FP28.4	Mil.
MMDP-672061FV-30	-55 to +125°C	30 ns	FP28.4	Mil.
SMDP-672061FV-15SB	-55 to +125°C	15 ns	FP28.4	SCC B
SMDP-672061FV-30SB	-55 to +125°C	30 ns	FP28.4	SCC B
5962-9317706QNC	-55 to +125°C	15 ns	FP28.4	QML Q
5962-9317705QNC	-55 to +125°C	30 ns	FP28.4	QML Q
5962-9317706VNC	-55 to +125°C	15 ns	FP28.4	QML V
5962-9317705VNC	-55 to +125°C	30 ns	FP28.4	QML V
MM0-672061FV-15-E	25°C	15 ns	Die	Engineering Samples
5962-9317706Q9A	-55 to +125°C	15 ns	Die	QML Q
5962-9317706V9A	-55 to +125°C	15 ns	Die	QML V

Note: 1. Contact Atmel for availability.

Package Drawings

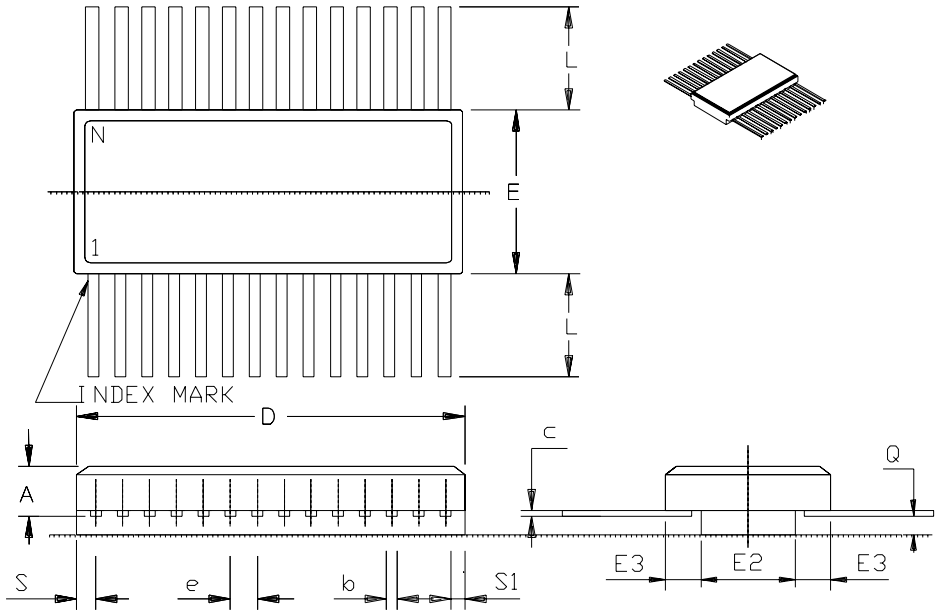
28-lead Side Braze (300 mils)



	MM		INCH	
A	2.82	3.94	.111	.155
A1	0.63	1.14	.025	.045
B	0.38	0.53	.015	.021
B1	0.96	1.52	.038	.060
C	0.20	0.30	.008	.012
D	27.43	28.45	1.080	1.120
E	7.49	8.25	.295	.325
E1	7.11	7.87	.280	.310
L	3.18	4.44	.125	.175
S	1.10	2.03	.043	.080
e	7.62	TYP	.300	TYP
e1	2.54	TYP	.100	TYP
a	0°		15°	

Package Drawings

28-lead Flat Pack (400 mils)



	MM		INCH	
	Min	Max	Min	Max
A	2.29	3.30	.090	.130
b	0.38	0.48	.015	.019
c	0.08	0.15	.003	.006
D	---	18.80	---	.740
E	9.65	10.67	.380	.420
E2	4.57	---	.180	---
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
L	6.35	9.40	.250	.370
Q	0.66	---	.026	---
S	---	1.30	---	.051
S1	0.00	---	.000	---
N	28		28	

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