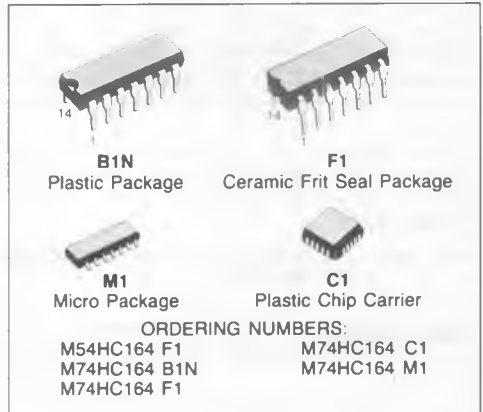


## 8 BIT SIPO SHIFT REGISTER

- **HIGH SPEED**  
 $t_{PD} = 18 \text{ ns (TYP)}$  at  $V_{CC} = 5V$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4 \mu A$  at  $T_A = 25^\circ C$
- **OUTPUT DRIVE CAPABILITY**  
 10 LSTTL LOADS
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $I_{OL} = I_{OH}$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- **WIDE OPERATING VOLTAGE RANGE**  
 $V_{CC}$  (OPR) = 2V to 6V
- **PIN AND FUNCTION COMPATIBLE**  
 WITH 54/74LS164

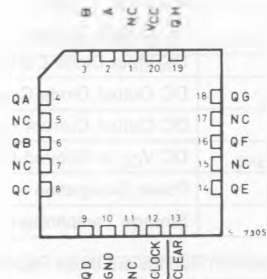
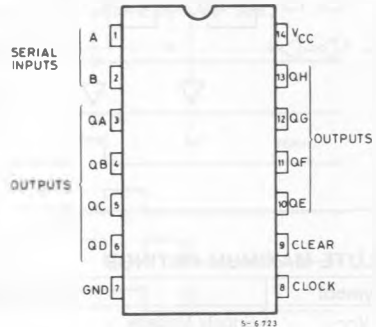


### DESCRIPTION

The M54/74HC164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HC164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs ( $\bar{A} \cdot \bar{B}$ ), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTIONS (top view)



NC =  
 No Internal  
 Connection

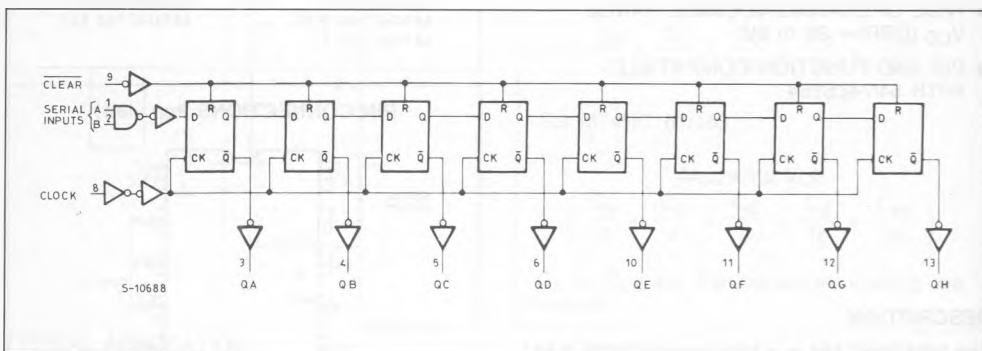
TRUTH TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H		X	X	NO CHANGE			
H		L	X	L	QAn	.....	QGn
H		X	L	L	QAn	.....	QGn
H		H	H	H	QAn	.....	QGn

X: DON'T CARE

QAn ~ QGn: THE LEVEL OF QA ~ QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to 7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Current Per Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C

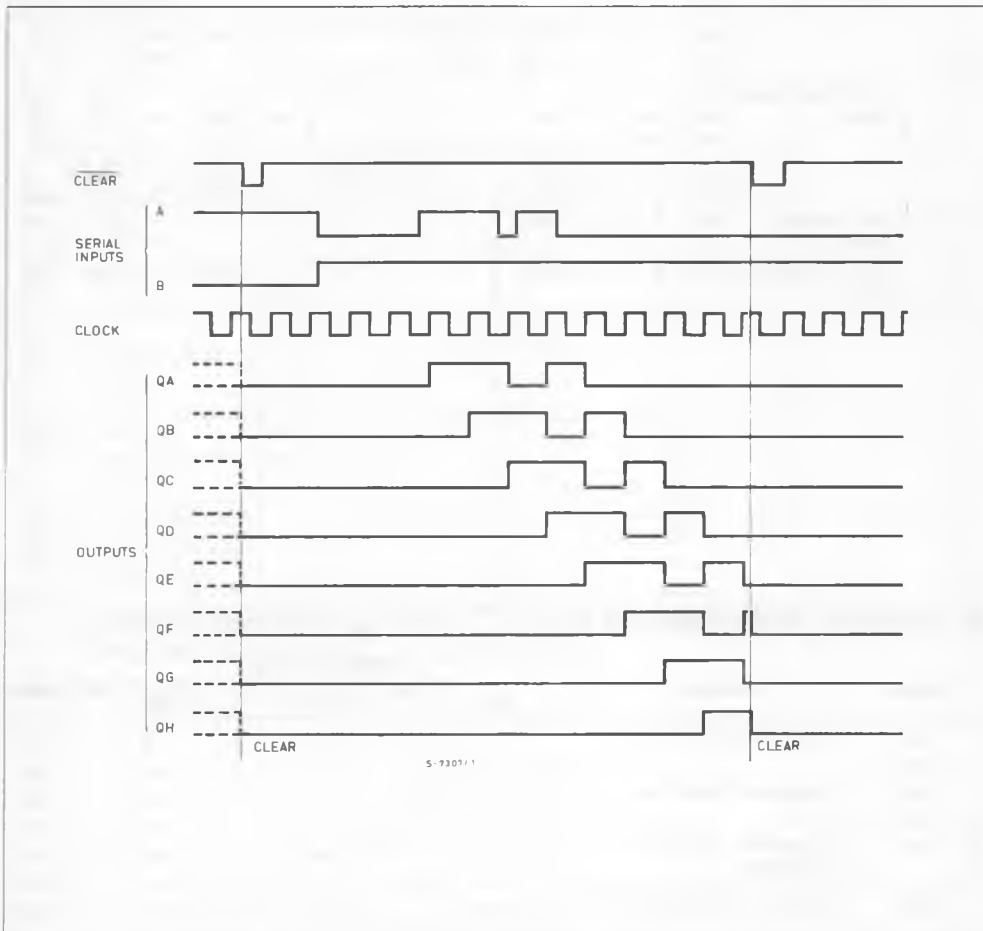
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_A$	Operating Temperature	74HC Series 54HC Series	- 55 to 125 - 40 to 85	°C
$t_r, t_f$	Input Rise and Fall Time	$V_{CC}$ $\begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns	

## TIMING CHART



## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition		T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V <sub>IL</sub>	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V <sub>OH</sub>	High Level Output Voltage	2.0	V <sub>I</sub>	I <sub>O</sub>	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V <sub>IH</sub> or V <sub>IL</sub>	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
V <sub>OL</sub>	Low Level Output Voltage	2.0	V <sub>IH</sub> or V <sub>IL</sub>	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>IH</sub> or V <sub>IL</sub>	4.0 mA 5.2 mA	—	0.17	0.26	—	0.33	—	0.40	V
		6.0			—	0.18	0.26	—	0.33	—	0.40	
		6.0			—	0.18	0.26	—	0.33	—	0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, C<sub>L</sub> = 15pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time		4	8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CK-Q)		18	29	ns
t <sub>PHL</sub>	Propagation Delay Time (CLEAR-Q)		19	30	ns
f <sub>MAX</sub>	Maximum Clock Frequency	30	51		Mhz

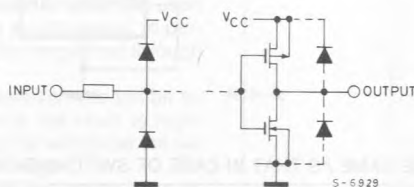
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - Q)	2.0 4.5 6.0		— — —	88 22 19	175 35 30	— — —	220 44 37	— — —	260 52 44	ns
$t_{PHL}$	Propagation Delay Time (CLEAR-Q)	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
$f_{MAX}$	Maximum Clock Frequency	2.0 4.5 6.0		5 27 32	9 46 54	— — —	4 22 26	— — —	3 18 21	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_s$	Minimum Set-up Time (A, B)	2.0 4.5 6.0		— — —	25 7 6	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_h$	Minimum Hold Time (A, B)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
$t_{REM}$	Minimum Removal Time (CLEAR)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
$C_{IN}$	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	112	—	—	—	—	—	pF

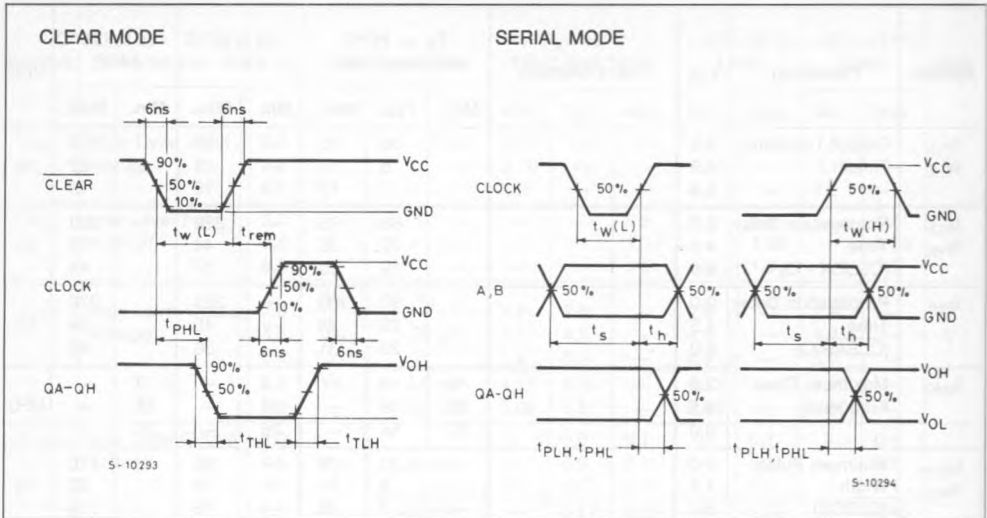
Note (\*)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current is: } I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

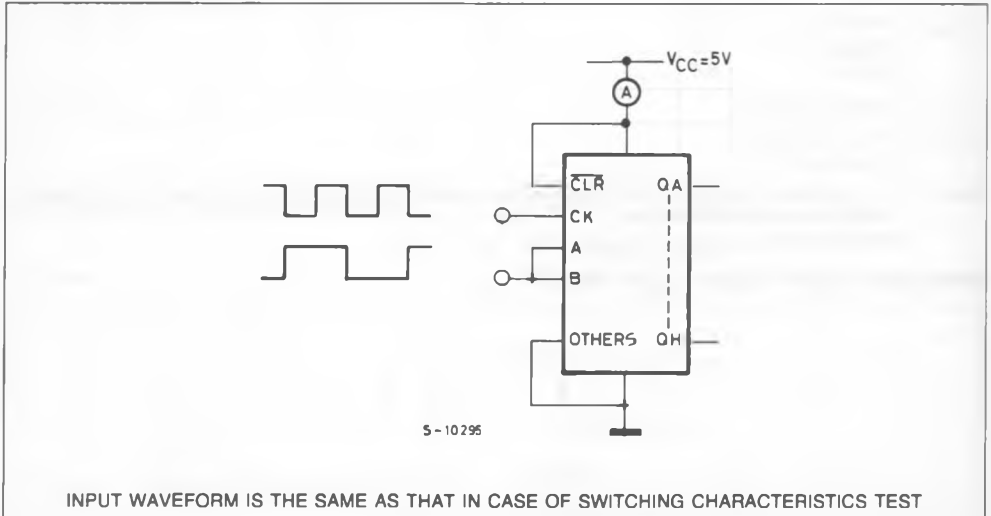
## INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT  $I_{CC}$  (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST