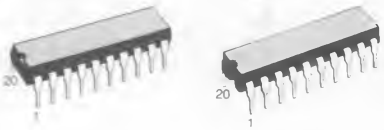
SGS-THOMSON MICROELECTRONICS

M54/74HC299
M74/74HC323

HC299 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
HC323 8-BIT PIPO SHIFT REGISTER WITH SYNCRONOUS CLEAR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) for Q_A, to Q_H,
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) for Q_A, to Q_H
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS299



B1N
Plastic Package

F1
Ceramic Frit Seal Package

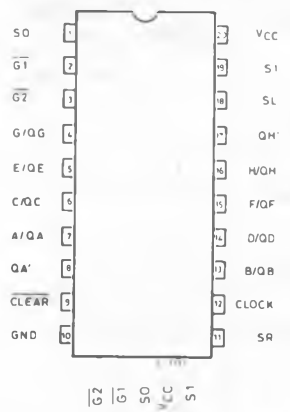
M1
Micro Package

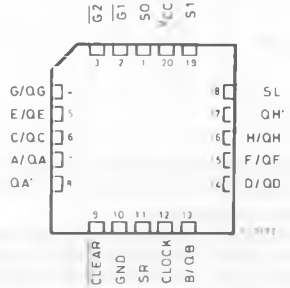
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

PIN CONNECTIONS (top view)



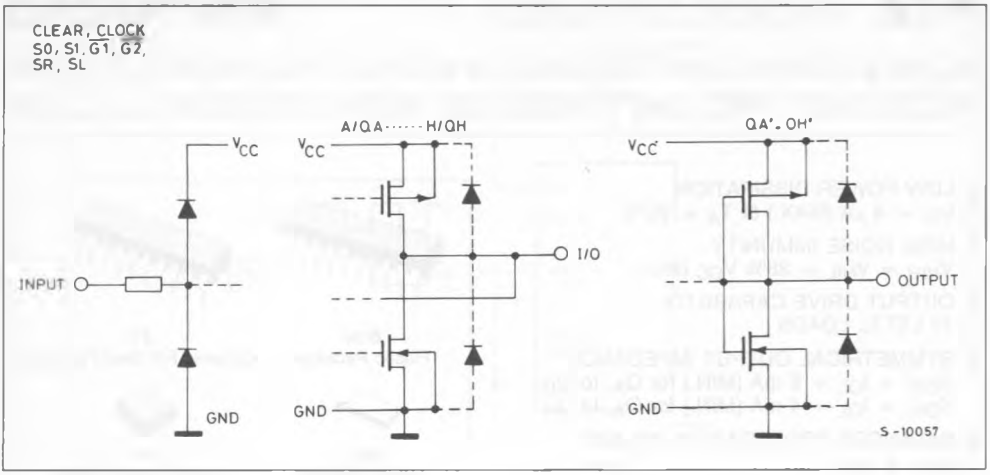


NC =
No Internal
Connection

DESCRIPTION

The M54/74HC299/323 are high speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power consumption.
These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGH and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, (G1, G2) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.
Clear function on the HC299 is asynchronous to CLOCK, while the HC323 is cleared synchronous to clock.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



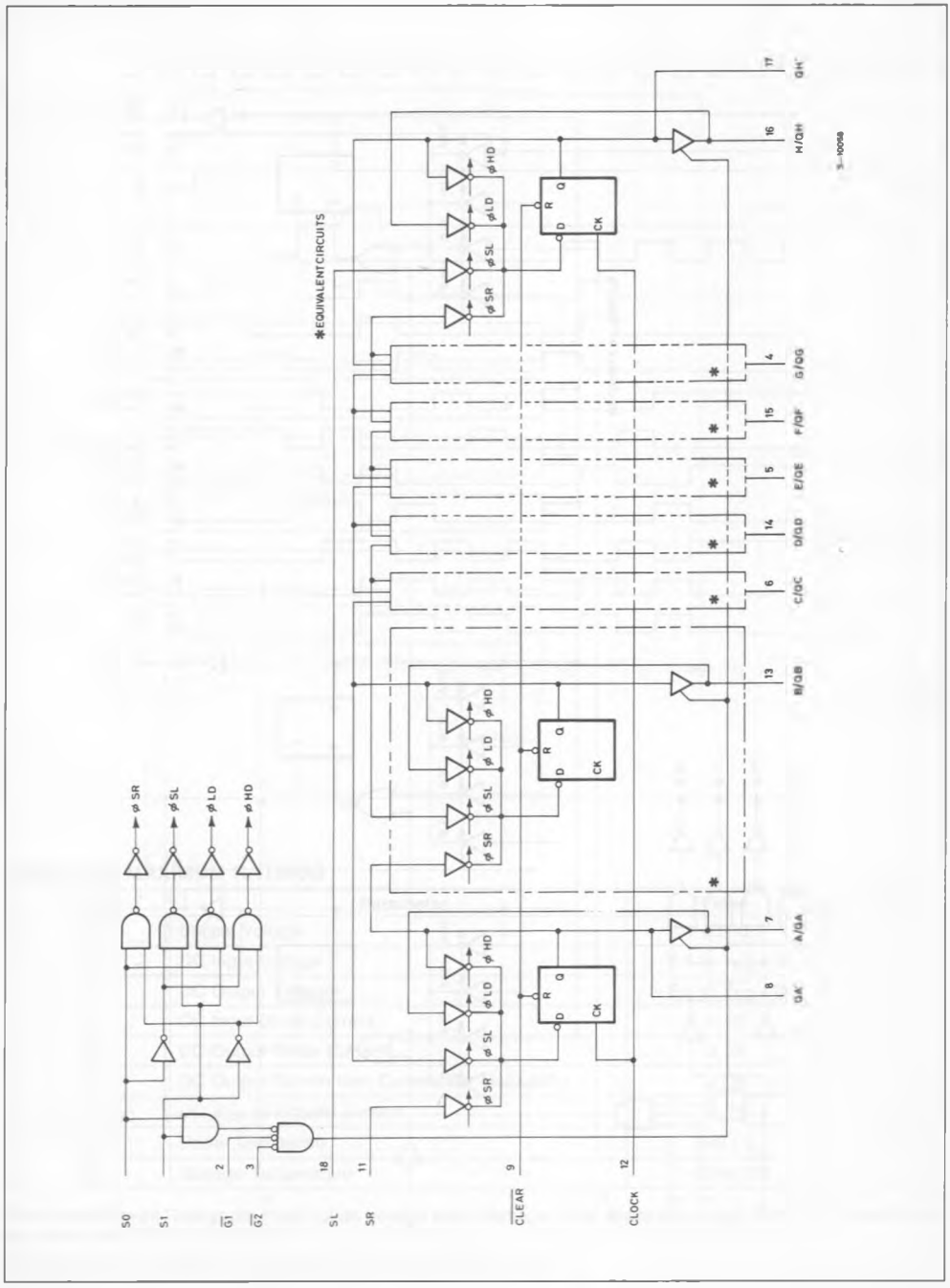
TRUTH TABLE

MODE	INPUTS							INPUTS/OUTPUTS				OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*	(299)	(323)	SL	SR				
Z	L	H	H	X	X	X		X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	↑	X	X	L	L	L	L
	L	X	L	L	L	X	↑	X	X	L	L	L	L
HOLD	H	L	L	L	L	X		X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↑		X	H	H	QGn	H	QGn
	H	L	H	L	L	↑		X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↑		H	X	QBn	H	QBn	H
	H	H	L	L	L	↑		L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↑		X	X	a	h	a	h

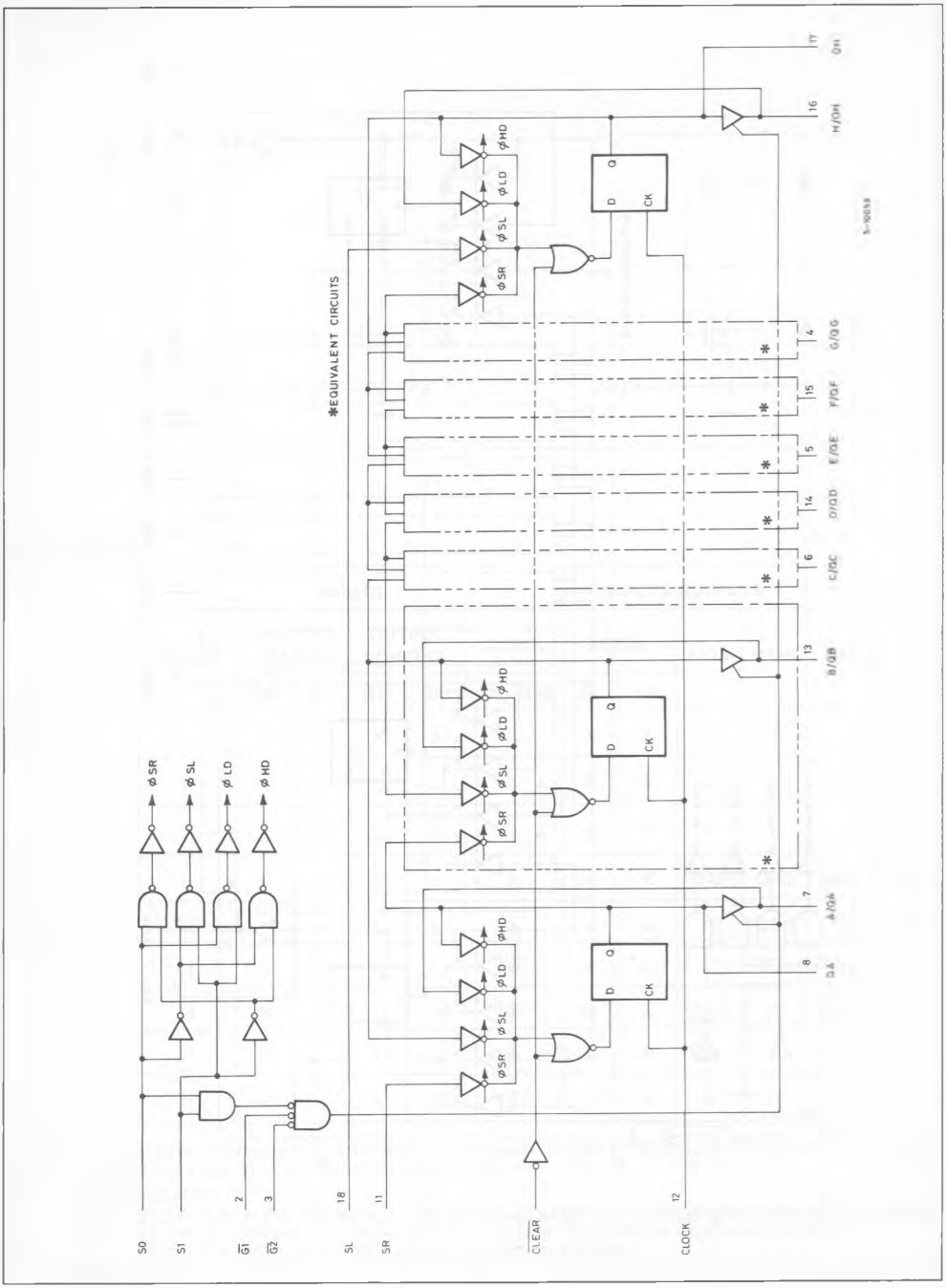
* When one or both output controls are high, the eight, input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Z : HIGH IMPEDANCE
Qno : THE LEVEL OF An BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED.
Qnn : THE LEVEL OF Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY ↓ OR ↑
a,h : THE LEVEL OF THE STEADY-STATE INPUTS A, H, RESPECTIVELY.
X : DON'T CARE

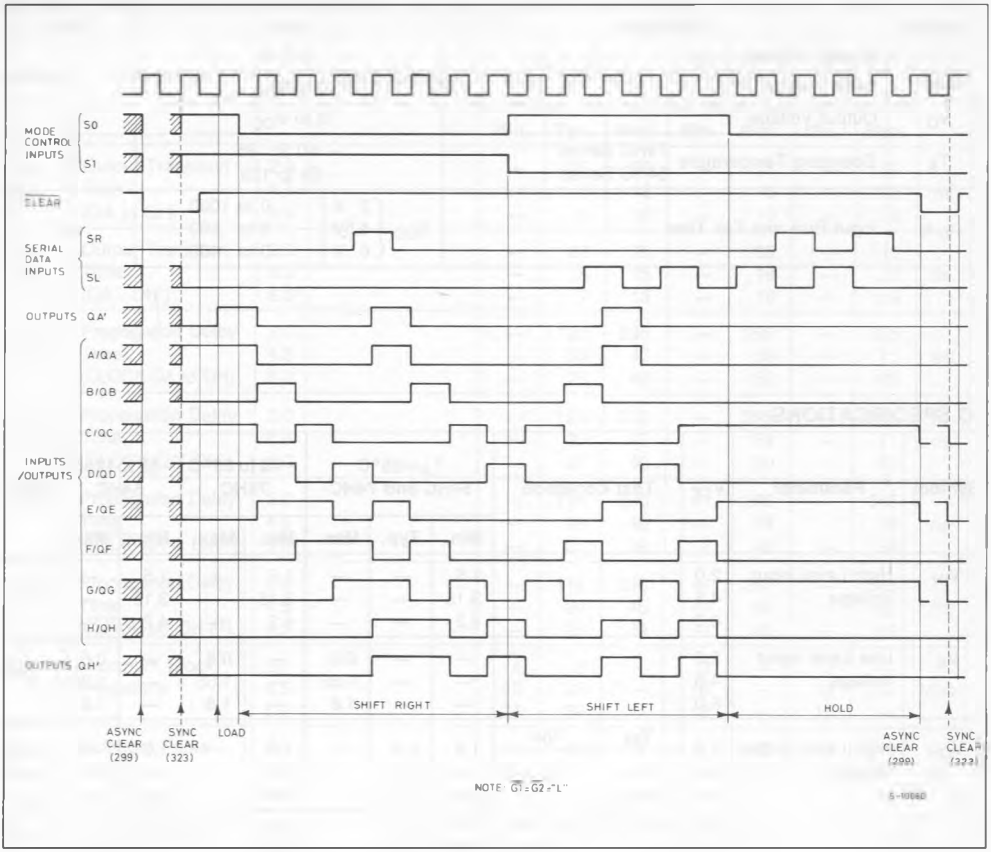
LOGIC DIAGRAM (HC299)



LOGIC DIAGRAM (HC323)



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	– 40 to 85 – 55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	– 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A to Q_H	– 6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		– 7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	Q_A', Q_H'	– 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		– 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A to Q_H	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	Q_A', Q_H'	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	6.0	V_{IN} = V_{IL} or V_{IH} V_{OUT} = V_{CC} or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA to QH)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (QA', QH')	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA to QH)	2.0		—	120	235	—	295	—	355	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA',QH')	2.0		—	120	235	—	295	—	345	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QA to QH)(1)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-QA', QH')(1)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	33	—	16	—	13	—	
		6.0		24	39	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$	2.0		—	50	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
t_s	Minimum Set-up Time (SL, SR, A to H)	2.0		—	25	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
t_s	Minimum Set-up Time (S0, S1)	2.0		—	50	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	32	
t_s	Minimum Set-up Time ($\overline{CLEAR}$) (2)	2.0		—	32	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (SL, SR, A to H)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (S0, S1)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	

(1) Apply to M54/74HC299
(2) Apply to M54/74HC323

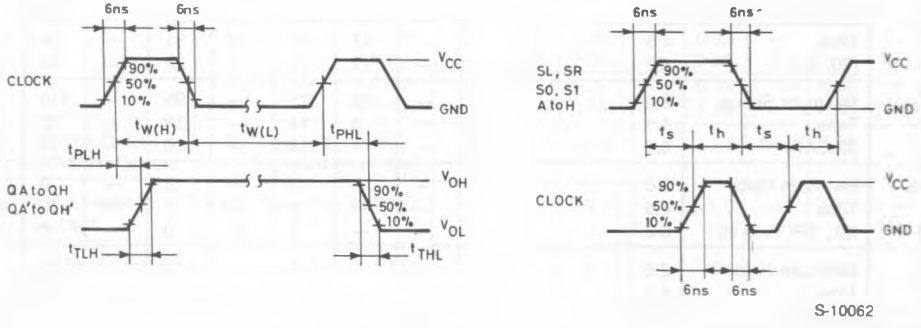
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_h	Minimum Hold Time ($\overline{CLEAR}$) (2)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$) (1)	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1k\Omega$	—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1k\Omega$	—	112	200	—	250	—	300	ns
		4.5		—	28	40	—	50	—	60	
		6.0		—	24	34	—	43	—	51	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance (QA to QH)			—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	221	—	—	—	—	—	pF

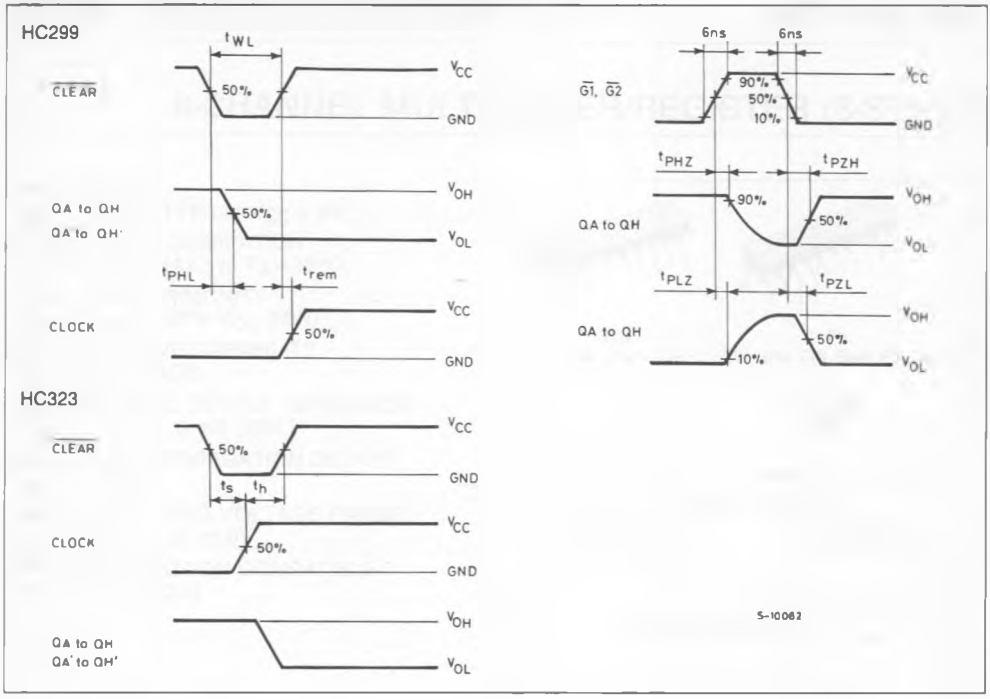
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average opeating current can be obtained from the equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

(1) Apply to M54/74HC299
(2) Apply to M54/74HC323

SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



TEST CIRCUIT I_{CC} (Opr.)