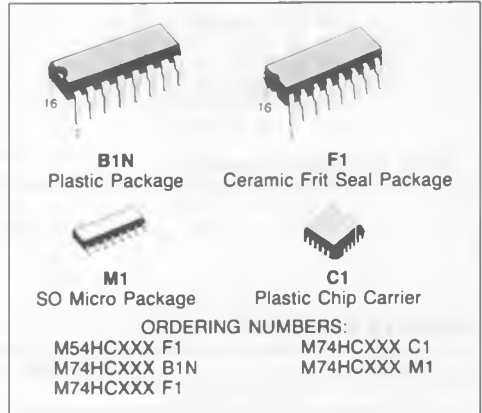


HEX BUS BUFFER (3-STATE)

HC365 NON-INVERTING - HC366 INVERTING

PRELIMINARY DATA

- **HIGH SPEED**
 $t_{PD} = 13 \text{ ns}$ (Typ) at $V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6 \text{ mA}$ (MIN.)
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 V_{CC} (OPR) = 2V to 6V
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS365/366



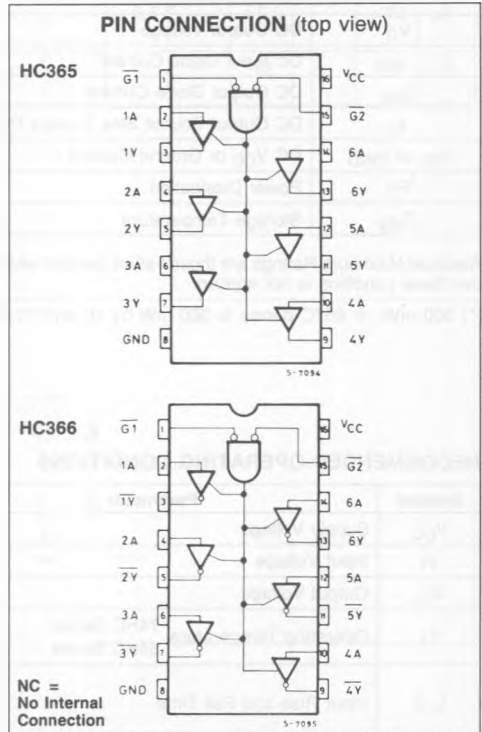
DESCRIPTION

The M54/74HC365 and the M54/74HC366 are high speed CMOS HEX BUS BUFFER fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$); all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, under all other conditions these output are disabled to be high-impedance. These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

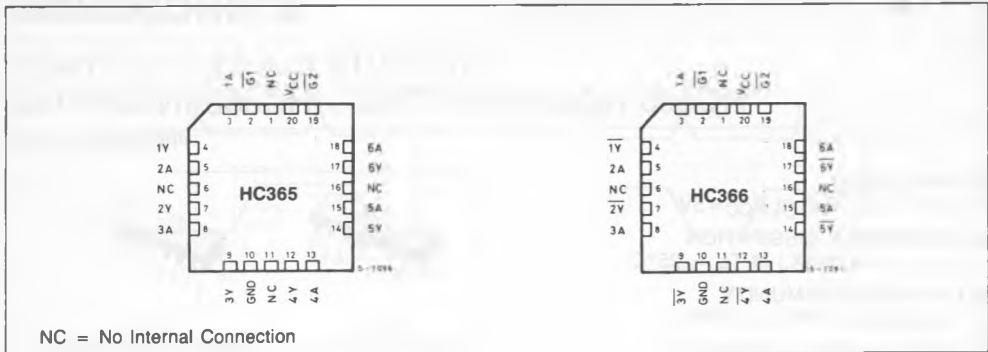
TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	A_n	Y_n (365)	\overline{Y}_n (366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X: DON'T CARE Z: HIGH IMPEDANCE



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	DC Input Voltage	- 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	- 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GN} D	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

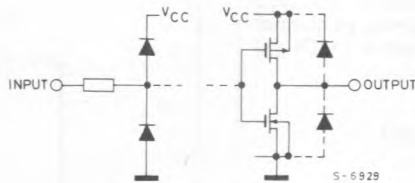
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature	74HC Series 54HC Series	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 4.5V 6 V	ns
			0 to 1000 0 to 500 0 to 400

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C			- 40 to 85°C		- 55 to 125°C		Unit
					54HC and 74HC			74HC		54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V _{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	- 6.0 mA - 7.8 mA	4.18	4.31	—	4.13	—	4.10	—		
6.0	5.68	5.8		—	5.63	—	5.60	—				
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5			6.0 mA 7.8 mA	—	0.17	0.26	—	0.33	—	
6.0	—	0.18	0.26	—		0.33	—	0.40				
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I _{OZ}	3-State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND I _O = 0		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{PLH} t_{PHL}	Propagation Delay Time*	2.0 4.5 6.0		— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
t_{PLH} t_{PHL}	Propagation Delay Time**	2.0 4.5 6.0		— — —	56 14 12	115 23 20	— — —	145 29 25	— — —	175 35 30	ns
t_{PZL} t_{PZH}	Output Enable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	76 19 16	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	96 24 20	175 35 30	— — —	220 44 37	— — —	265 53 45	ns
C_{OUT}	Output Capacitance			—	10	—	—	—	—	10	pF
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	
$C_{PD} (1)$	Power Dissipation Capacitance		54/74HC365 54/74HC366	—	34 32	—	—	—	—	—	

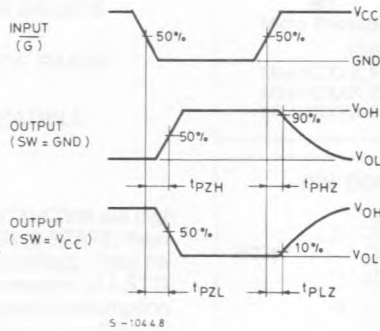
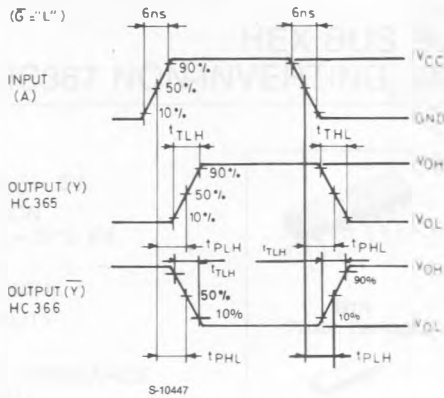
Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation:

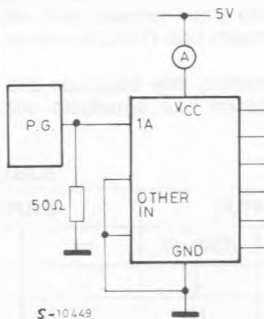
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

- * M54/74HC365 only
- ** M54/74HC366 only

SWITCHING CHARACTERISTICS TEST WAVEFORM



NOTE: SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLE.

TEST CIRCUIT I_{CC} (Opr.)

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

 C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC} \text{ (Opr.)}}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD} , a relatively high frequency of 1MHz was applied to f_{IN} , in order to eliminate any error caused by the quiescent supply current.