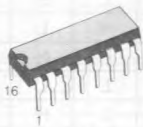
SGS-THOMSON MICROELECTRONICS

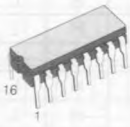
M54HC4511
M74HC4511

BCD TO-7 SEGMENT LATCH/DECODER/DRIVER

- HIGH SPEED
  t_{PD} = 15 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 20 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4511B



B1N
Plastic Package



F1
Ceramic Frit Seal Package

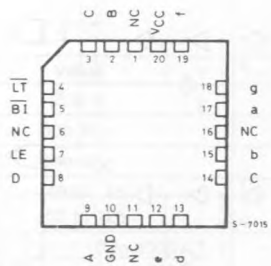
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC4511 F1	M74HC4511 F1
M74HC4511 B1N	M74HC4511 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C²MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

The segment output driver, which is CMOS fabricated in silicon gate C²MOS technology, has large I_{OH} capability which enables common cathode Leds to be directly driven.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L".

These functions operate regardless of other inputs and are used to test the display.

Input BI is used to pulse-modulate the brightness of the display.

When an error input code (over 10) is applied to the BCD input, all segment outputs will go "L"(turn off).

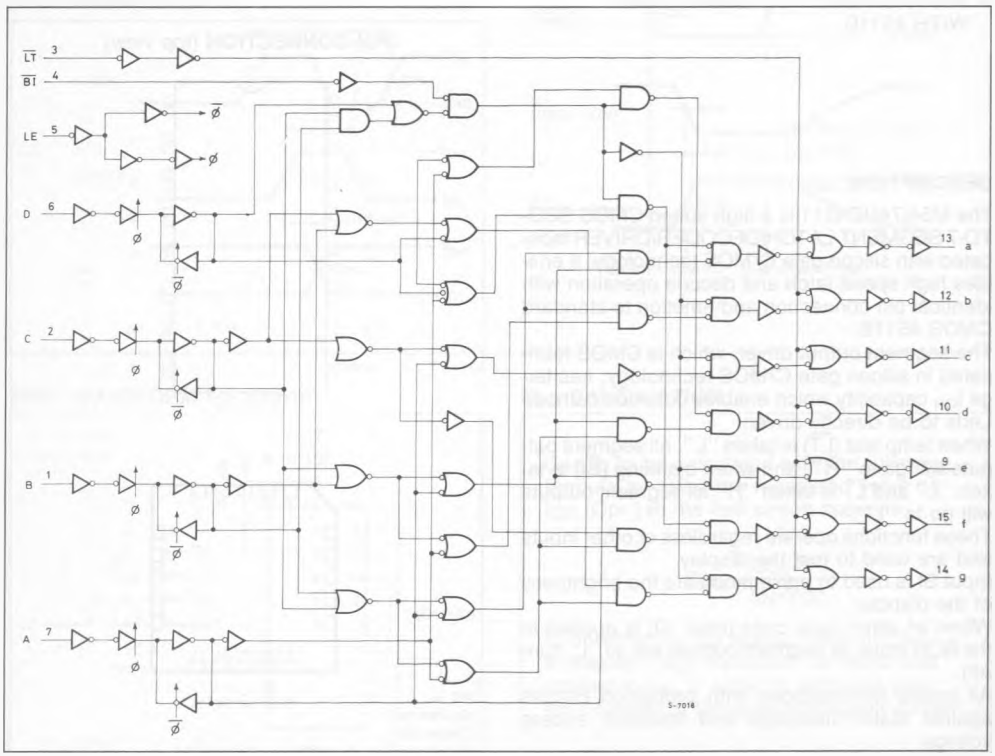
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

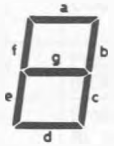
INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

X: DON'T CARE

LOGIC DIAGRAM



DISPLAY MODE



INPUT CODE											
	A	L	H	L	H	L	H	L	H	L	H
	B	L	L	H	H	L	L	H	H	L	L
	C	L	L	L	L	H	H	H	H	L	L
	D	L	L	L	L	L	L	L	L	H	H
DISPLAY		0	1	2	3	4	5	6	7	8	9

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	+25/−35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	+150/−50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

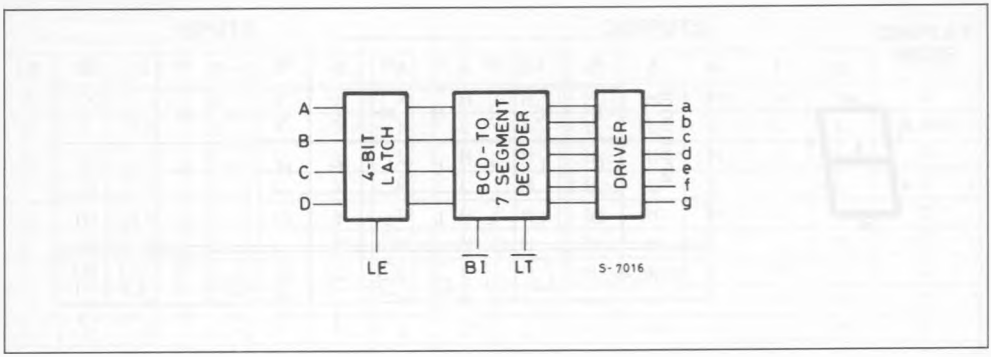
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC}	2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

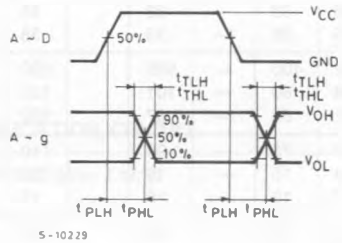
Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O −20 μA −6.0 mA −20 mA −5.2 mA	1.9 4.4 5.9 4.18 3.20 5.68	2.0 4.5 6.0 4.31 3.80 5.8	— — — — — —	1.9 4.4 5.9 4.13 2.90 5.63	— — — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

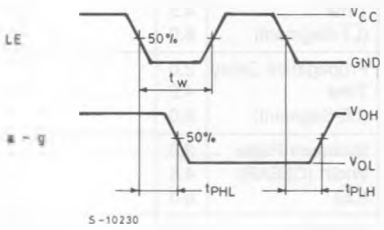
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{BCD}$ - Segment)		46	71	ns
t_{PHL} t_{PHL}	Propagation Delay Time $\overline{BI}$- Segment		28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{LT}$ - Segment		16	26	ns
t_{PHL} t_{PHL}	Propagation Delay Time $\overline{LE}$ - Segment		46	71	ns

SWITCHING CHARACTERISTICS TEST WAVEFORM

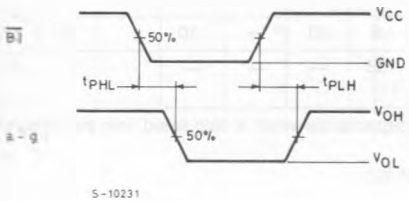
Data Segment Delay Time



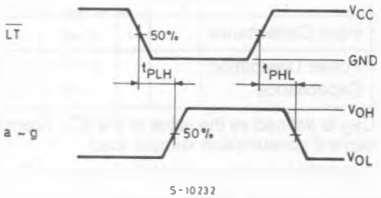
LE-Segment Delay Time



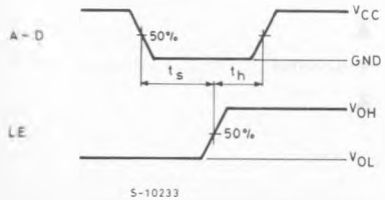
$\overline{BI}$-Segment Delay Time



$\overline{LT}$-Segment Delay Time



Data Set-up/Hold Time



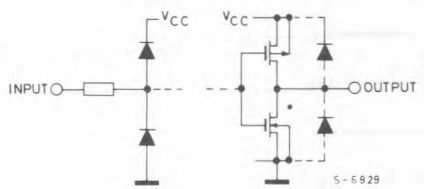
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Low to High	2.0		—	25	60	—	75		90	ns
		4.5		—	6	12	—	15		18	
		6.0		—	5	10	—	13		15	
t_{THL}	Output Transition Time High to Low	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD-Segment)	2.0		—	192	400	—	505		600	ns
		4.5		—	48	80	—	101		120	
		6.0		—	41	68	—	87		102	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{BI}$-Segment)	2.0		—	116	250	—	315		375	ns
		4.5		—	29	50	—	63		75	
		6.0		—	25	43	—	54		64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LT}$-Segment)	2.0		—	72	150	—	190		225	ns
		4.5		—	18	30	—	38		45	
		6.0		—	15	26	—	33		38	
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Segment)	2.0		—	192	400	—	505		600	ns
		4.5		—	48	80	—	101		120	
		6.0		—	41	68	—	87		102	
$t_{W(L)}$	Minimum Pulse Width (CLEAR) ($\overline{LE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time	2.0		—	35	75	—	95		110	ns
		4.5		—	9	15	—	19		22	
		6.0		—	8	13	—	16		19	
t_h	Minimum Data Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	136	—	—	—			pF

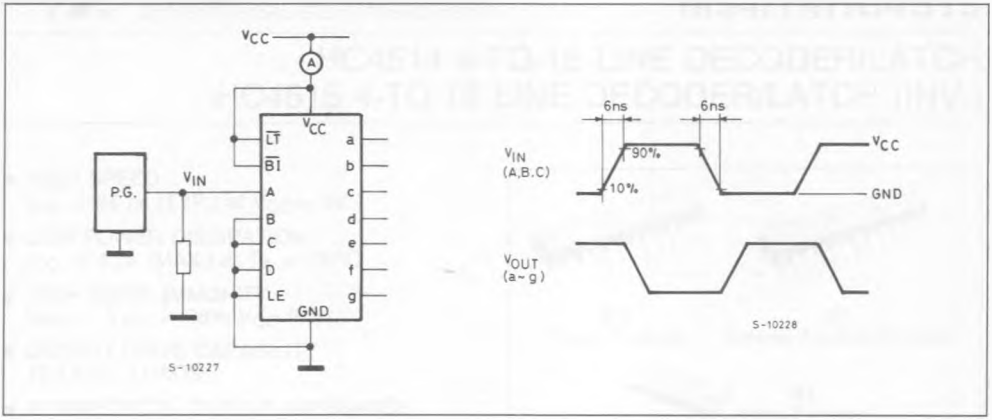
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



APPLICATION CIRCUIT

Static Display Circuit