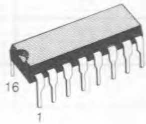
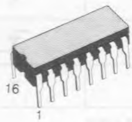
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 27 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120ns ~ 60s over at V_{CC} = 4.5V
- OUTPUT PULSE WIDTH INDEPENDENT FROM TRIGGER INPUT PULSE WIDTH.
- PIN AND FUNCTION COMPATIBLE WITH 4538B



B1N
Plastic Package



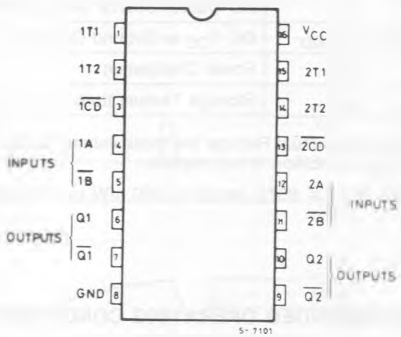
F1
Ceramic Frit Seal Package

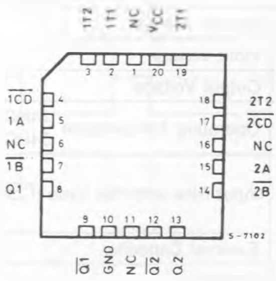
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC123 F1
M74HC123 B1N
M74HC123 F1
M74HC123 C1
M74HC123 M1

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4538 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Each multivibrator features both a negative, A, and a positive, B, edge triggered input, either of which can be used as an inhibt input. Also included is a clear input that when taken low resets the one shot. The monostable multivibrators are retriggerable. That is, they may be triggered reapeatedly while their outputs are generating a pulse and the pulse will be extended. Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7 (R)(C) where PW is in seconds, R in Ohms, and C is in Farads.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H			OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	DC Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	– 65 to 150	°C

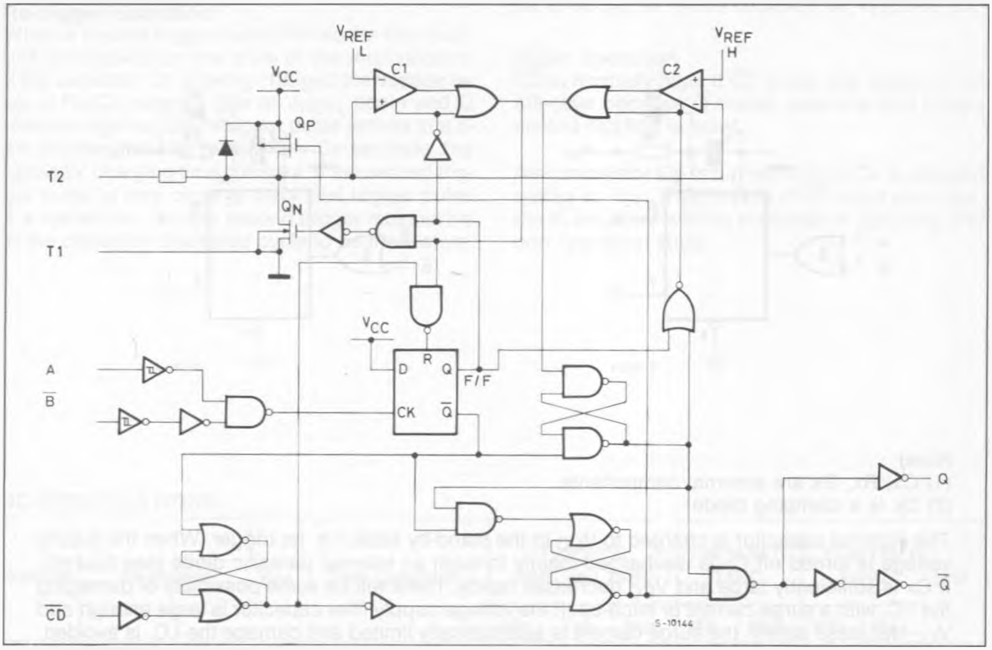
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

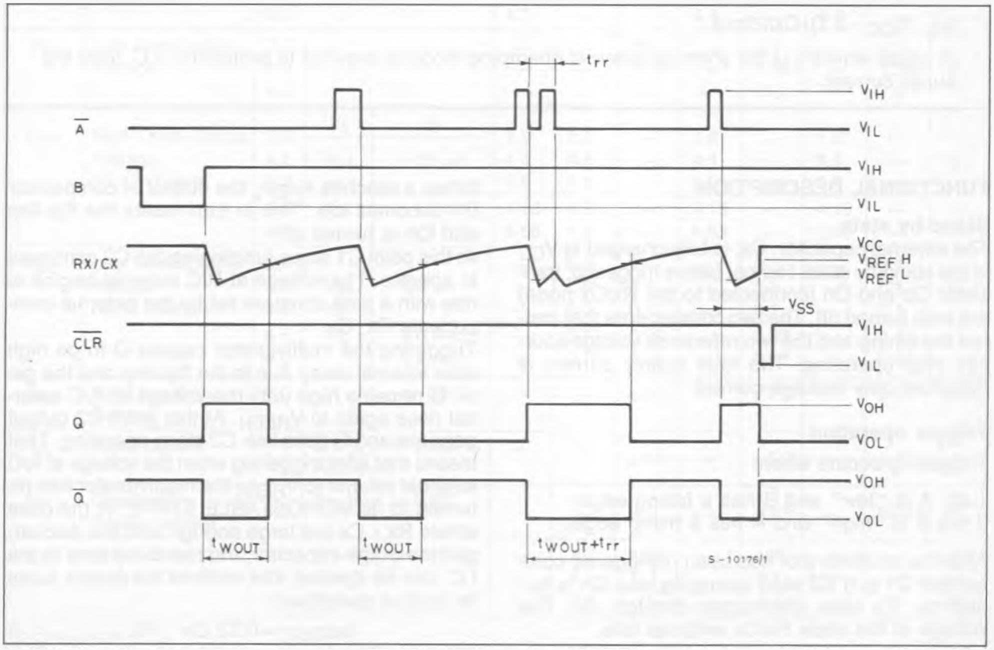
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	– 40 to 85 – 55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns
Cx	External Capacitor	NO LIMITATION	
Rx	External Resistor	V_{CC} 3 V: 5K to 1M V_{CC} 3 V: 1K to 1M	Ω

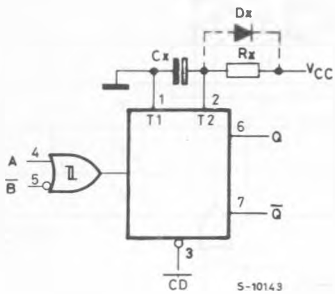
SYSTEM DIAGRAM

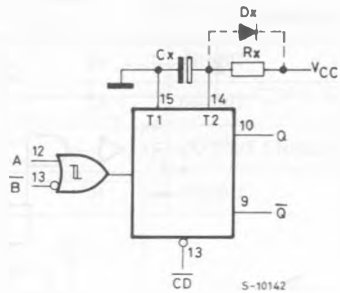


TIMING CHART



BLOCK DIAGRAM





Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external champing diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:

1 st) A is "low" and $\overline{B}$ has a falling edge;
2 nd) $\overline{B}$ is "high" and A has a rising edge;

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.
At this point C1 stops functioning but C2 continues to operate. The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.
Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and G goes low. C2 stops operating. That means that after triggering when the voltage at R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.72\ Cx \cdot Rx$$

FUNCTIONAL DESCRIPTION (Continued)

Re-trigger operation

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx • Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e., the second trigger must arrive in the capacitor discharge cycle to be ineffective.

Hence the minimum time for a second trigger to be effective, trr (Min.) depends on V_{CC} and Cx.

Reset operation

CD is normally high. If $\overline{CD}$ is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if $\overline{CD}$ input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC Min.	Typ.	Max.	− 40 to 85°C 74HC Min.	Max.	− 55 to 125°C 54HC Min.	Max.	Unit
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)		V_I	I_O								
		2.0 4.5 6.0	V_{IH} or V_{IL}	− 20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		− 4.0 mA − 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_{IN}	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{IN}	Input Current	6.0	$V_I = V_{CC}$ or GND Rext/Cext		—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{CC}	Quiescent Supply current	6.0	$V_I = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	μA
I_{CC}	Active State (1) Supply Current	2.0 4.5 6.0	$V_I = V_{CC}$ or GND pins 2, 14 $V_{in} = V_{CC}/2$		— — —	40 0.1 0.2	120 0.3 0.6	— — —	160 0.4 0.8	— — —	— — —	μA mA mA

(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,$\overline{B}$-Q,$\overline{Q}$)		28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$-Q,$\overline{Q}$)		21	34	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

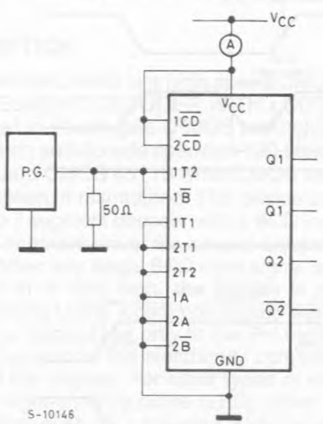
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, $\overline{B}$-Q,$\overline{Q}$)	2.0 4.5 6.0		— — —	128 32 27	250 50 43	— — —	315 63 54	— — —	375 75 64	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$-Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42	— — —	295 59 50	ns
t_{WOUT}	Outpul Pulse Width	3.0 5.0	Cx = 12pF Rx = 1kΩ	— —	210 140	— —	— —	— —	— —	— —	ns
		3.0 5.0	Cx = 100pF Rx = 10kΩ	— —	1.45 1.40	— —	— —	— —	— —	— —	µs
		3.0 5.0	Cx = 1000pF Rx = 10kΩ	— —	10.5 10	— —	— —	— —	— —	— —	µs
Δt_{WOUT}	Output Pulse Width Error Between Circuits (in Same Package)			—	±1	—	—	—	—	—	%
$t_{W(H)}$ $t_{W(L)}$	Minimum Trigger Pulse Width	2.0 4.5 6.0	A_{IN} $\overline{B}_{IN}$	— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Clear Pulse Width	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{rr}	Minimum Retrigger Time	4.5 6.0	Cx = 100pF Rx = 1KΩ	— —	74 63	— —	— —	— —	— —	— —	ns
		4.5 6.0	Cx = 0.01μF Rx = 1KΩ	— —	1.1 1.0	— —	— —	— —	— —	— —	μs
t_{REM}	Minimum Clear Removal time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	90	—	—	—	—	—	pF

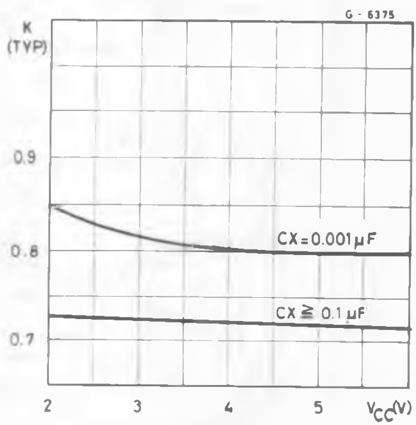
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable) (I_{CC}': Active Supply Current) (Duty: %)

TEST CIRCUIT I_{CC} (Opr.)

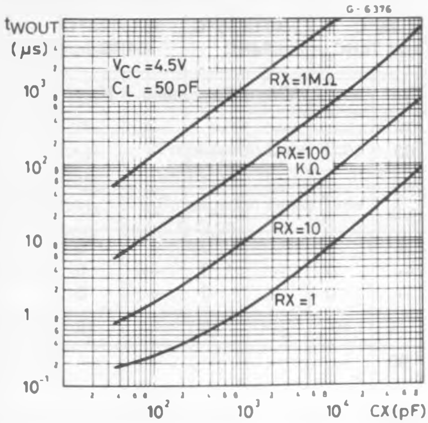


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

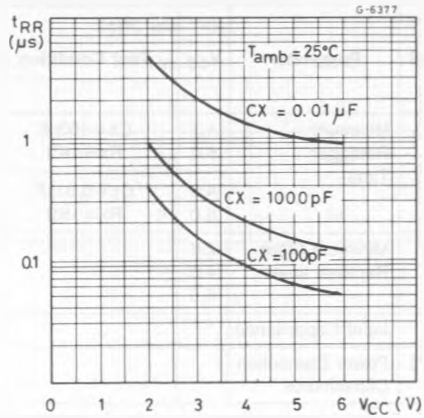
Output Pulse Width Constant
K = Supply Voltage



t_{WOUT} - Cx Characteristics (Typ.)



t_{rr} - V_{CC} Characteristics (Typ.)



SWITCHING CHARACTERISTICS TEST WAVEFORM