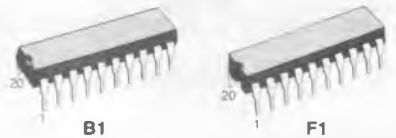
SGS-THOMSON MICROELECTRONICS

M54HCT563/573
M74HCT563/573

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
HCT563 INVERTING - HCT573 NON-INVERTING

- HIGH SPEED
  t_{PD} = 20 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (Min.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS563/573



B1
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

These devices are high speed C²MOS OCTAL LATCHES with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

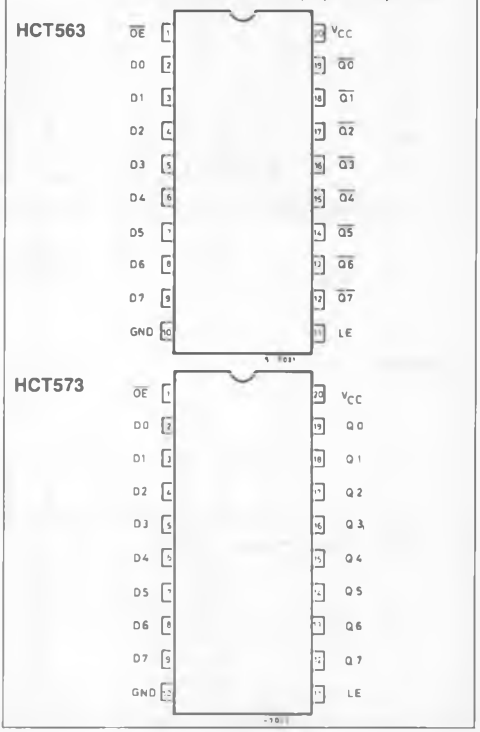
These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE input is held high, the Q outputs will follow the data input precisely or inversely. The Q outputs will be latched precisely or inversely at the logic level of D input data the instant LE is taken low.

When the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level) and when high the outputs will be in a high impedance state.

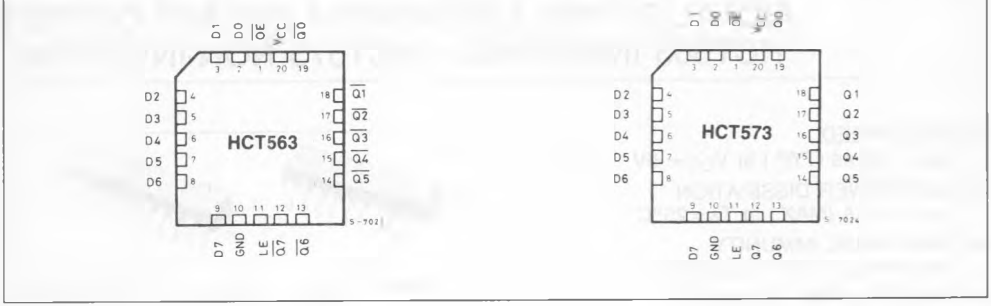
The application designer has a choice of a combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

These integrated circuits are totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families. M54HCT/74HCT devices are designed to directly interface HSC²MOS system with TTL and NMOS components. These components are also plug in replacements for LSTTL devices but with lower power consumption.

PIN CONNECTIONS (top view)

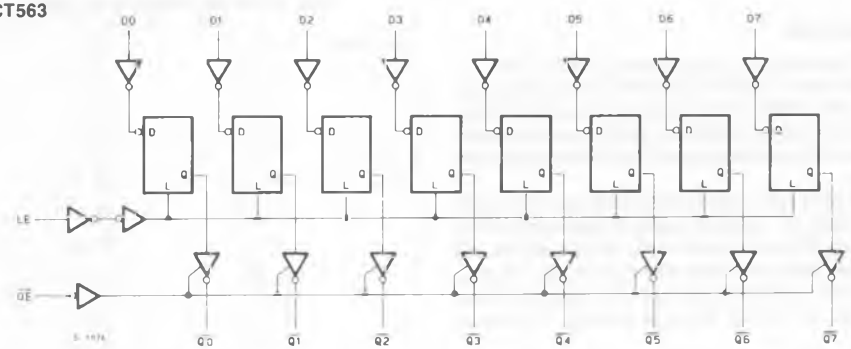


CHIP CARRIER

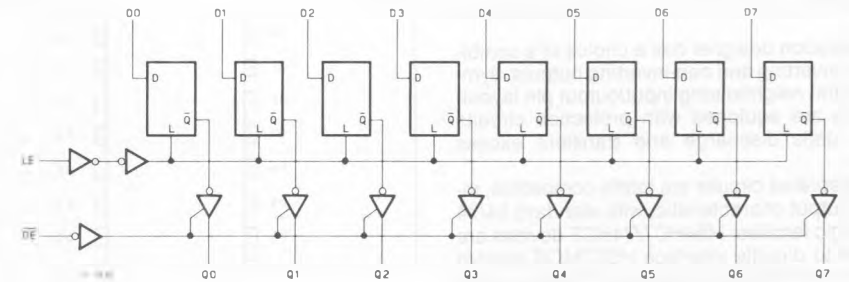


LOGIC DIAGRAM

HCT563



HCT573



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HCT573)	$\overline{Q}$ (HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	Qn
L	H	L	L	H
L	H	H	H	L

Qn: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.
X: DON'T CARE HZ = HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

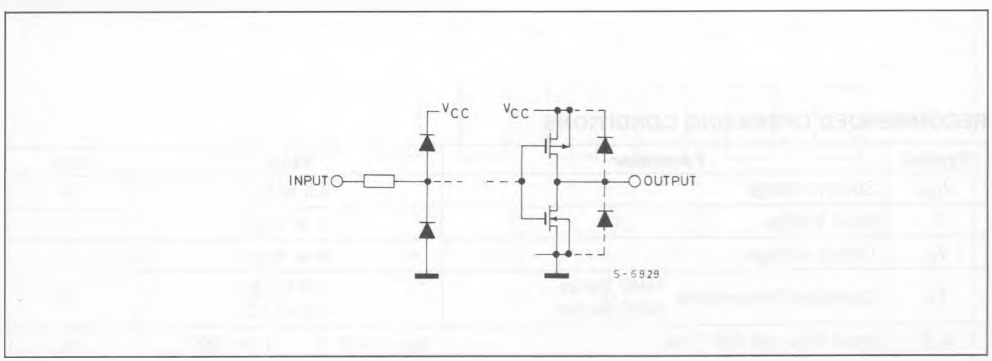
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 4.5V	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage		V_I	I_O								
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4		—	4.4	—	4.4	—	V
		4.5		-6.0 mA	4.18	4.31	—	4.13	—	4.1		
V_{OL}	Low Level Output Voltage	4.5	V_{IH} or V_{IL}	$20\ \mu A$	—		0.1	—	0.1	—	0.1	V
		4.5		6.0 mA	—	0.17	0.32	—	0.37	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3 State Output Current	5.5			—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT

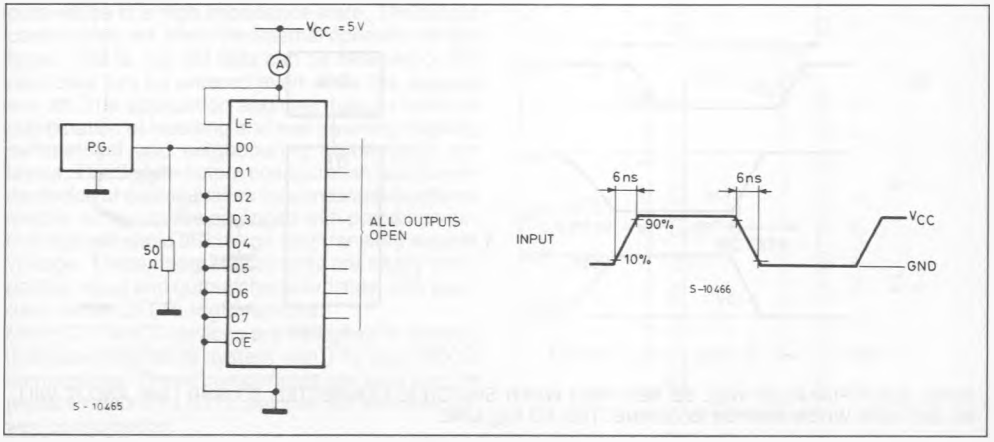


AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q,$\overline{Q}$)	4.5		—	24	35	—	44		53	ns
t_{PLH}	Propagation Delay Time (D-Q,$\overline{Q}$)	4.5		—	22	35	—	44		53	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	4.5		—	8	15	—	19		22	ns
t_s	Minimum Set-up Time	4.5		—	2	10	—	13		15	ns
t_h	Minimum Hold Time	4.5		—	—	5	—	5		5	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	R_L = 1KΩ	—	18	35	—	44		53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	R_L = 1KΩ	—	26	37	—	46		56	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	
C_{PD} (*)	Power Dissipation Capacitance			—	41	—	—	—			

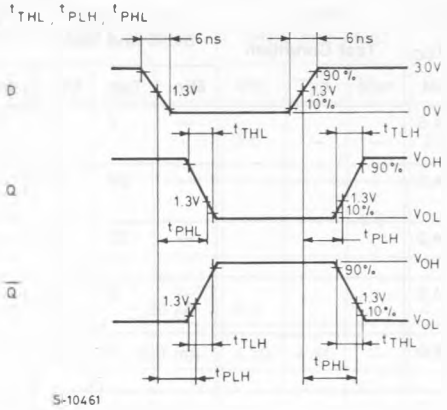
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate).

TEST CIRCUIT I_{CC} (Opr.)

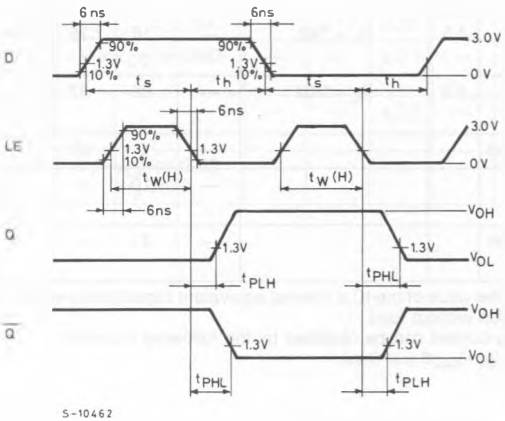


SWITCHING CHARACTERISTICS TEST WAVEFORM

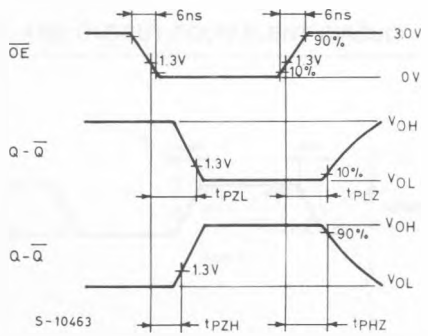
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

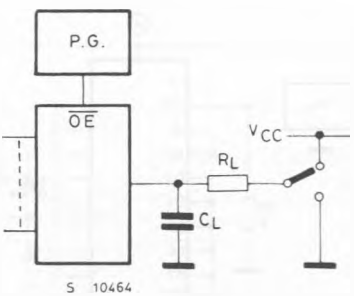


t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$)
t_s, t_h, t_w



t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}





NOTE: EACH FLIP-FLOP WILL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT WILL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.