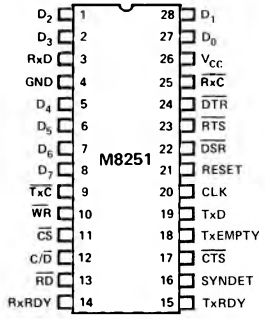
MILITARY TEMP.

M8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1,16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate — DC to 56k Baud (Sync Mode)**
  DC to 8.1k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **All Inputs and Outputs Are TTL Compatible**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

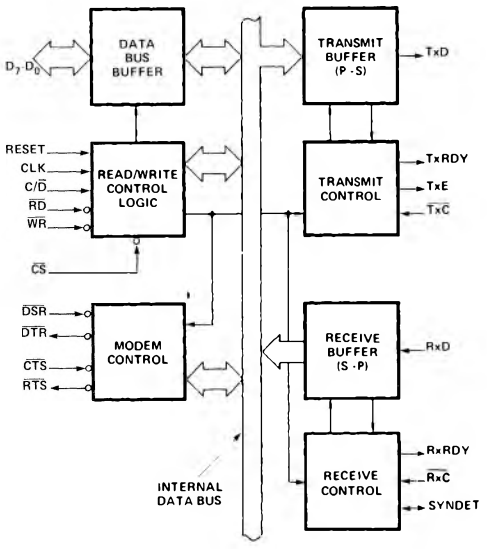
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

M8251 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			–50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{CC}	Power Supply Current		45	80		

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

TEST LOAD CIRCUIT:

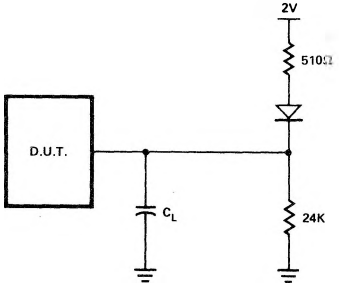
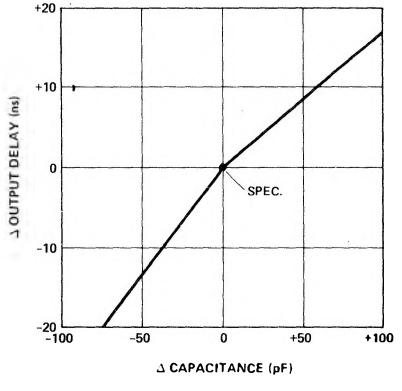


Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)



A.C. CHARACTERISTICS [2]

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.420		1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220			ns	
t_R,t_F	Clock Rise and Fall Time	0		50	ns	
t_{WR}	$\overline{WRITE}$ Pulse Width	400			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	200			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	40			ns	
t_{AW}	Address Stable before $\overline{WRITE}$	20			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20			ns	
t_{RD}	READ Pulse Width	430			ns	
t_{DD}	Data Delay from $\overline{READ}$			350	ns	
t_{DF}	$\overline{READ}$ to Data Floating [3]	25		200	ns	C_L=15pF to 100pF
t_{AR}	Address (CE, C/$\overline{D}$) Stable before $\overline{READ}$	50			ns	
t_{RA}	Address (CE, C/$\overline{D}$) Hold Time for $\overline{READ}$	5			ns	
t_{DTx}	TxD Delay from Falling Edge of TxC			1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2			μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2			μs	
f_{Tx} [1]	Transmitter Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
f_{Rx} [1]	Receiver Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit			16	CLK Period	
t_{Rx}	RxRDY Delay from Center of Data Bit	15		20	CLK Period	
t_{IS}	Internal Syndet Delay from Center of Data Bit	20		25	CLK Period	
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC			16	CLK Period	

Note 1: The TxC and RxC frequencies have the following limitation with respect to CLK.
For ASYNC Mode, t_{Tx} or $t_{Rx} \geq 4.5\ t_{CY}$
For SYNC Mode, t_{Tx} or $t_{Rx} \geq 30\ t_{CY}$
2. AC timings are measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and load circuit of Figure 1.
3. Float timings are measured at V_{OH} = 2.48V, V_{OL} = 2.08V

Figure 1. Test Load Circuit.