PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

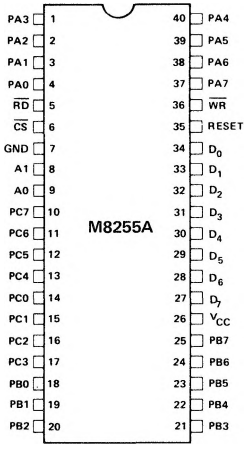
M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS™-80 Microprocessor Family**
- **Full Military Temperature Range -55° C to +125° C**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

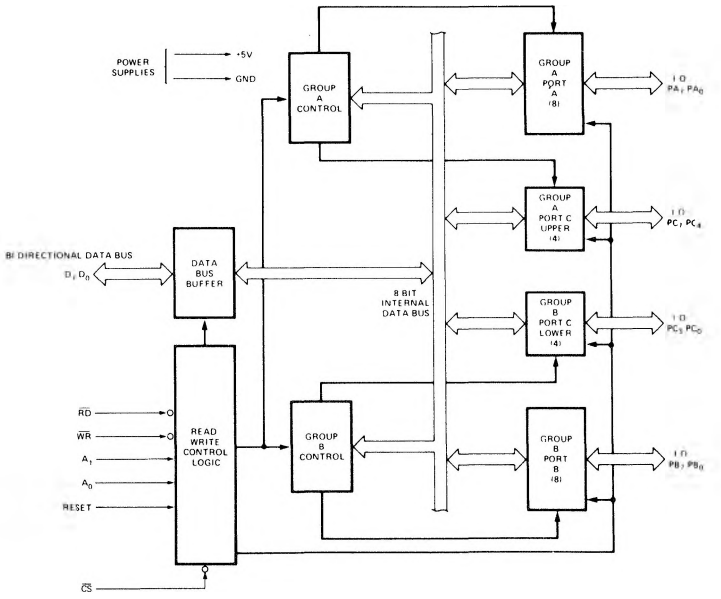
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

M8255A BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to +125°C; V_{CC} = +5V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL} = 1.7mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -50μA (-100μA for D.B. Port)
I_{OH}[1]	Darlington Drive Current	1.0		4.0	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
I_{CC}	Power Supply Current			120	mA	
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
$\|I_{OFL}\|$	Output Float Leakage			10	μA	V_{OUT} = 0.45V/V_{CC}

NOTE:
1. Available on 8 pins only.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			400	ns	
t_{DW}	Time D.B. Stable Before $\overline{WR}$	50			ns	
t_{WD}	Time D.B. Stable After $\overline{WR}$	35			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	20			ns	
t_{CW}	Time $\overline{CS}$ Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time $\overline{CS}$ Stable After $\overline{WR}$	35			ns	
t_{WB}	Delay From $\overline{WR}$ To Output			500	ns	C_L = 50pF
t_{RP}	Pulse Width of $\overline{RD}$	405			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	0			ns	
t_{HR}	Input Hold Time	0			ns	
t_{RD}	Delay From $\overline{RD}$ = 0 To System Bus			295	ns	C_L = 100pF
t_{OD}	Delay From $\overline{RD}$ = 1 To System Bus	10		150	ns	C_L = 15pF/100pF
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time $\overline{CS}$ Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width Of $\overline{STB}$ Pulse	500			ns	
t_{PS}	Set-Up Time For Peripheral	60			ns	
t_{PH}	Hold Time For Peripheral	180			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD}$ = 1	0			ns	

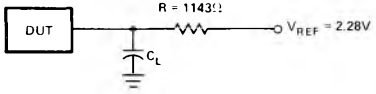
A.C. CHARACTERISTICS (Continued)

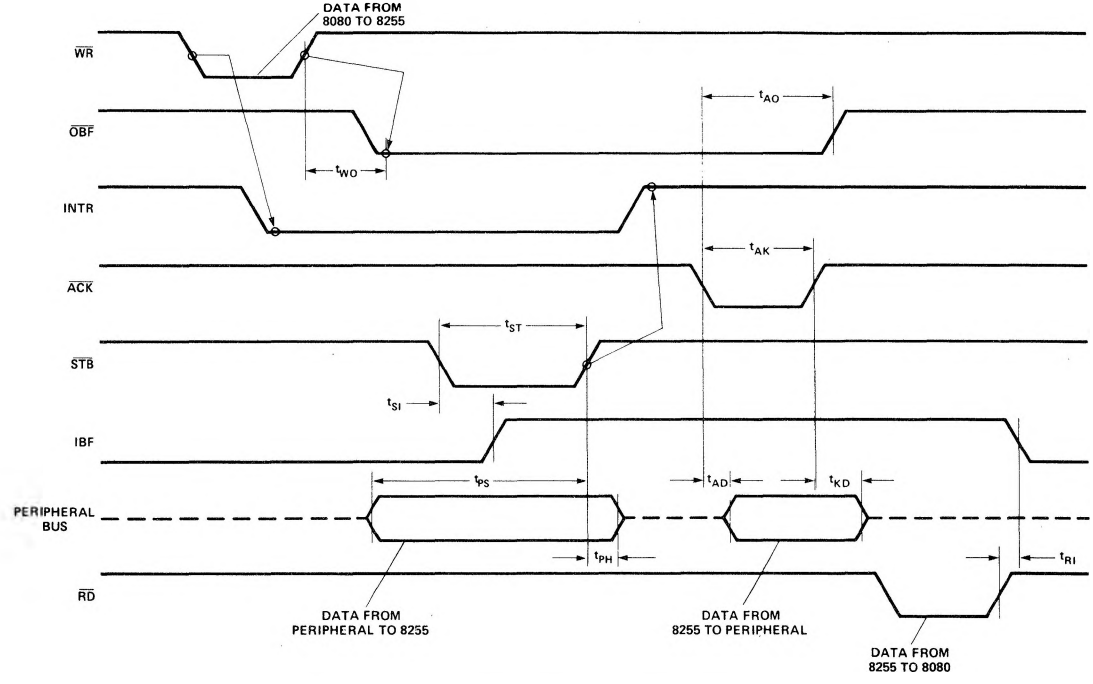
t_{RC}	Hold Time For CS After $\overline{RD}$ = 1	0			ns	
t_{AD}	Time From $\overline{ACK}$ = 0 To Output (Mode 2)			400	ns	C_L = 50pF
t_{KD}	Time From $\overline{ACK}$ = 1 To Output Floating	20		300	ns	C_L = 15pF/50pF
t_{WO}	Time From $\overline{WR}$ = 1 To $\overline{OBF}$ = 0			700	ns	C_L = 50pF
t_{AO}	Time From $\overline{ACK}$ = 0 To $\overline{OBF}$ = 1			450	ns	
t_{SI}	Time From $\overline{STB}$ = 0 To IBF = 1			450	ns	
t_{RI}	Time From $\overline{RD}$ = 1 To IBF = 0			360	ns	

CAPACITANCE $T_A = 25°C$, V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT:





Mode 2 (Bi-directional)