/V\/XXI/V\

CMOS 10-Bit A/D Converter with Track-and-Hold

General Description

The MAX177 is a complete CMOS sampling 10-bit analog-to-digital converter (ADC) that combines an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33µs includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

The MAX177 accepts -2.5V to +2.5V inputs. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX177 employs a standard microprocessor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

Audio and Telecom Processing

High Accuracy Process Control

High Speed Data Acquisition

Functional Diagram
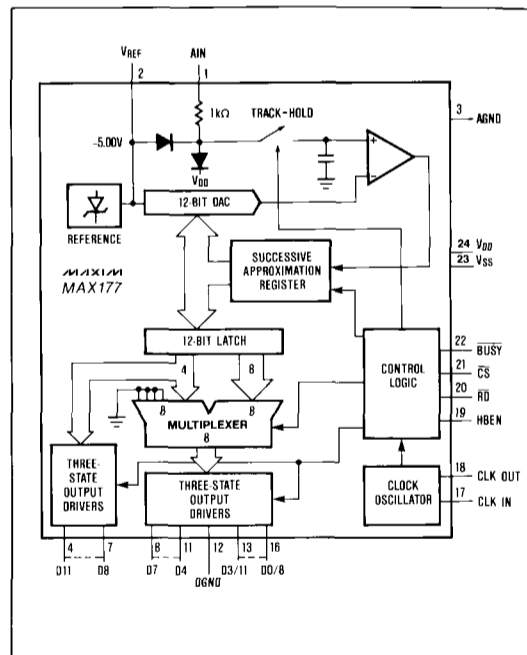
Features

♦ **12-Bit Resolution and 10-Bit Linearity**

♦ **8.33µs Conversion Time**

♦ **Internal Analog Track-Hold**

♦ **6MHz Full Power Bandwidth**

♦ **On-Chip ±40ppm/°C Voltage Reference**

♦ **High Input Resistance (500MΩ)**

♦ **100ns Data Access Time**

♦ **180mW (Max) Power Consumption**

♦ **24 Lead Narrow DIP and Wide SO Packages**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX177CNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX177CWG	0°C to +70°C	Wide SO	±1 LSB
MAX177C/D	0°C to +70°C	Dice**	±1 LSB
MAX177ENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX177EWG	-40°C to +85°C	Wide SO	±1 LSB
MAX177MRG	-55°C to +125°C	CERDIP	±1 LSB

* All devices — 24 lead packages
** Consult factory for dice specifications.

Pin Configuration

Top View
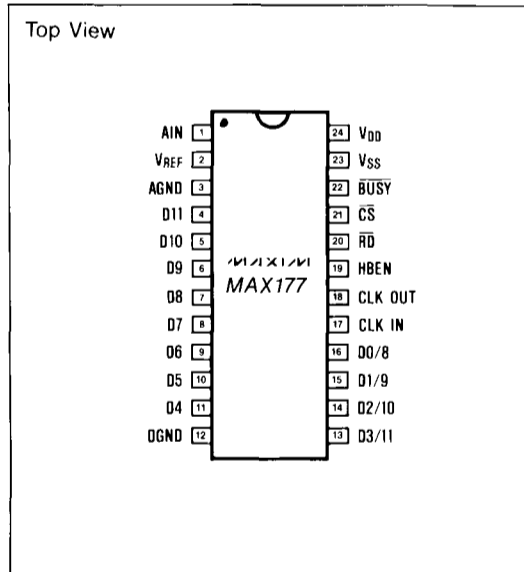
/v\/xi/v\ is a registered trademark of Maxim Integrated Products.

CMOS 10-Bit A/D Converter with Track-and-Hold

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode, T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.5MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN		2.4			V
Input Capacitance (Note 4)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN				10	pF
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	$\overline{CS}$, $\overline{RD}$, HBEN			10	µA
			CLK IN			20	
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SOURCE} = 200µA		4			V
Three-State Leakage Current	I_L	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	µA
Three-State Output Capacitance (Note 4)	C_O					15	pF
POWER REQUIREMENTS							
Postive Supply Voltage	V_{DD}	±5% For Specified Performance			5		V
Negative Supply Voltage	V_{SS}	±5% For Specified Performance		-12		-15	V
Positive Supply Rejection		FS Change, V_{SS} = -15V or -12V V_{DD} = 4.75 to 5.25V			±0.01		%
Negative Supply Rejection		FS Change, V_{DD} = 5V V_{SS} = -14.24 to -15.75V V_{SS} = -11.4 to -12.6V			±0.01		%
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			7	10	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -12V			104	150	mW

Note 1: Typical change over temp is ±1mV.
Note 2: Ideal last code transition = FS -1.8mV LSB, adjusted for offset.
Note 3: Full Scale Tempco = dFS/dT, where dFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Guaranteed by design, not subject to test.
Note 5: V_{REF} Tempco = $dV_{REF}//dT$, where dV_{REF} is reference voltage change from T_A = 25°C to $T_{MIN}T_{MAX}$.
Note 6: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 7: This specification is 100% production tested.
Note 8: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 9: t_7 is defined as the time required for the data line to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX177, please refer to MAX163/164/167 data sheet.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode, T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.5MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN		2.4			V
Input Capacitance (Note 4)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN				10	pF
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	$\overline{CS}$, $\overline{RD}$, HBEN			10	µA
			CLK IN			20	
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SOURCE} = 200µA		4			V
Three-State Leakage Current	I_L	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	µA
Three-State Output Capacitance (Note 4)	C_O					15	pF
POWER REQUIREMENTS							
Postive Supply Voltage	V_{DD}	±5% For Specified Performance			5		V
Negative Supply Voltage	V_{SS}	±5% For Specified Performance		-12		-15	V
Positive Supply Rejection		FS Change, V_{SS} = -15V or -12V V_{DD} = 4.75 to 5.25V			±0.01		%
Negative Supply Rejection		FS Change, V_{DD} = 5V V_{SS} = -14.24 to -15.75V V_{SS} = -11.4 to -12.6V			±0.01		%
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			7	10	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -12V			104	150	mW

Note 1: Typical change over temp is ±1mV.
Note 2: Ideal last code transition = FS -1.8mV LSB, adjusted for offset.
Note 3: Full Scale Tempco = dFS/dT, where dFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Guaranteed by design, not subject to test.
Note 5: V_{REF} Tempco = dV_{REF}//dT, where dV_{REF} is reference voltage change from T_A = 25°C to $T_{MIN}T_{MAX}$.
Note 6: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 7: This specification is 100% production tested.
Note 8: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 9: t_7 is defined as the time required for the data line to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX177, please refer to MAX163/164/167 data sheet.

CMOS 10-Bit A/D Converter with Track-and-Hold

TIMING CHARACTERISTICS

(V$_{DD}$ = +5V, V$_{SS}$ = –12V or –15V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, Note 6, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T$_A$ = 25°C			MAX177C/E		MAX177M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t$_1$		0			0		0		ns
$\overline{RD}$ to BUSY Delay (Note 7)	t$_2$	CL = 50pF		80	170		220		260	ns
Data Access Time (Notes 7, 8)	t$_3$	CL = 100pF		50	100		130		150	ns
$\overline{RD}$ Pulse Width	t$_4$		100			130		150		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t$_5$		0			0		0		ns
Data Setup Time After BUSY (Notes 7, 8)	t$_6$			40	80		105		120	ns
Bus Relinquish Time (Notes 7, 9)	t$_7$			30	50		65		75	ns
HBEN to $\overline{RD}$ Setup Time	t$_8$		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t$_9$		0			0		0		ns
Delay Between READ Operations	t$_{10}$		200			200		200		ns
Delay Between Conversions	t$_{11}$		1			1		1		µs
Aperture Delay	t$_{12}$	Jitter < 50ps		25						ns

a. High-Z to V$_{OH}$ (t$_3$) and V$_{OL}$ to V$_{OH}$ (t$_6$)   b. High-Z to V$_{OL}$ (t$_3$) and V$_{OH}$ to V$_{OL}$ (t$_6$)
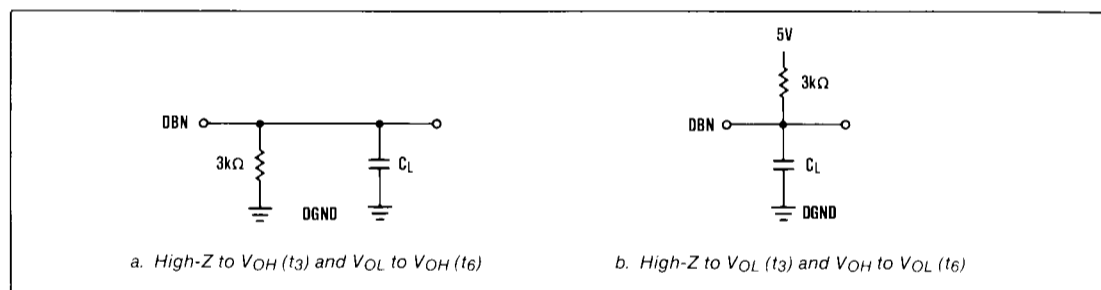
Figure 1. Load Circuits for Access Time

a. V$_{OH}$ to High-Z   b. V$_{OL}$ to High-Z
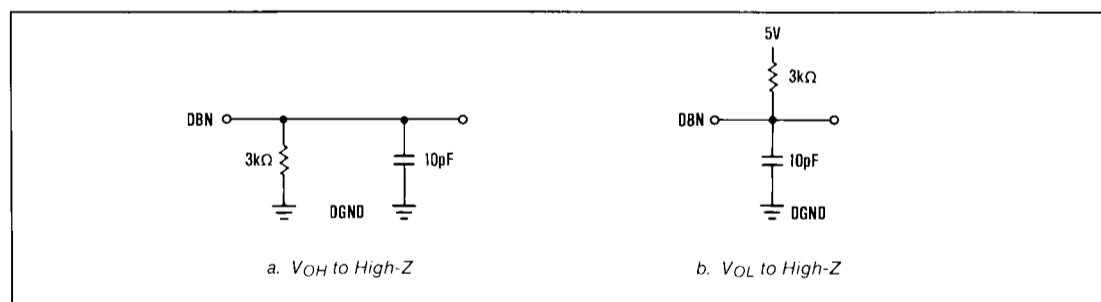
Figure 2. Load Circuits for Bus Relinquish Time