19-2192; Rev 0; 10/01

MAXIM

Dual-Rate Fibre Channel Repeaters

General Description

The MAX3772–MAX3775 are dual-rate (1.0625Gbps and 2.125Gbps) fibre channel repeaters. They are optimized for use in fibre channel arbitrated loop applications and operate from a +3.3V supply. The MAX3772–MAX3775 exceed fibre channel jitter tolerance requirements and can recover data signals with up to 0.7 unit interval (UI) jitter. The circuit's fully integrated phase-locked loop (PLL) provides a frequency lock indication and does not need an external reference clock. These repeaters provide low-jitter CML clock and data outputs, and are pin compatible with the MAX3770 repeater (except RATESEL pin and exposed paddle). The MAX3773/MAX3774 can also be used for impedance transformation between 100Ω (differential) and 150Ω (differential) systems. To reduce the number of external components, all signal inputs and outputs are internally terminated. The MAX3772–MAX3775 are available in 16-pin QSOP-EP packages.

Applications

1.0625Gbps/2.125Gbps Dual-Rate Fibre Channel

Fibre Channel Data Storage Systems

Storage Area Networks

Fibre Channel Hubs

100Ω/150Ω (Differential) Impedance Transformation

Features

- **Pin Selectable 1.0625Gbps/2.125Gbps Dual-Rate Fibre Channel Operation**
- **Exceeds Fibre Channel Jitter Tolerance Requirements**
- **1400mV Differential Output Swing**
- **+3.0V to +3.6V Operation**
- **No Reference Clock Required**
- **Frequency Lock Indication**
- **290mW Power Consumption (MAX3775) at +3.3V**
- **100Ω/150Ω (differential) Input/Output Terminations**

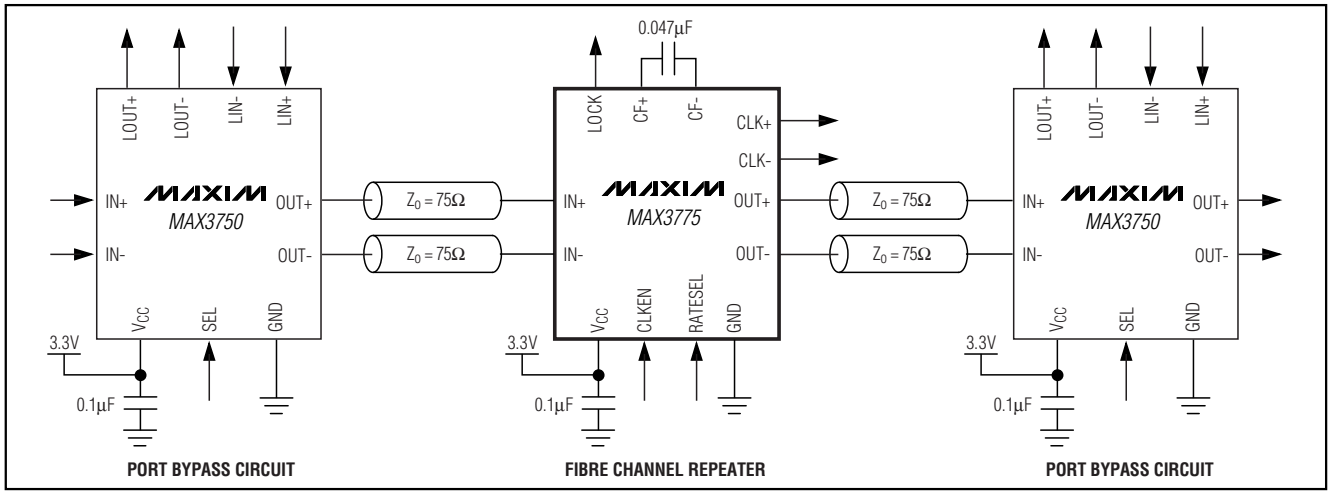
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3772CEE	0°C to +70°C	16 QSOP-EP
MAX3773CEE	0°C to +70°C	16 QSOP-EP
MAX3774CEE	0°C to +70°C	16 QSOP-EP
MAX3775CEE	0°C to +70°C	16 QSOP-EP

Pin Configuration appears at end of data sheet.

Selector Guide appears at end of data sheet.

Typical Operating Circuits



Dual-Rate Fibre Channel Repeaters

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +5.0V
Pin Voltage Levels (IN±, CF±, RATESEL, CLKEN, LOCK) .....-0.5V to (V_{CC} + 0.5V)
Current into LOCK.....-1mA to +10mA
CML Output Currents (OUT±, CLK±), R_{OUT} = 75Ω..... +22mA
CML Output Currents (OUT±, CLK±), R_{OUT} = 50Ω..... +33mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP-EP (derate 18.9mW/°C above +70°C)...702mW
Operating Junction Temperature Range.....-55°C to +150°C
Operating Temperature Range .....-55°C to +110°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, 8B/10B data coding, C_F = 0.047µF, lock pin loaded with ≥ 15kΩ resistor, all high-speed inputs and outputs AC-coupled, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (Note 1)	CLKEN = GND	MAX3772/MAX3773	80	101	140	mA
		MAX3774/MAX3775	68	88	124	
	CLKEN = V_{CC}	MAX3772/MAX3773	115	146	195	
		MAX3774/MAX3775	95	121	164	
Differential Voltage Signal at OUT±	Figure 1	MAX3772/MAX3773, 100Ω terminated	1000	1400	1800	mVp-p
		MAX3774/MAX3775, 150Ω terminated	1000	1400	1800	
Differential Voltage Signal at CLK±	Figure 1	MAX3772/MAX3773 100Ω terminated	1000	1400	1800	mVp-p
		MAX3774/MAX3775, 150Ω terminated	1000	1400	1800	
Input Data Rate Range	1.0625Gbps operation, RATESEL = GND		-100		+100	ppm
	2.125Gbps operation, RATESEL = V_{CC}		-100		+100	
Input Edge Speed	20% to 80% 1.0625Gbps operation		136		325	ps
	20% to 80% 2.125Gbps operation		75		160	
Data Transition Time (OUT±)	20% to 80% (Note 2)		100	130	175	ps
Clock Transition Time (CLK±)	20% to 80% (Note 2)		50	75	100	ps
LOCK Output Low	I_{OL} = +250µA (sinking)				0.4	V
LOCK Output High	I_{OH} = -100µA (sourcing)		2.4			V
CLKEN, RATESEL Input Current			-50		50	µA
CLKEN, RATESEL Input Low			-0.3		0.8	V
CLKEN, RATESEL Input High			2		V_{CC} + 0.3	V
Differential Input Voltage Swing			200		2200	mVp-p
Input Common-Mode Voltage				V_{CC} - 0.45		V
Differential Voltage across CF±	(Note 2)				V_{CC}	V
CDR Lock Time	Input = CJTPAT (Note 3)			500		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, 8B/10B data coding, C_F = 0.047µF, lock pin loaded with ≥ 15kΩ resistor, all high-speed inputs and outputs AC-coupled, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input Resistance (IN±)	MAX3772/MAX3774		78	100	122	Ω
	MAX3773/MAX3775		118	150	182	
Differential Output Resistance (OUT±, CLK±)	MAX3772/MAX3773		78	100	122	Ω
	MAX3774/MAX3775		118	150	182	
Supply Noise Tolerance (Note 4)	10Hz ≤ f < 100Hz			100		mVp-p
	100Hz ≤ f < 1MHz			40		
	1MHz ≤ f < 2.5GHz			10		
OPERATION AT 2.125Gbps (Note 2)						
Random Jitter Generation at OUT± and CLK±	Input = K28.7 (Note 5)			4.4		ps_{RMS}
	Input = CRPAT (Note 6)			2.8		
	Input = CRPAT (Notes 6, 7)			2.9		
Deterministic Jitter on OUT±	Input = K28.5 (Note 8)				22	psp-p
	Input = RPAT (Notes 7, 9)				48	
Total Jitter at OUT±	Input = RPAT (Notes 7, 9, 10)				99	psp-p
Sinusoidal Component of Jitter Tolerance (BER = 10^{-12})	Input = CJTPAT (Notes 3, 7)	f = 85kHz	1.5			UI
		f = 1270kHz	0.1			
		f = 10MHz	0.1			
Total High-Frequency Jitter Tolerance	Input = CJTPAT (Notes 3, 7, 9)		0.7			UI
Jitter Transfer Bandwidth	Measured with 50% edge density				11	MHz
Jitter Transfer Peaking	(Note 11)				0.05	dB
Propagation Delay				1.0	1.5	ns
Clock to Q Delay	Falling clock to data transition		150	280	300	ps
OPERATION AT 1.0625Gbps (Note 2)						
Random Jitter Generation at OUT± and CLK±	Input = K28.7 (Note 5)			6.2		ps_{RMS}
	Input = CRPAT (Note 6)			3.6		
	Input = CRPAT (Notes 6, 7)			4.9		
Deterministic Jitter on OUT±	Input = K28.5 (Note 8)				40	psp-p
	Input = RPAT (Notes 7, 9)				75	
Total Jitter at OUT±	Input = RPAT (Notes 7, 9, 10)				160	psp-p
Sinusoidal Component of Jitter Tolerance (BER = 10^{-12})	Input = CJTPAT (Notes 3, 7)	f = 42.5kHz	1.5			UI
		f = 635kHz	0.1			
		f = 5MHz	0.1			
Total High-Frequency Jitter Tolerance	Input = CJTPAT (Notes 3, 7, 9)		0.7			UI
Jitter Transfer Bandwidth	Measured with 50% edge density				6	MHz
Jitter Transfer Peaking	(Note 11)				0.05	dB
Propagation Delay					5	ns
Clock to Q Delay	Falling clock to data transition		200	510	740	ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, 8B/10B data coding, C_F = 0.047µF, lock pin loaded with ≥ 15kΩ resistor, all high-speed inputs and outputs AC-coupled, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

Note 1: Supply current includes output currents.

Note 2: Guaranteed by design and characterization.

Note 3: Compliant jitter tolerance pattern in hex (CJTPAT):

Pattern Sequence:	Repetitions:
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
87 1E 38 71 E3	41
87 1E 38 70 BC 78 F4 AA AA AA	1
AA AA AA AA AA	12
AA A1 55 55 E3 87 1E 38 71 E1	1
AB 9C 96 86 E6	1
C1 6A AA 9A A6	1

Note 4: Meets jitter output specifications with noise applied.

Note 5: K28.7 Pattern: 00 1111 1000.

Note 6: Compliant random pattern in hex (CRPAT):

Pattern Sequence:	Repetitions:
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
86 BA 6C64 75 D0 E8 DC A8 B4 79 49 EA A6 65	16
72 31 9A 95 AB	1
C1 6A AA 9A A6	1

Note 7: Parameter measured with 0.40UI deterministic jitter (patterns other than K28.7), and 0.20UI random jitter (BER = 10^{-12}) applied to the input. Jitter is in compliance with the inter-enclosure, fibre channel jitter tolerance (at compliance point α_R) and jitter output (at compliance point α_T) specifications (FC-PI rev 10.0). Output jitter is specified as an output total given a non-zero jitter input.

Note 8: K28.5 Pattern: 00 1111 1010 11 0000 0101

Note 9: Random Pattern in hex (RPAT): 3EB0 5C67 85D3 172C A856 D84B B6A6 65

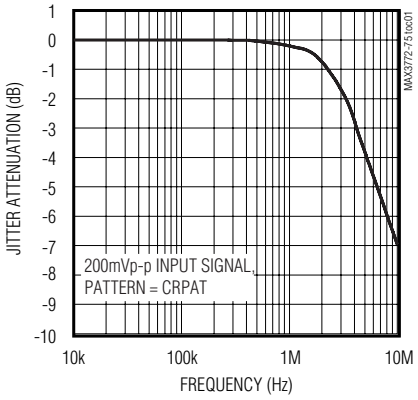
Note 10: Using differential drive over the entire input amplitude range. The input signal bandwidth is limited to 0.75 x (bit-rate) by a 4th-order Bessel Thompson filter or equivalent. Total jitter (TJ) is the range of the eye pattern where the BER exceeds 10^{-12}. TJ can be estimated as TJ = DJ + 14 x RJ. DJ is deterministic jitter. RJ is a one sigma distribution (RMS) of random jitter.

Note 11: Simulation shows peaking of 0.01dB max. Characterization results limited by test equipment.

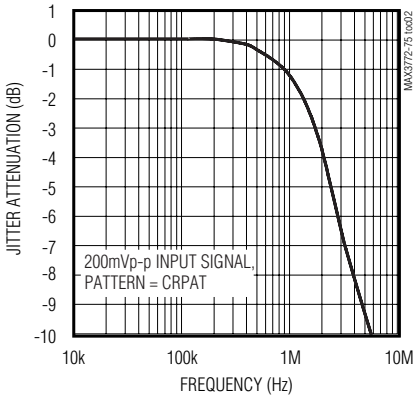
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

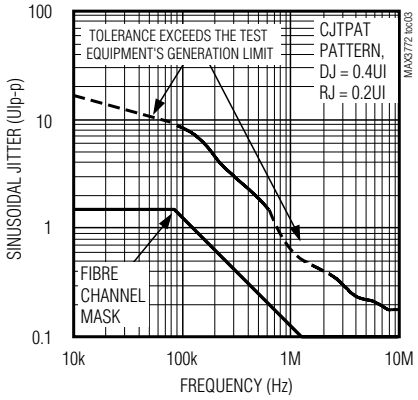
2.125Gbps JITTER TRANSFER vs. FREQUENCY



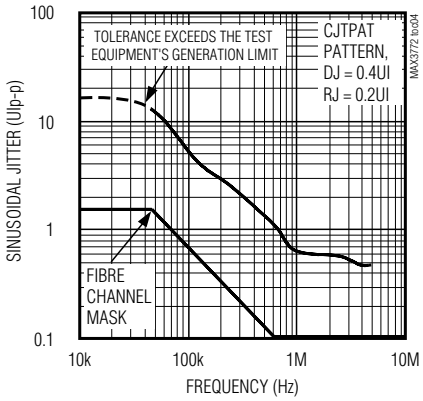
1.0625Gbps JITTER TRANSFER vs. FREQUENCY



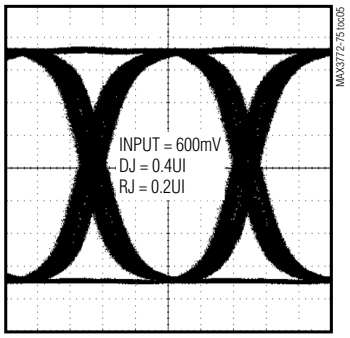
2.125Gbps JITTER TOLERANCE



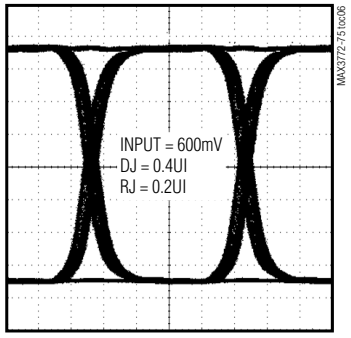
1.0625Gbps JITTER TOLERANCE



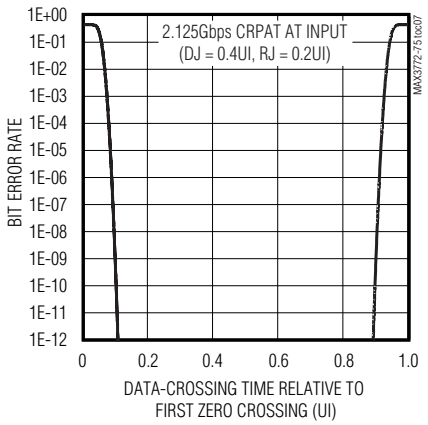
OUTPUT EYE DIAGRAM AT OUT± (2.125Gbps CRPAT)



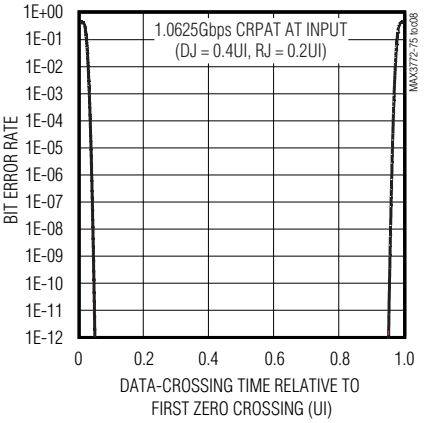
OUTPUT EYE DIAGRAM AT OUT± (1.0625Gbps CRPAT)



2.125Gbps OUTPUT JITTER BATHTUB PLOT



1.0625Gbps OUTPUT JITTER BATHTUB PLOT



Dual-Rate Fibre Channel Repeaters

Pin Description

PIN	NAME	FUNCTION
1	CF+	CDR Filter Capacitor Positive Connection. C_F = 0.047µF.
2	CF-	CDR Filter Capacitor Negative Connection. C_F = 0.047µF.
3, 6, 12	GND	Electrical Ground
4	IN+	Noninverted Data Input
5	IN-	Inverted Data Input
7, 8	V_{CC}	Supply Voltage
9	RATESEL	Rate Select Pin. TTL low selects 1.0625Gbps operation. TTL high selects 2.125Gbps operation.
10	OUT-	Inverted Data Output
11	OUT+	Noninverted Data Output
13	CLKEN	Clock Output Enable. TTL high enables the clock output. TTL low disables the clock output.
14	CLK-	Inverted Clock Output. Enabled when CLKEN is forced high; disabled when CLKEN is forced low.
15	CLK+	Noninverted Clock Output. Enabled when CLKEN is forced high; disabled when CLKEN is forced low.
16	LOCK	Frequency Lock Indicator. When data is present, a high level indicates the PLL is frequency-locked. The output of the LOCK pin may chatter when large jitter is applied to the input.
EP	Exposed Paddle	The exposed paddle must be soldered to the circuit board ground for proper thermal performance.

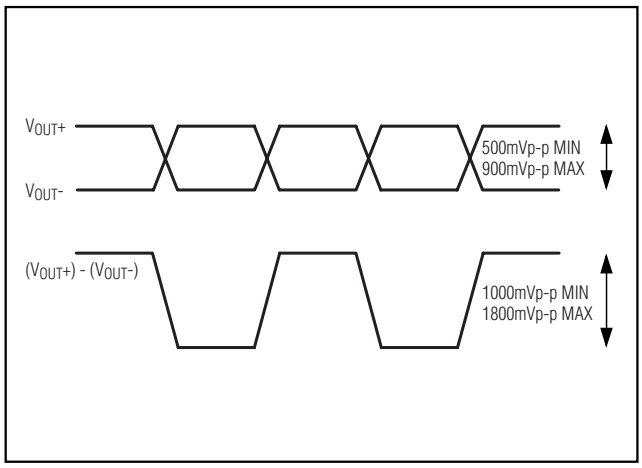


Figure 1. Example of Output Signal with Matched Output Loads

Detailed Description

Figure 2 shows the functional block diagram of the MAX3772–MAX3775 fibre channel repeaters. They consist of a fully integrated PLL, CML input and output buffers, and a data latch. The PLL consists of a combined phase detector (PD) and frequency detector (FD), a loop filter, and a voltage-controlled oscillator (VCO). The input and output signal buffers employ low-noise CML architecture and are terminated on-chip.

Phase and Frequency Detector

The frequency difference between the VCO clock and the received data is derived by sampling the in-phase and quadrature VCO outputs on the edges of the input data signal. The FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the PD produces a voltage proportional to the phase difference between the incoming data and the internal clock. The PLL drives this error voltage to zero, aligning the recovered clock to the center of the incoming eye.

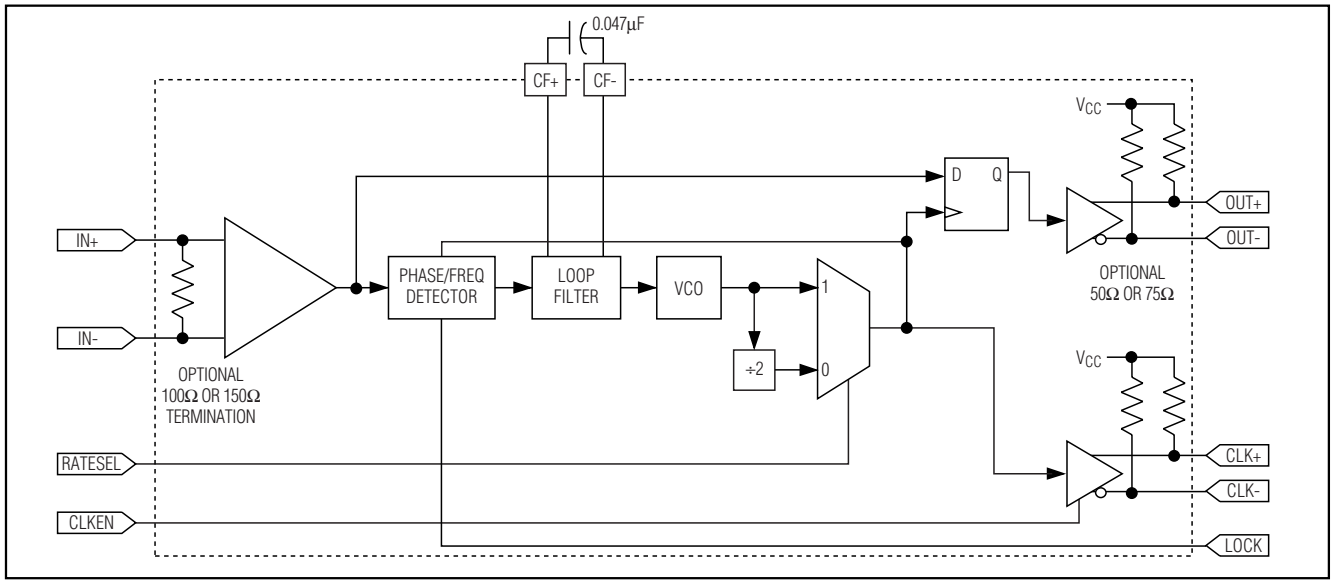


Figure 2. Block Diagram

Loop Filter, VCO, and Latch

The phase detector and frequency detector outputs are summed into a loop filter. An external capacitor (between CF+ and CF-) is required to set the PLL damping factor. The fully integrated VCO contains an internal current reference and filter circuitry to minimize the influence of V_{CC} noise. The VCO creates a clock output with frequency proportional to the control voltage applied by the loop filter. Data recovery is accomplished by using the recovered clock signal to latch the incoming data to the CML output buffers, significantly reducing output jitter.

LOCK Output

An active high LOCK output monitor derived from the frequency detector indicates that the PLL is frequency-locked onto the input data. Without input data, the LOCK signal may settle high or low. The use of a low-pass RC filter is recommended to reduce the effects of chatter that could be caused by high input-jitter content. For optimum jitter performance, keep the load ≥ 15kΩ on the output of the LOCK pin.

RATESEL Input

The RATESEL input is used to select between input data rates of 2.125Gbps and 1.0625Gbps. This function allows the repeater to sample data at the correct data rate by selecting a divide-by-2 network, giving maximum jitter tolerance at both data rates. The loop bandwidth of the repeater scales with the selected frequency; i.e., the loop-bandwidth at an input rate of 1.0625Gbps is half that at the input rate of 2.125Gbps. See the *Applications Information* section for the functionality of the RATESEL pin.

Applications Information

Input and Output Terminations

Figures 3 and 4 show models for the MAX3772–MAX3775 inputs and outputs, including packaging parasitics.

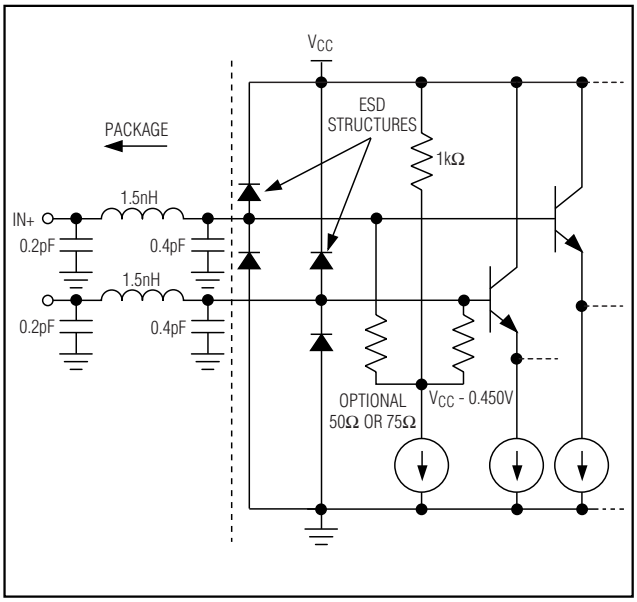


Figure 3. Input Structure

Dual-Rate Fibre Channel Repeaters

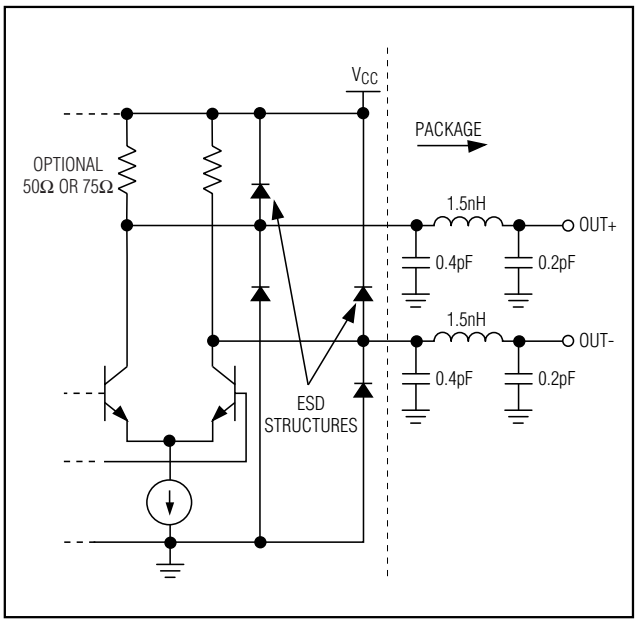


Figure 4. Output Structure

Control Functions

The MAX3772–MAX3775 have two control inputs: RATESEL and CLKEN.

RATESEL is an input that sets the operational data rate for the repeaters. Table 1 shows the selected input data rates when using the RATESEL function.

CLKEN is an input that can be used to enable or disable the output clock, as shown in Table 2.

Table 1. Input Data Rate Using RATESEL Function

RATESEL LEVEL	DATA RATE SELECTED
GND	1.0625Gbps
V_{CC}	2.125Gbps

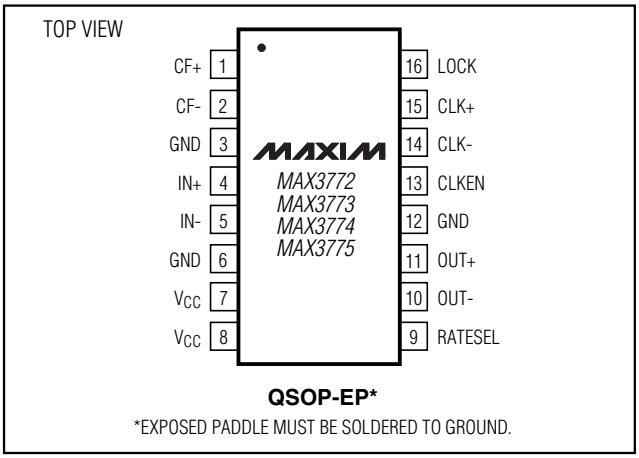
Table 2. CLKEN Function

CLKEN LEVEL	CLOCK OUTPUT
GND	Disabled
V_{CC}	Enabled

Layout Procedure

The MAX3772–MAX3775 performance can be greatly affected by circuit-board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. All IN, OUT, and CLK pins should be connected with 0.1µF coupling capacitors equivalent or better than X5R. A 0.047µF capacitor should be used for the loop filter. If DC coupling is desired pay particular attention to the DC voltage and current requirements at the pins of interest (see *DC Electrical Characteristics*). The MAX3750/MAX3754/MAX3755 port bypass circuits can be DC-coupled to the Maxim dual-rate repeaters. The exposed paddle of the repeater must be connected to ground and should be soldered onto the circuit board for optimal thermal and electrical operation.

Pin Configuration



QSOP-EP*

*EXPOSED PADDLE MUST BE SOLDERED TO GROUND.

Selector Guide

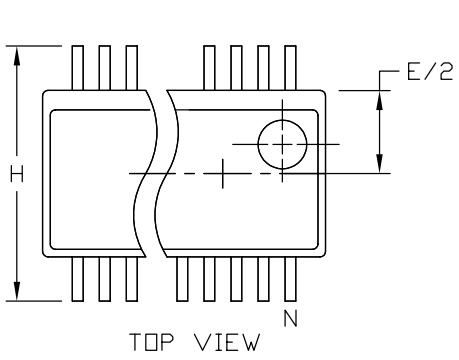
PART	DIFFERENTIAL INPUT TERMINATION	DIFFERENTIAL OUTPUT TERMINATION
MAX3772CEE	100Ω	100Ω
MAX3773CEE	150Ω	100Ω
MAX3774CEE	100Ω	150Ω
MAX3775CEE	150Ω	150Ω

Chip Information

TRANSISTOR COUNT: 1280

PROCESS: Si

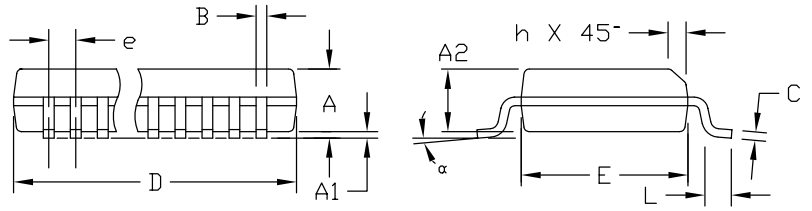
Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.084	.108	2.13	2.74
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.078	.102	1.98	2.59	EXPOSED PAD	



NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006″ PER SIDE.
3. DIMENSIONS X AND Y APPLY ONLY TO EXPOSED PAD QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 16L QSOP, .150″ EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0112	B	1/1