19-1697; Rev 1; 8/00

MAXIM

2.75Gbps Dual Mux/Buffer

General Description

The MAX3781 is a 2.75Gbps dual multiplexer (mux) and buffer. Each half of the MAX3781 has a transmitter with a fanout of two and a receiver with a 2:1 mux.

Operating from a single +3.3V supply, this device accepts CML or AC-coupled PECL inputs and provides CML outputs. The outputs can be AC-coupled for compatibility with PECL inputs if needed. The MAX3781 is packaged in a compact 48-pin 7x7mm TQFP exposed-paddle package and typically consumes 1.2W power. A power-saving mode disables the unused buffer output and reduces typical power to 0.9W.

Applications

System Interconnect Redundancy

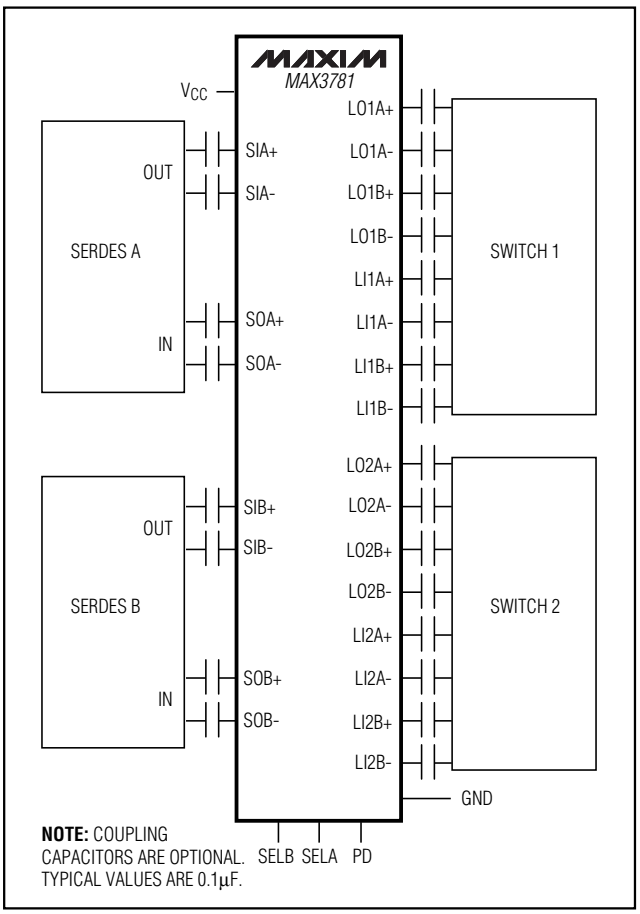
Serial Backplane Redundancy

2.75Gbps Serial Communications

Features

- **11ps Deterministic Jitter**
- **On-Chip Termination Resistors Compatible with 50Ω Transmission Lines at All Ports**
- **1.2W Power Consumption (0.9W in Power-Saving Mode)**
- **+3.3V Power Supply**
- **Two-Port Integration**

Typical Application Circuit

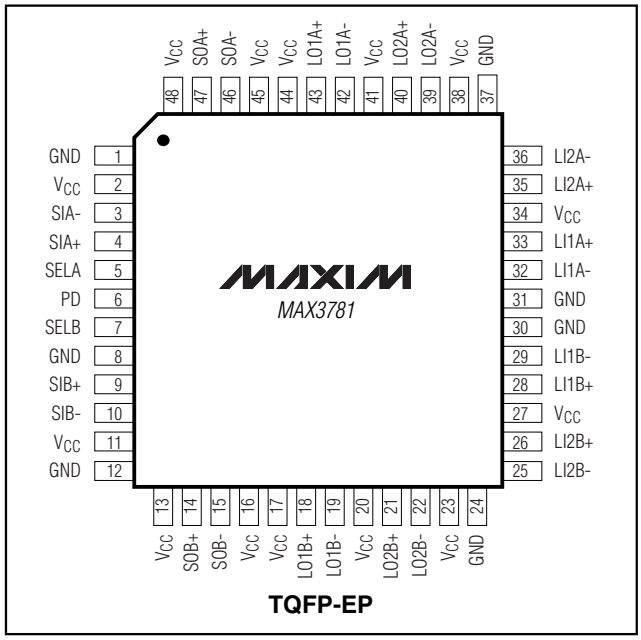


Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3781UCM	0°C to +85°C	48 TQFP-EP*

**EP = Exposed paddle*

Pin Configuration



TQFP-EP

2.75Gbps Dual Mux/Buffer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VCC .....-0.5 to +4.0V
Continuous Current at Serial Outputs
(SO_, LO_ _ Pins) .....±36mA
Voltage at SELA, SELB, PD Pins .....-0.5V to (V_{CC} + 0.5V)
Common-Mode Input Voltage
(SI_, LI_ _ Pins).....-0.5V to (V_{CC} + 0.5V)
Differential Input Voltage (Note 1) .....±2.8V
Continuous Power Dissipation (T_A = +85°C)
48-Pin TQFP-EP (derate 27mW/°C above +85°C).....1.76W
Operating Temperature Range..... 0°C to +85°C
Storage Temperature Range .....-55C° to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: The sum of the common-mode voltage and differential voltage on any input pin should be within -0.5V to (V_{CC} + 0.5V).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_{LOAD} = 100Ω differential, data rate = 2.75Gbps, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +3.3V.)

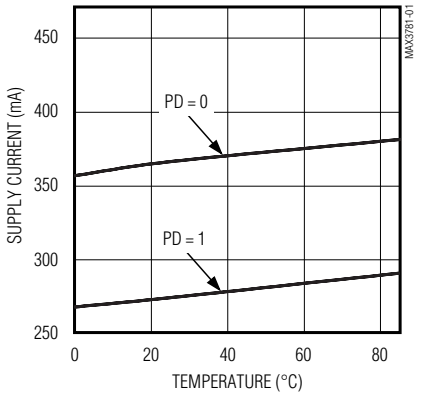
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Data Rate			0	2750		Mbps
Power Dissipation		PD = low		1.2	1.53	W
		PD = high		0.9	1.14	
Supply Current		PD = low		365	425	mA
		PD = high		273	316	
Differential Output Voltage	V_{OUT}	R_L= 50Ω to V_{CC}, or 100Ω differential	1200	1600	2200	mV_{P-P}
Output Impedance	R_{OUT}	Single ended	42.5	50	57.5	Ω
Input Impedance	R_{IN}	Differential	85	100	116	Ω
Differential Input Voltage	V_{IN}		200		2200	mV_{P-P}
Random Jitter				1	2	ps_{RMS}
Deterministic Jitter		K28.5 pattern (Note 2)		11	25	ps_{P-P}
Serial Output Edge Speed (20%–80%)	t_r, t_f	2.75Gbps input		90	135	ps
		1.25Gbps input		90	200	
Progagation Delay				275	500	ps
TTL Input Current High		V_{IH} = +2.0V to (V_{CC} + 0.3V)			180	µA
TTL Input Current Low		V_{IL} = -0.3V to +0.8V			410	µA

Note 2: Deterministic jitter is measured with a repeating K28.5 pattern (00111110101100000101).

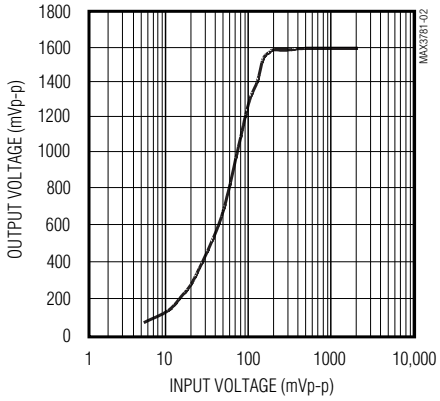
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

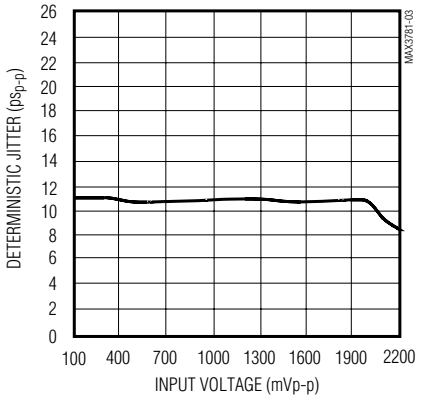
SUPPLY CURRENT vs. TEMPERATURE



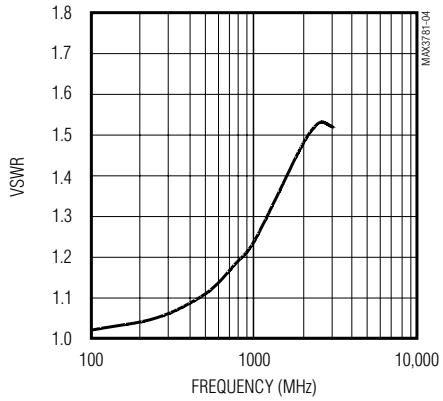
DIFFERENTIAL OUTPUT VOLTAGE vs. DIFFERENTIAL INPUT VOLTAGE



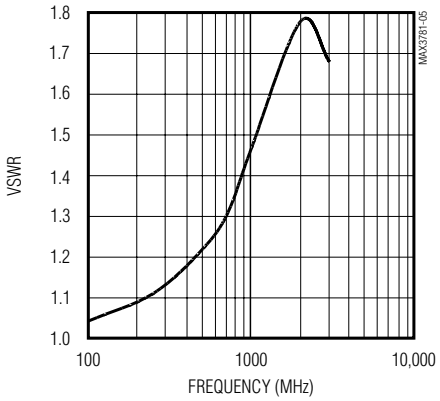
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



INPUT VSWR (BY SIMULATION)



OUTPUT VSWR (BY SIMULATION)



2.75Gbps Dual Mux/Buffer

Pin Description

PIN	NAME	FUNCTION
1, 8, 12, 24, 30, 31, 37	GND	Ground
2, 11, 13, 16, 17, 20, 23, 27, 34, 38, 41, 44, 45, 48	V_{CC}	Power
3	SIA-	Serial Input A Negative
4	SIA+	Serial Input A Positive
5	SELA	Select Line A. Set high to select channel 1; set low for channel 2 (internally pulled high).
6	PD	Power-Down Mode Select. Set high for power-down mode (internally pulled high).
7	SELB	Select Line B. Set high to select channel 1; set low for channel 2 (internally pulled high).
9	SIB+	Serial Input B Positive
10	SIB-	Serial Input B Negative
14	SOB+	Serial Output B Positive
15	SOB-	Serial Output B Negative
18	LO1B+	Line Output 1B Positive
19	LO1B-	Line Output 1B Negative
21	LO2B+	Line Output 2B Positive
22	LO2B-	Line Output 2B Negative
25	LI2B-	Line Input 2B Negative
26	LI2B+	Line Input 2B Positive
28	LI1B+	Line Input 1B Positive
29	LI1B-	Line Input 1B Negative
32	LI1A-	Line Input 1A Negative
33	LI1A+	Line Input 1A Positive
35	LI2A+	Line Input 2A Positive
36	LI2A-	Line Input 2A Negative
39	LO2A-	Line Output 2A Negative
40	LO2A+	Line Output 2A Positive
42	LO1A-	Line Output 1A Negative
43	LO1A+	Line Output 1A Positive
46	SOA-	Serial Output A Negative
47	SOA+	Serial Output A Positive
EP	Exposed Paddle	Ground. This must be soldered to a circuit board for proper thermal performance (see *Exposed Paddle (EP) Package*).

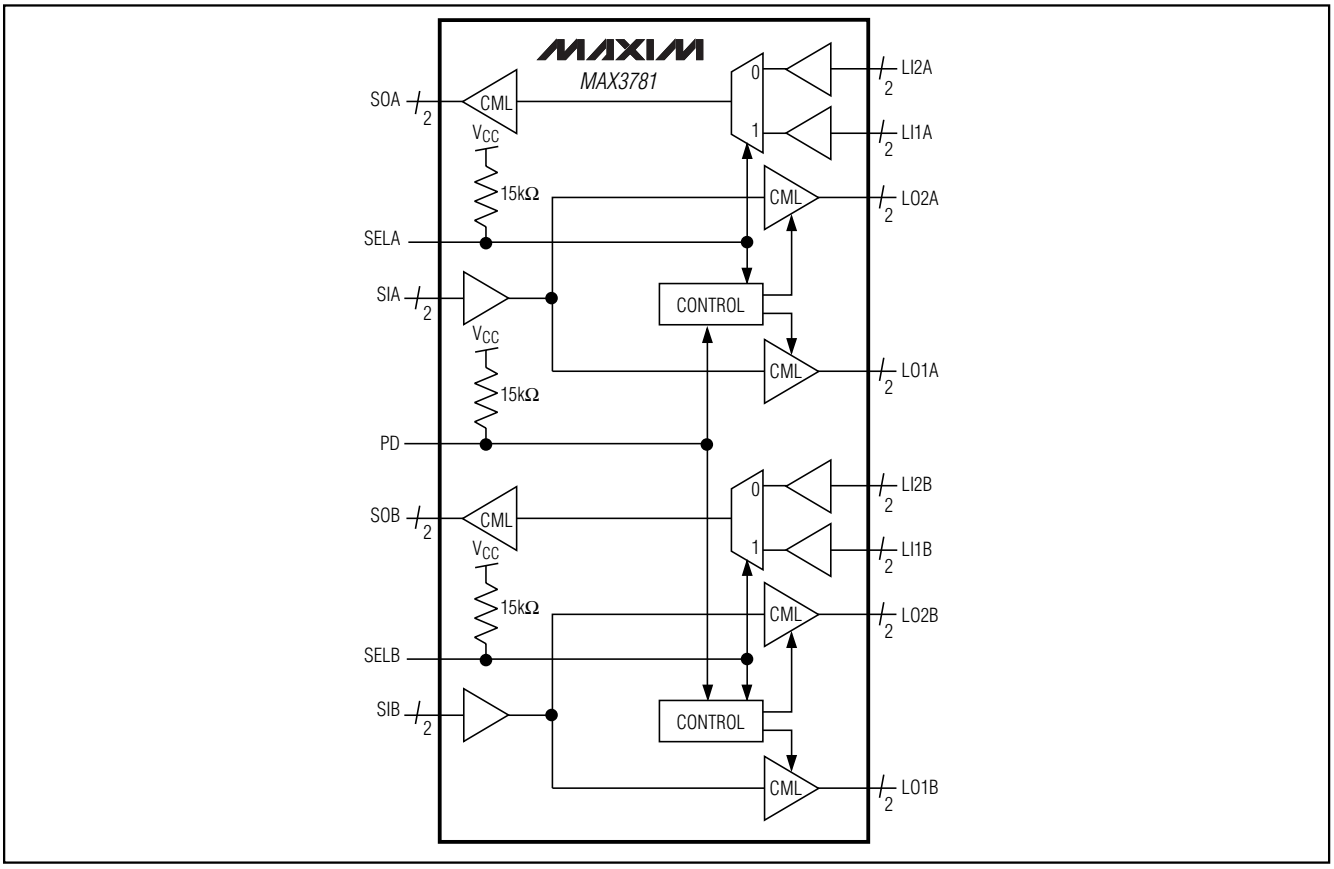


Figure 1. Functional Diagram

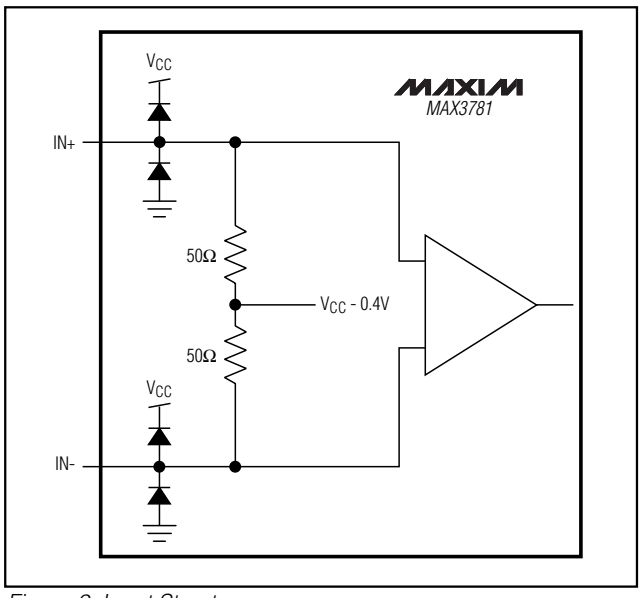


Figure 2. Input Structure

Detailed Description

The MAX3781 is a 2.75Gbps dual mux/buffer. Each half of the MAX3781 has a transmitter with a fanout of two and a receiver with a 2:1 mux. Figure 1 is a functional diagram of the MAX3781 dual mux/buffer.

Input Stages

The input amplifiers accept CML or AC-coupled PECL signals and have an on-chip 100Ω differential impedance to simplify termination. The input structure is shown in Figure 2.

2.75Gbps Dual Mux/Buffer

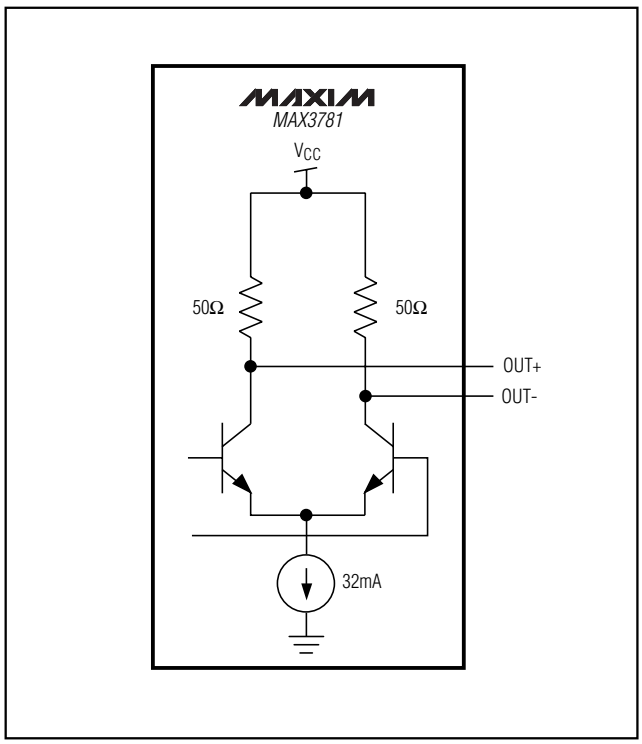


Figure 3. CML Output Structure

Table 1. Operating Modes

SEL_	PD	LO1_	LO2_	SO_
0	0	SI_	SI_	LI2_
0	1	–	SI_	LI2_
1	0	SI_	SI_	LI1_
1	1	SI_	–	LI1_

Control Lines

TTL-compatible control lines are provided to select the MAX3781's operating mode (Table 1). SELA and SELB select the data routing in to and out of the chip. The PD pin may be asserted (high) to disable the unused output to save power. All control lines are internally pulled high through 15kΩ resistors.

Output Buffers

The outputs are high-speed CML interfaces. They have 50Ω back termination, eliminating the need for external matching resistors. The output structure is shown in Figure 3.

Exposed-Paddle (EP) Package

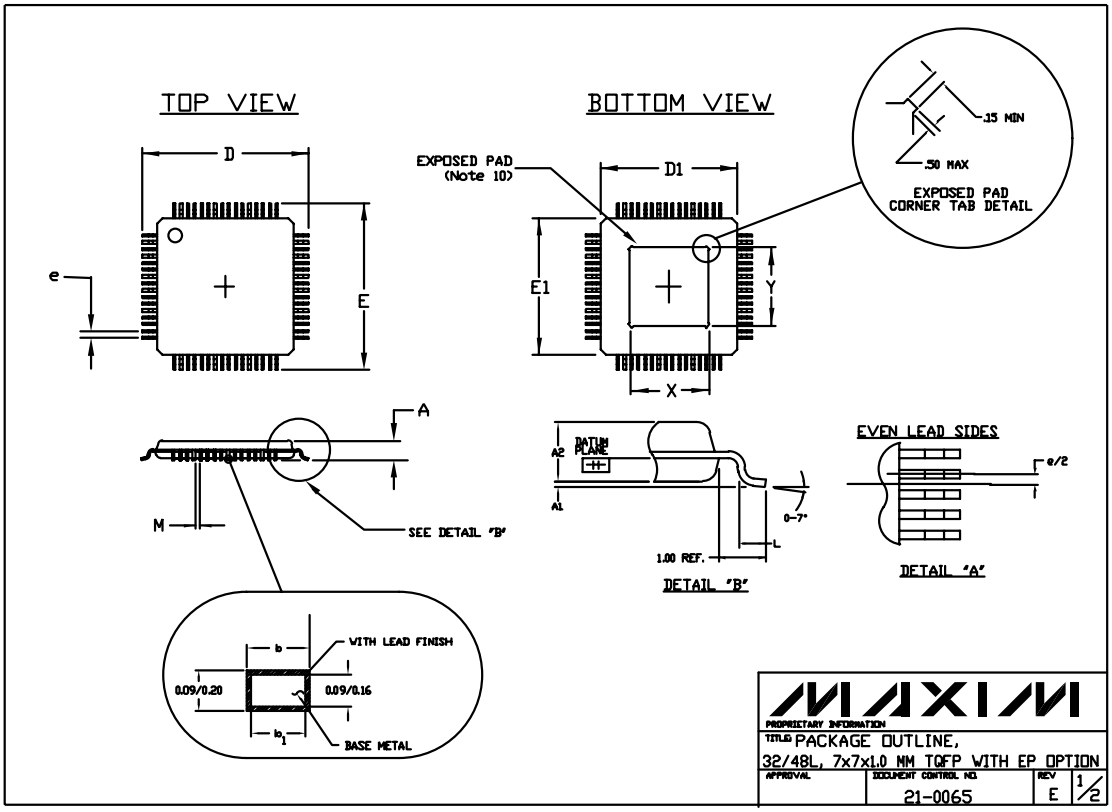
The exposed-paddle, 48-pin TQFP-EP incorporates features that provide a very low thermal resistance path for heat removal from the IC. The paddle is electrical ground on the MAX3781 and should be soldered to the circuit board for proper thermal and electrical performance.

Chip Information

TRANSISTOR COUNT: 2805

PROCESS: BIPOLAR

Package Information



Package Information (continued)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D		9.00 BSC.			9.00 BSC.	
D_1		7.00 BSC.			7.00 BSC.	
E		9.00 BSC.			9.00 BSC.	
E_1		7.00 BSC.			7.00 BSC.	
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15	—	—	0.14	—	—
N		32			48	
e		0.80 BSC.			0.50 BSC.	
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.0 MM TQFP WITH EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0065	E	2/2