19-4194; Rev 2; 11/96

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

General Description

The MAX410/MAX412/MAX414 single/dual/quad op amps set a new standard for noise performance in high-speed, low-voltage systems. Input voltage-noise density is guaranteed to be less than 2.4nV/√Hz at 1kHz. A unique design not only combines low noise with ±5V operation, but also consumes 2.5mA supply current per amplifier. Low-voltage operation is guaranteed with an output voltage swing of $7.3V_{P-P}$ into 2kΩ from ±5V supplies. The MAX410/MAX412/MAX414 also operate from supply voltages between ±2.4V and ±5V for greater supply flexibility.

Unity-gain stability, 28MHz bandwidth, and 4.5V/µs slew rate ensure low-noise performance in a wide variety of wideband and measurement applications. The MAX410/MAX412/MAX414 are available in DIP and SO packages in the industry-standard single/dual/quad op-amp pin configurations.

Applications

Low-Noise Frequency Synthesizers

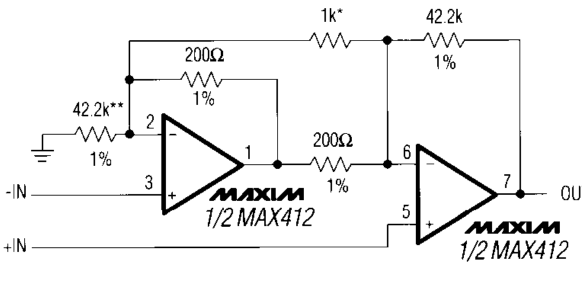
Infrared Detectors

High-Quality Audio Amplifiers

Ultra Low-Noise Instrumentation Amplifiers

Bridge Signal Conditioning

Typical Operating Circuit



* TRIM FOR GAIN
** TRIM FOR COMMON-MODE REJECTION

LOW-NOISE INSTRUMENTATION AMPLIFIER

Features

- ♦ **Voltage Noise: 2.4nV/√Hz Max at 1kHz**
- ♦ **2.5mA Supply Current Per Amplifier**
- ♦ **Low Supply Voltage Operation: ±2.4V to ±5V**
- ♦ **28MHz Unity-Gain Bandwidth**
- ♦ **4.5V/µs Slew Rate**
- ♦ **250µV Max Offset Voltage (MAX410/MAX412)**
- ♦ **115dB Min Voltage Gain**

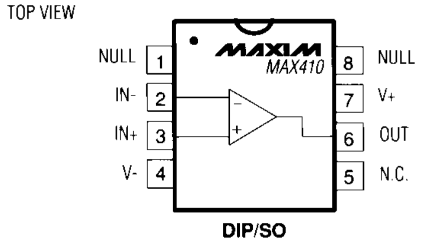
Ordering Information

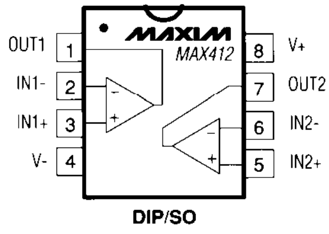
PART	TEMP. RANGE	PIN-PACKAGE
MAX410CPA	0°C to +70°C	8 Plastic DIP
MAX410BCPA	0°C to +70°C	8 Plastic DIP
MAX410CSA	0°C to +70°C	8 SO
MAX410BCSA	0°C to +70°C	8 SO
MAX410C/D	0°C to +70°C	Dice*
MAX410EPA	-40°C to +85°C	8 Plastic DIP
MAX410BEPA	-40°C to +85°C	8 Plastic DIP
MAX410ESA	-40°C to +85°C	8 SO
MAX410BESA	-40°C to +85°C	8 SO
MAX410MJA	-55°C to +125°C	8 CERDIP
MAX410BMJA	-55°C to +125°C	8 CERDIP

Ordering Information continued at end of data sheet.

* *Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations





Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-)	12V
Differential Input Current (Note 1)	±20mA
Input Voltage Range	V+ to V-
Common-Mode Input Voltage	(V+ + 0.3V) to (V- - 0.3V)
Short-Circuit Current Duration	Continuous
Continuous Power Dissipation (T_A = +70°C)	
MAX410/MAX412	
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C)	640mW
MAX414	
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	800mW
14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C)	727mW
Operating Temperature Ranges:	
MAX41_C _ _	0°C to +70°C
MAX41_E _ _	-40°C to +85°C
MAX41_MJ_	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1.0V are applied, limit input current to 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B			±120	±250	µV
		MAX414, MAX414B			±150	±320	
Input Bias Current	I_B				±80	±150	nA
Input Offset Current	I_{OS}				±40	±80	nA
Differential Input Resistance	R_{IN}(Diff)				20		kΩ
Common-Mode Input Resistance	R_{IN}(CM)				40		MΩ
Input Capacitance	C_{IN}				4		pF
Input Noise-Voltage Density	e_n	MAX410, MAX412, MAX414	10Hz		7		nV/√Hz
			1000Hz (Note 2)		1.8	2.4	
		MAX410B, MAX412B, MAX414B	1000Hz (Note 3)		2.4	4.0	
Input Noise-Current Density	i_n	f_o = 10Hz			2.6		pA/√Hz
		f_o = 1000Hz			1.2		
Common-Mode Input Voltage	V_{CM}			±3.5	+3.7/ -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V		115	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V		96	103		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_o = 3.6V to -3.7V		115	122		dB
		R_L = 600Ω, V_o = ±3.5V		110	120		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ		+3.6/ -3.7	+3.7/ -3.8		V
Short-Circuit Output Current	I_{SC}				35		mA
Slew Rate	SR	10kΩ ll 20pF load			4.5		V/µs
Unity-Gain Bandwidth	GBW	10kΩ ll 20pF load			28		MHz
Settling Time	t_S	To 0.1%			1.3		µs
Channel Separation	CS	f_o = 1kHz			135		dB
Operating Supply-Voltage Range	V_S			±2.4		±5.25	V
Supply Current	I_S	Per amplifier			2.5	2.7	mA

Note 2: Sample tested to 0.1% AQL.

Note 3: Guaranteed by design.

ELECTRICAL CHARACTERISTICS

($V+ = 5V$, $V- = -5V$, $T_A = 0°C$ to $+70°C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±150	±350	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±100	±200	nA
Input Offset Current	I_{OS}			±80	±150	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.8		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm3.5V$	105	121		dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm2.4V$ to $\pm5.25V$	90	97		dB
Large-Signal Gain	A_{VOL}	$R_L = 2k\Omega$, $V_O = \pm3.6V$	110	120		dB
		$R_L = 600\Omega$, $V_O = \pm3.5V$	90	119		
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.6	±3.7		V
Supply Current	I_S	Per amplifier			3.3	mA

ELECTRICAL CHARACTERISTICS

($V+ = 5V$, $V- = -5V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted.)

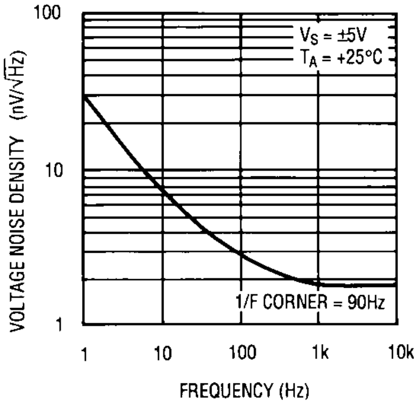
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B		±200	±400	µV
		MAX414, MAX414B		±200	±450	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.6		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm3.5V$	105	120		dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm2.4V$ to $\pm5.25V$	90	94		dB
Large-Signal Gain	A_{VOL}	$R_L = 2k\Omega$, $V_O = \pm3.5V$	110	118		dB
		$R_L = 600\Omega$, $V_O = 3.4V$ to $-3.5V$	90	114		
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.5	+3.7/ -3.6		V
Supply Current	I_S	Per amplifier			3.3	mA

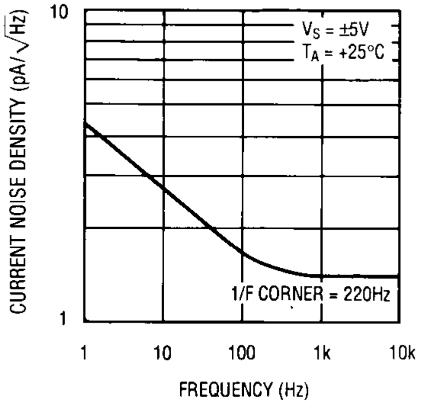
ELECTRICAL CHARACTERISTICS

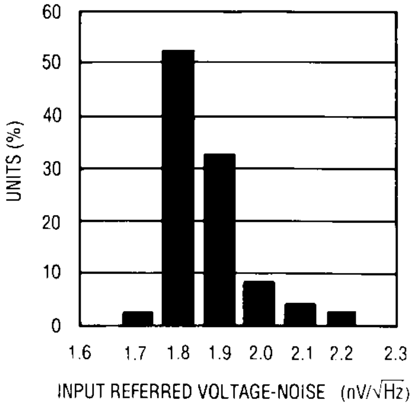
($V+ = 5V$, $V- = -5V$, $T_A = -55°C$ to $+125°C$, unless otherwise noted.)

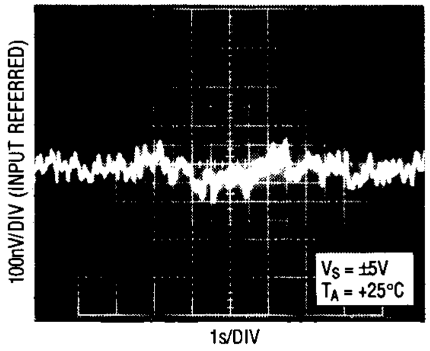
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B		±200	±400	µV
		MAX414, MAX414B		±200	±500	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.6		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm3.5V$	105	120		dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm2.4V$ to $\pm5.25V$	90	94		dB
Large-Signal Gain	A_{VOL}	$R_L = 2k\Omega$, $V_O = \pm3.5V$	110	118		dB
		$R_L = 600\Omega$, $V_O = 3.4V$ to $-3.5V$	90	114		
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	æ3.5	+3.7/ -3.6		V
Supply Current	I_S	Per amplifier			3.5	mA

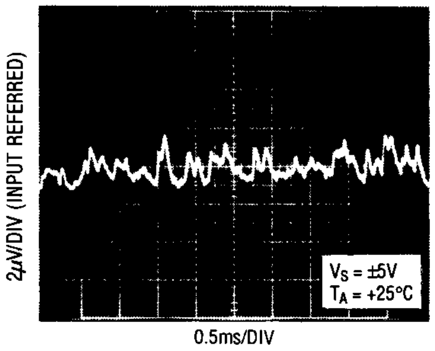
Typical Operating Characteristics


VOLTAGE NOISE DENSITY vs. FREQUENCY


CURRENT NOISE DENSITY vs. FREQUENCY

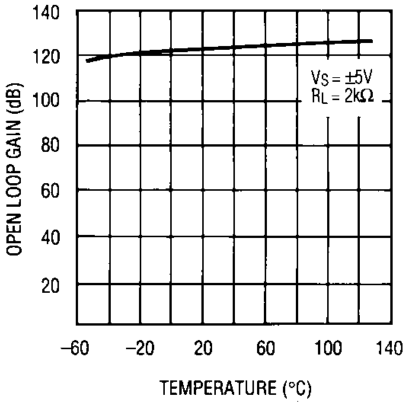

1kHz VOLTAGE NOISE DISTRUBUTION


0.1Hz TO 10Hz VOLTAGE NOISE

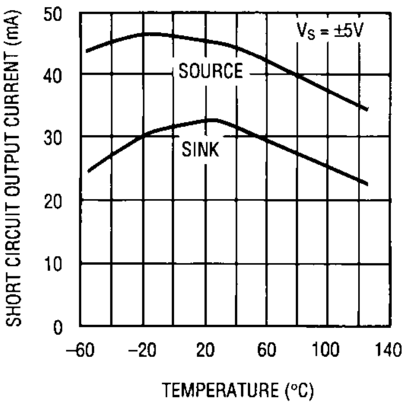

WIDEBAND NOISE DC TO 20kHz

Typical Operating Characteristics (continued)

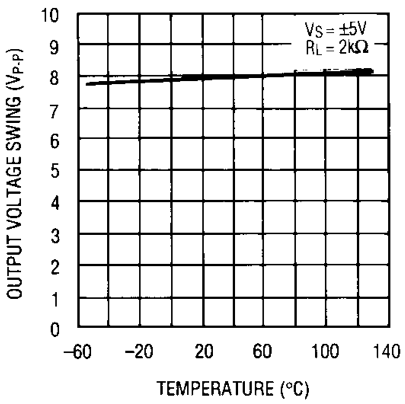
OPEN LOOP GAIN vs. TEMPERATURE



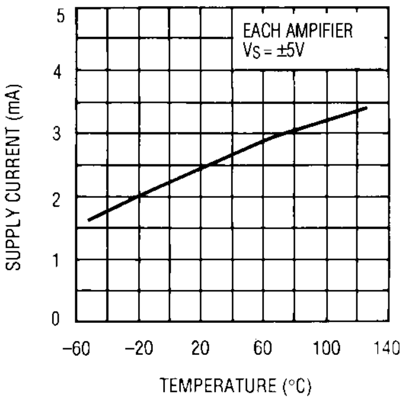
SHORT CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



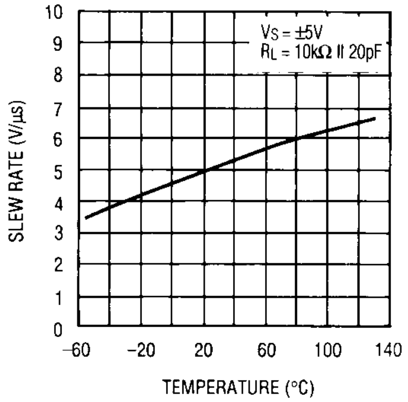
OUTPUT VOLTAGE SWING vs. TEMPERATURE



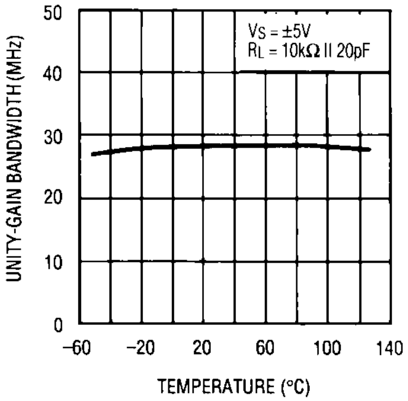
SUPPLY CURRENT vs. TEMPERATURE



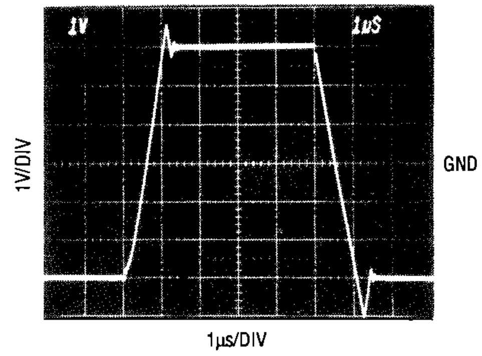
SLEW RATE vs. TEMPERATURE



UNITY-GAIN BANDWIDTH vs. TEMPERATURE

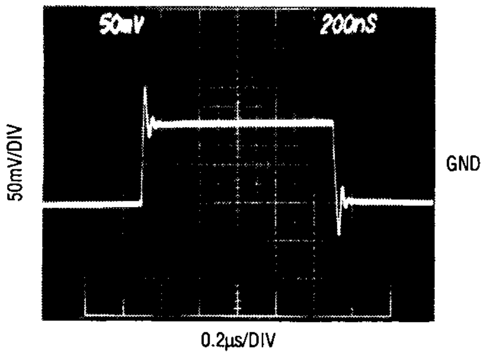


LARGE-SIGNAL TRANSIENT RESPONSE



AV = +1, RF = 499Ω, RL = 2kΩ II 20pF
VS = ±5V, TA = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE

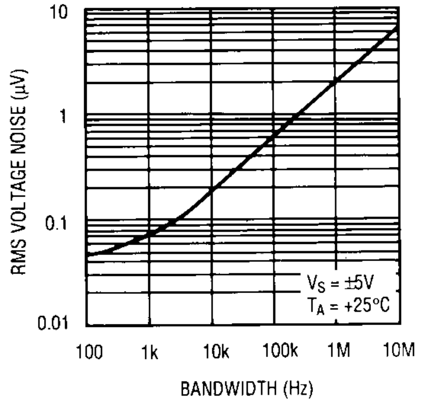


AV = +1, RF = 200Ω, RL = 2kΩ II 20pF
VS = ±5V, TA = +25°C

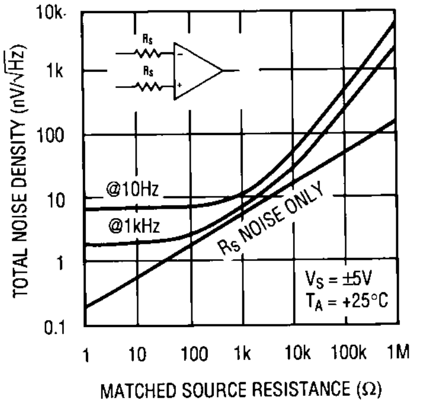
Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

Typical Operating Characteristics (continued)

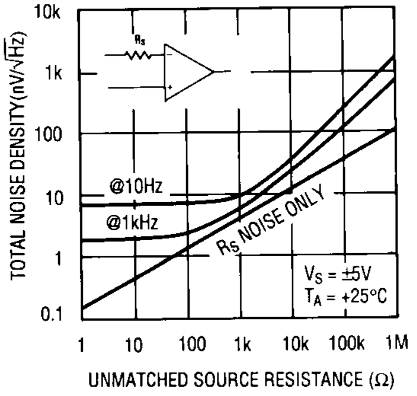
WIDEBAND VOLTAGE NOISE (0.1Hz TO FREQUENCY INDICATED)



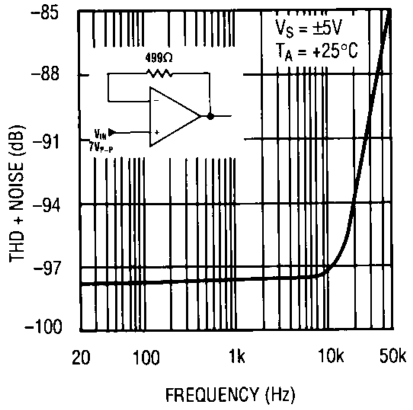
TOTAL NOISE DENSITY vs. MATCHED SOURCE RESISTANCE



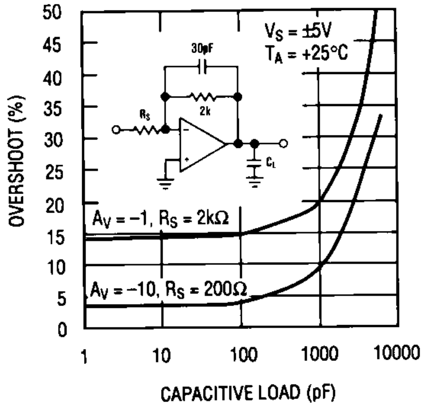
TOTAL NOISE DENSITY vs. UNMATCHED SOURCE RESISTANCE



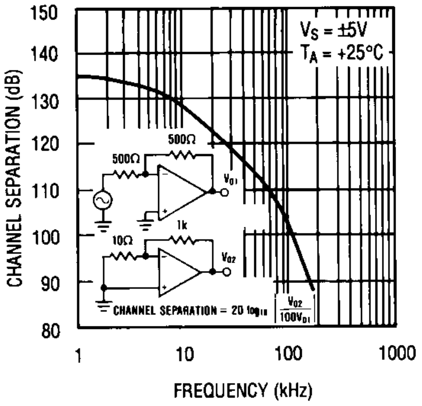
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



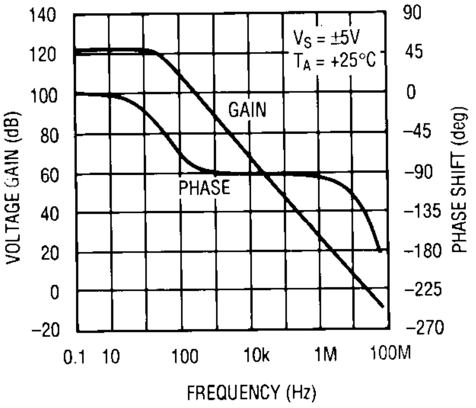
PERCENTAGE OVERSHOOT vs. CAPACITIVE LOAD



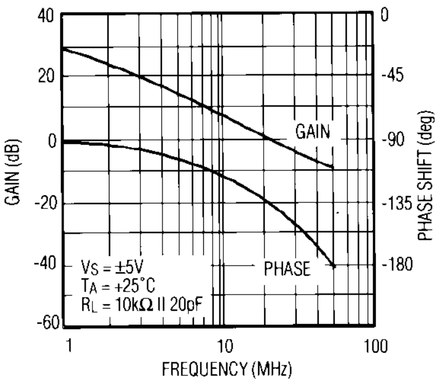
MAX412, MAX414 CHANNEL SEPARATION vs. FREQUENCY



GAIN, PHASE vs. FREQUENCY



GAIN, PHASE vs. FREQUENCY



Applications Information

The MAX410/MAX412/MAX414 provide low voltage noise performance. Obtaining low voltage noise from a bipolar op amp requires high collector currents in the input stage, since voltage noise is inversely proportional to the square root of the input stage collector current. However, op amp current noise is proportional to the square root of the input stage collector current, and input bias current is proportional to input stage collector current. Therefore, to obtain optimum low noise performance, DC accuracy, and AC stability, minimize the value of the feedback and source resistance.

Total Noise Density vs.Source Resistance

The standard expression for the total input referred noise of an op amp at a given frequency is:

$$e_t = \sqrt{e_n{}^2 + (R_p + R_n)^2\, i_n{}^2 + 4kT\,(R_p + R_n)}$$

Where:

R_n = Inverting input effective series resistance

R_p = Noninverting input effective series resistance

e_n = Input voltage noise density at the frequency of interest

i_n = Input current noise density at the frequency of interest

T = Ambient temperature in Kelvin (K)

k = 1.38×10^{-23}J/K (Boltzman's constant).

In Figure 1, R_p = R3 and R_n = R1 II R2. In a real application, the output resistance of the source driving the input must be included with Rp and Rn. The following example demonstrates how to calculate the total output noise density at a frequency of 1kHz for the MAX412 circuit in Figure 1.

Gain = 1000

4kT at +25°C = 1.64×10^{-20}

R_p = 100Ω

R_n = 100Ω II 100kΩ = 99.9Ω

e_n = 1.8nV/$\sqrt{\text{Hz}}$ at 1kHz

i_n = 1.2pA/$\sqrt{\text{Hz}}$ at 1kHz

$$e_t = \left[(1.8 \times 10^{-9})^2 + (100 + 99.9)^2\,(1.2 \times 10^{-12})^2 + (1.64 \times 10^{-20})\,(100 + 99.9)\right]^{1/2} = 2.56\text{nV}/\sqrt{\text{Hz}} \text{ at } 1\text{kHz}$$

Output noise density = $(1000)e_t$ = 2.56µV/$\sqrt{\text{Hz}}$at1kHz.

In general, the amplifier's voltage noise dominates with equivalent source resistances less than 200Ω. As the equivalent source resistance increases, resistor noise becomes the dominant term, eventually making the voltage noise contribution from the MAX410/MAX412/MAX414 negligible. As the source resistance is further increased, current noise becomes dominant. For example, when the equivalent source resistance is greater than 3kΩ at 1kHz, the current noise component is larger than the resistor noise. The graph of Total Noise Density vs. Matched Source Resistance in the *Typical Operating Characteristics* shows this phenomenon. Optimal MAX410/MAX412/MAX414 noise performance and minimum total noise is achieved with an equivalent source resistance of less than 10k.

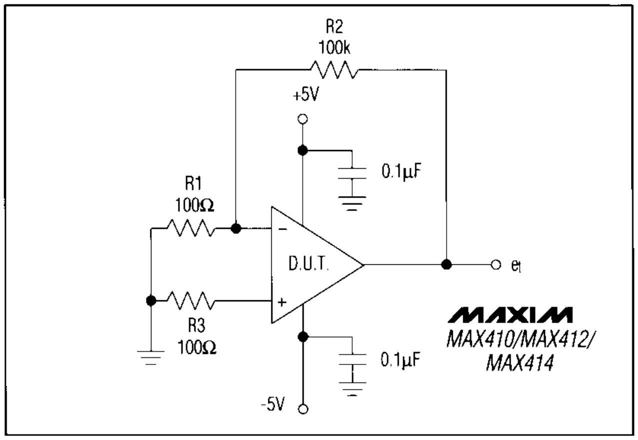


Figure 1. Total Noise vs. Source Resistance Example

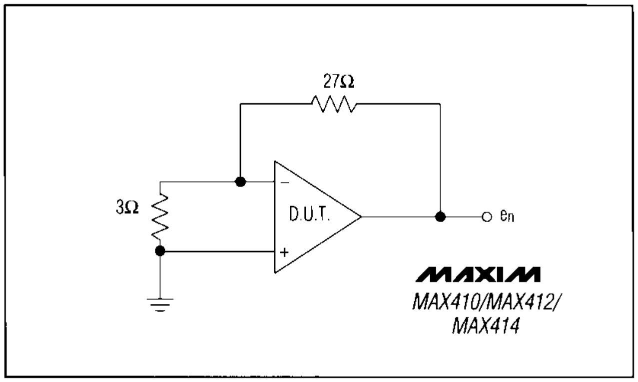


Figure 2. Voltage Noise Density Test Circuit

Voltage Noise Testing

RMS voltage noise density is measured with the circuit shown in Figure 2, using the Quan Tech model 5173 noise analyzer, or equivalent. The voltage noise density at 1kHz is sample tested on production units. When measuring op amp voltage noise, only low-value, metal film resistors are used in the test fixture.

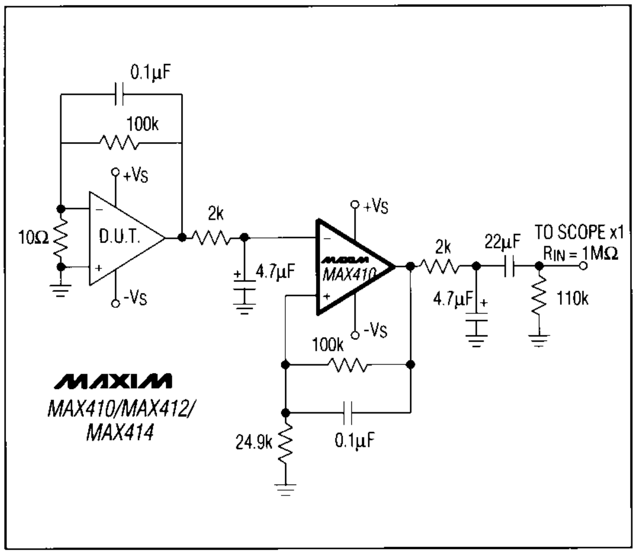


Figure 3. 0.1Hz to 10Hz Voltage Noise Test Circuit

The 0.1Hz to 10Hz peak-to-peak noise of the MAX410/MAX412/MAX414 is measured using the test circuit shown in Figure 3. Figure 4 shows the frequency response of this circuit. The test time for the 0.1Hz to 10Hz noise measurement should be limited to 10 seconds, which has the effect of adding a second zero to the test circuit, providing increased attenuation for frequencies below 0.1Hz.

Current Noise Testing

The current noise density can be calculated, once the value of the input-referred noise is determined, by using the standard expression given below:

$$i_n = \frac{\sqrt{e_{no}{}^2 - [(A_{VCL})^2(4kT)(R_n + R_p)]}}{(R_n + R_p)(A_{VCL})} \; A/\sqrt{Hz}$$

Where:

R_n = Inverting input effective series resistance

R_p = Noninverting input effective series resistance

e_{no} = Output voltage noise density at the frequency of interest (V/$\sqrt{Hz}$)

i_n = Input current noise density at the frequency of interest (A/$\sqrt{Hz}$)

A_{VCL} = Closed-loop gain

T = Ambient temperature in Kelvin (K)

k = 1.38 x 10^{-23}J/K (Boltzman's constant).

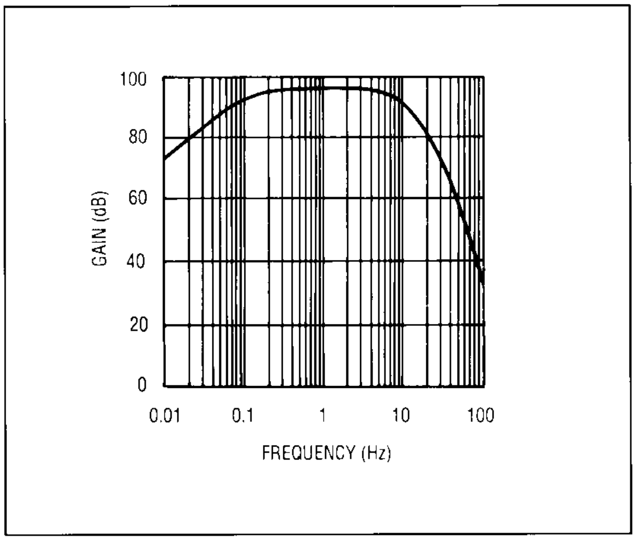


Figure 4. 0.1Hz to 10Hz Voltage Noise Test Circuit, Frequency Response

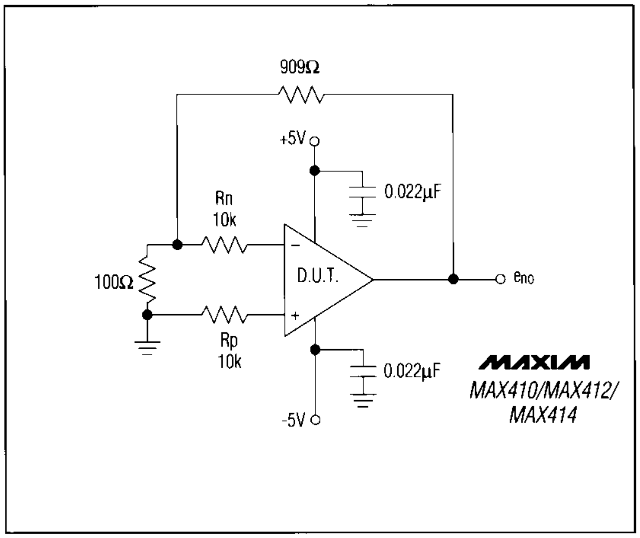


Figure 5. Current Noise Test Circuit

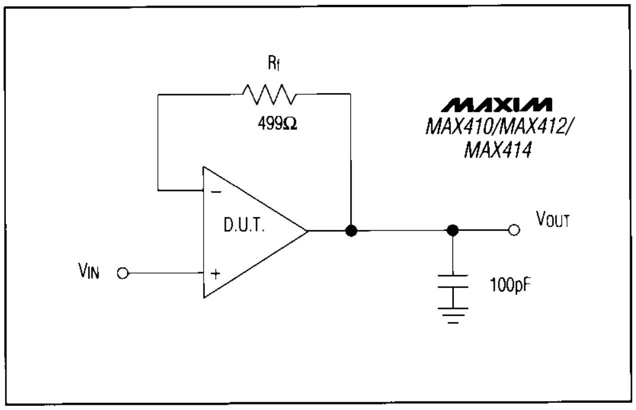


Figure 6a. Voltage Follower Circuit with 100pF Load

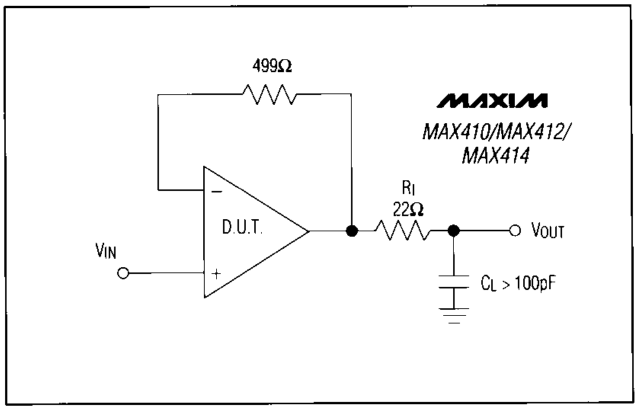


Figure 7a. Capacitive Load Driving Circuit

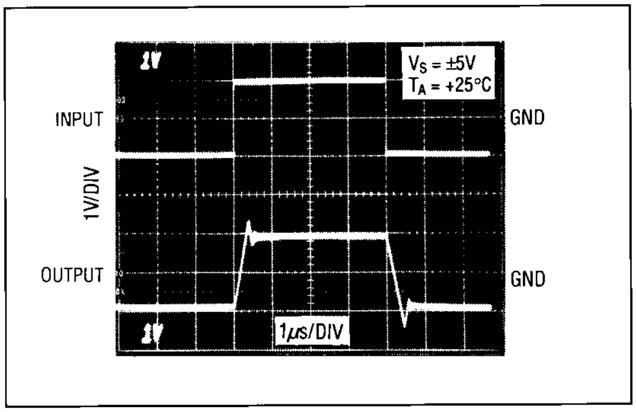


Figure 6b. Driving 100pF Load as shown in Figure 6a.

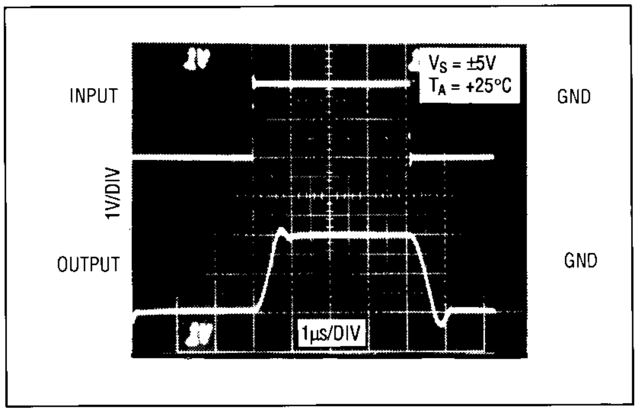


Figure 7b. Driving 6800pF Load with 22Ω Isolation Resistor

Rp and Rn include the resistances of the input driving source(s), if any.

If the Quan Tech model 5173 is used, then the A_{VCL} terms in the numerator and denominator of the equation given above should be eliminated because the Quan Tech measures input-referred noise. For the circuit in Figure 5, assuming Rp is approximately equal to Rn and the measurement is taken with the Quan Tech model 5173, the equation simplifies to:

$$i_n = \frac{\sqrt{e_{no}{}^2 - [(1.64 \times 10^{-20})(20 \times 10^3)]}}{(20 \times 10^3)} \ \mathrm{A}/\sqrt{\mathrm{Hz}}$$

Input Protection

To protect amplifier inputs from excessive differential input voltages, most modern op amps contain input protection diodes and current-limiting resistors. These resistors increase the amplifier's input referred noise. They have not been included in the MAX410/MAX412/MAX414, to optimize noise performance. The MAX410/MAX412/MAX414 do contain back-to-back input protection diodes which will protect the amplifier for differential input voltages of ±1.0V. If the amplifier must be protected from higher differential input voltages, add external current-limiting resistors in series with the op-amp inputs to limit the potential input current to less than 20mA.

Capacitive Load Driving

Driving large capacitive loads increases the likelihood of oscillation in amplifier circuits. This is especially true for circuits with high loop gains, like voltage followers. The output impedance of the amplifier and a capacitive load form an RC network that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded.

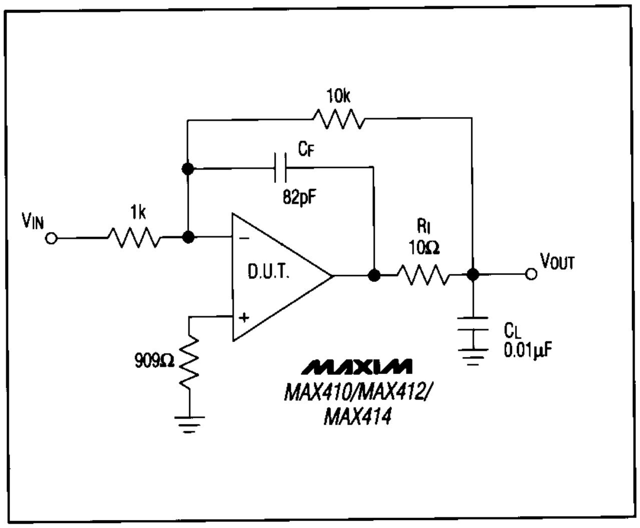


Figure 8. Capacitive-Load Driving Circuit with Loop-Enclosed Isolation Resistor

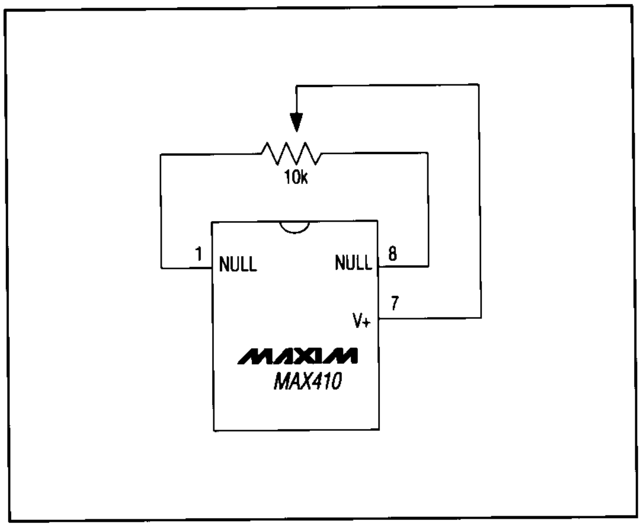


Figure 9. MAX410 Offset Null Circuit

In voltage follower circuits, the MAX410/MAX412/MAX414 remain stable while driving capacitive loads as great as 100pF. See Figures 6a and 6b.

When driving capacitive loads greater than 100pF, add an output isolation resistor to the voltage follower circuit, as shown in Figure 7a. This resistor isolates the load capacitance from the amplier output and restores the phase margin. Figure 7b is a photograph of the response of a MAX410/MAX412/MAX414 driving a 6800pF load with a 22Ω isolation resistor.

The capacitive load driving performance of the MAX410/MAX412/MAX414 is plotted for closed-loop gains of -1V/V and -10V/V in the % Overshoot vs. Capacitive Load graph in the *Typical Operating Characteristics*.

Feedback around the isolation resistor (R_I) increases the accuracy at the capacitively loaded output (see Figure 8). The MAX410/MAX412/MAX414 are stable with a 0.01µF load for the values of R_I and C_F shown. In general, for decreased closed loop gain, increase R_I or C_F. To drive larger capacitive loads, increase the value of C_F.

Total Supply Voltage Considerations

Although the MAX410/MAX412/MAX414 are specified with ±5V power supplies, they are also capable of single-supply operation with voltages as low as 4.8V. The minimum input voltage range for normal amplifier operation is between V- + 1.5V and V+ - 1.5V. The minimum room-temperature output voltage range (with a 2kΩ load) is between V+ - 1.4V and V- + 1.3V for total supply voltages between 4.8V and 10V. The output voltage range, referenced to the supply voltages, decreases slightly over temperature, as indicated in the ±5V *Electrical Charateristics* tables. Operating characteristics at total supply voltages of less than 10V are guaranteed by design and PSRR tests.

MAX 410 Offset Voltage Null

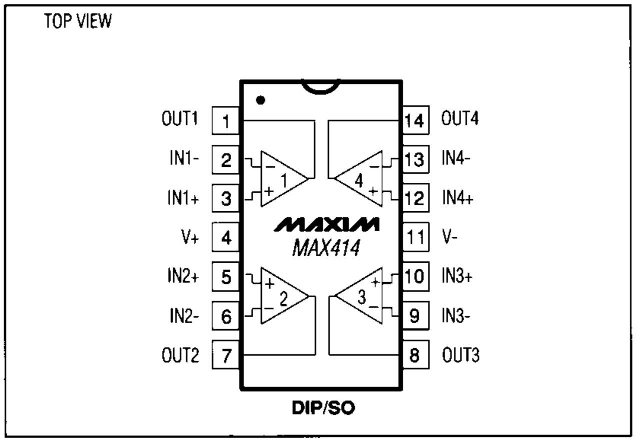
The offset null circuit of Figure 9 provides approximately ±450µV of offset adjustment range, sufficient for zeroing offset over the full operating temperature range.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX412CPA	0°C to +70°C	8 Plastic DIP
MAX412BCPA	0°C to +70°C	8 Plastic DIP
MAX412CSA	0°C to +70°C	8 SO
MAX412BCSA	0°C to +70°C	8 SO
MAX412C/D	0°C to +70°C	Dice*
MAX412EPA	-40°C to +85°C	8 Plastic DIP
MAX412BEPA	-40°C to +85°C	8 Plastic DIP
MAX412ESA	-40°C to +85°C	8 SO
MAX412BESA	-40°C to +85°C	8 SO
MAX412MJA	-55°C to +125°C	8 CERDIP
MAX412BMJA	-55°C to +125°C	8 CERDIP
MAX414CPD	0°C to +70°C	14 Plastic DIP
MAX414BCPD	0°C to +70°C	14 Plastic DIP
MAX414CSD	0°C to +70°C	14 SO
MAX414BCSD	0°C to +70°C	14 SO
MAX414EPD	-40°C to +85°C	14 Plastic DIP
MAX414BEPD	-40°C to +85°C	14 Plastic DIP
MAX414ESD	-40°C to +85°C	14 SO
MAX414BESD	-40°C to +85°C	14 SO
MAX414MJD	-55°C to +125°C	14 CERDIP
MAX414BMJD	-55°C to +125°C	14 CERDIP

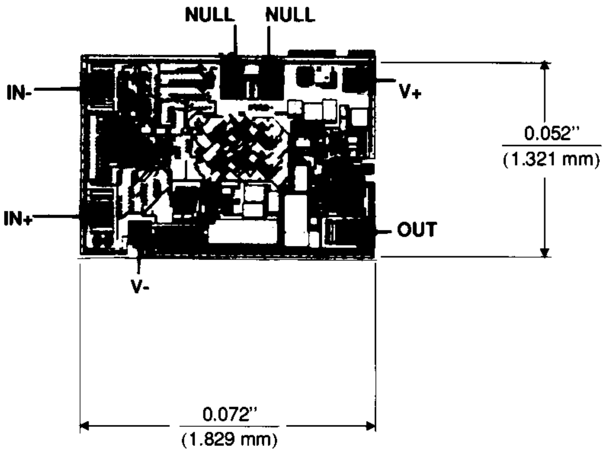
** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations (continued)



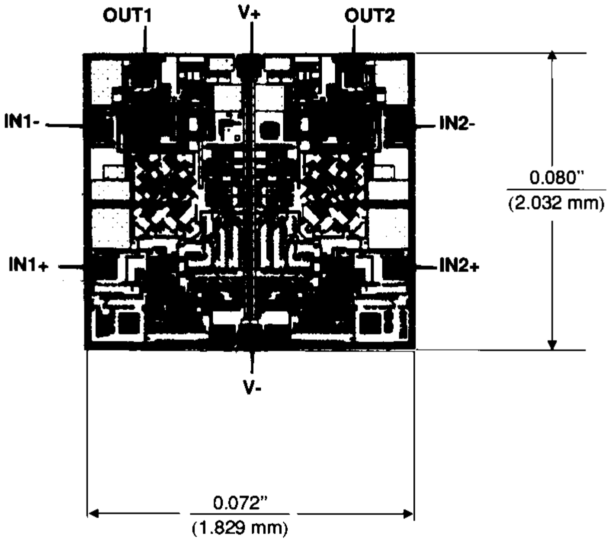
Chip Topographies

MAX410



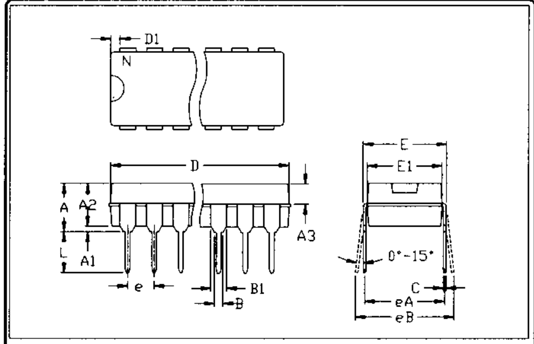
SUBSTRATE CONNECTED TO: V-
TRANSISTOR COUNT: 132

MAX412



SUBSTRATE CONNECTED TO: V-
TRANSISTOR COUNT: 262

Packaging Information

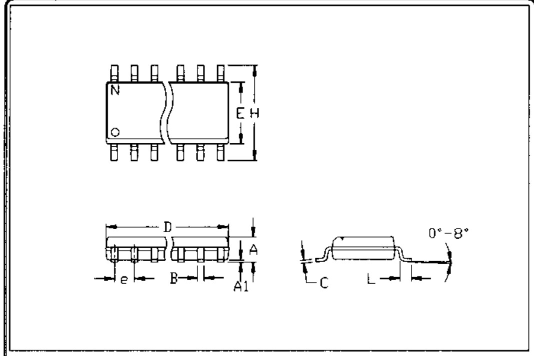


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

PACKAGE FAMILY OUTLINE: PDIP .300" 1/1 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

PACKAGE FAMILY OUTLINE: SOIC .150" 1/1 21-0041 A