19-4325; Rev 2; 10/94

MAXIM

Quad, High-Side MOSFET Drivers

General Description

The MAX620/MAX621 incorporate four MOSFET drivers and a charge-pump high-side power supply to power high-side switching and control circuits. The charge pump delivers a regulated output voltage 11V greater than V_{CC} to the drivers, which then translate a TTL/CMOS input signal to a noninverted output that swings from ground to the high-side voltage. The outputs drive N-channel FETs in high-side or low-side switching applications, including a wide range of line- and battery-powered applications.

The MAX620/MAX621 are microprocessor compatible and feature undervoltage lockout capability. This lockout feature inhibits the FET driver outputs until the high-side voltage reaches the proper level, as indicated by a Power-Ready output.

The MAX620 requires three inexpensive charge-pump capacitors. The MAX621 has internal capacitors—no external components are needed.

Applications

Portable Computer Battery Load Management

High-Side Power, N-Channel MOSFET Switching

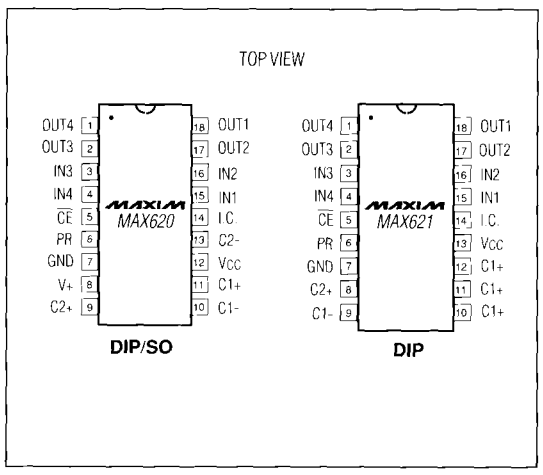
Low-Side Switching from Low Supply Voltages

Quad-Latching Level Translators

H-Bridge Motor Drivers

Stepper Motor Drivers

Pin Configurations



Features

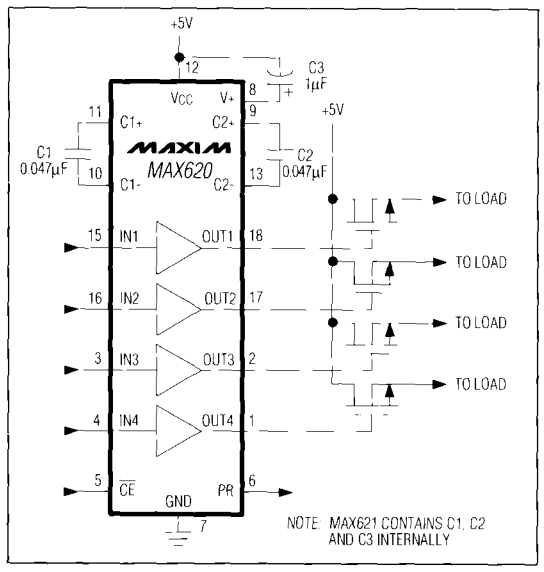
- ♦ **Wide Operating Voltage Range**
- ♦ **Minimum Component Count**
- ♦ **Output Voltage Regulated to V_{CC} Plus 11V (Typ)**
- ♦ **Low Quiescent Current – 70µA (Typ)**
- ♦ **Undervoltage Lockout**
- ♦ **Power-Ready Output**
- ♦ **Internal Quad Latch**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX620CPN	0°C to +70°C	18 Plastic DIP
MAX620CWN	0°C to +70°C	18 Wide SO
MAX620C/D	0°C to +70°C	Dice*
MAX620EPN	-40°C to +85°C	18 Plastic DIP
MAX620EWN	-40°C to +85°C	18 Wide SO
MAX621CPN	0°C to +70°C	18 Plastic DIP
MAX621EPN	-40°C to +85°C	18 Plastic DIP

*Contact factory for dice specifications.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} 17V
V+ to GND 30V
Inputs and Driver Outputs ..... (GND-0.3V) to (V+ + 0.3V)
PR Output ..... (GND-0.3V) to (V_{CC} + 0.3V)
Continuous Driver Output Current 25mA
V+ Output Current (MAX620 Only) 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8mW/°C above +70°C) 640mW
Wide SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX62 _ C _ _ ..... 0°C to +70°C
MAX62 _ E _ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5		16.5	V
High-Side Voltage (Note 1)	V+	I_{OUT} = 0, V_{CC} = 4.5V, C1 = C2 = 0.047µF, C3 = 1µF	14.5	15.5	17.5	V
		I_{OUT} = 0, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5	27.5	29.5	
		I_{OUT} = 250µA, V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF	15	16	18	
		I_{OUT} = 500µA, V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF (Note 2)	26.5	27.5	29.5	
Power-Ready Threshold	PRT	I_{OUT} = 100µA Sink (Notes 3, 4)	12.0	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA (Note 4)	3.8	4.7	5.0	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA (Note 4)		0.1	0.4	V
Switching Frequency	f_O	I_{OUT} = 0, T_A = +25°C		70		kHz
Quiescent Supply Current	I_Q	MAX620: V_{CC} = 5V, C1 = C2 = 0.047µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0		70	500	µA
		MAX621: V_{CC} = 5V, T_A = +25°C, I_{OUT} = 0				
		MAX620: V_{CC} = 16.5V, C1 = C2 = 0.01µF, C3 = 1µF, T_A = +25°C, I_{OUT} = 0 (Note 5)		50	350	
		MAX621: V_{CC} = 16.5V, T_A = +25°C, I_{OUT} = 0				

ELECTRICAL CHARACTERISTICS (continued)

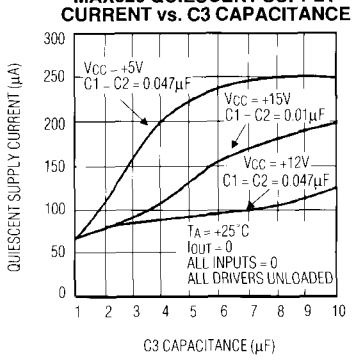
(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE DRIVERS						
Input Threshold Low	V_{TL}				0.8	V
Input Threshold High	V_{TH}		2.4			V
Input Bias Current	I_B	0V < V_{IN} < 5V	-100		100	nA
Chip Enable Threshold Low	CE_{LO}				0.8	V
Chip Enable Threshold HIgh	CE_{HI}		2.4			V
Minimum $\overline{CE}$ Pulse Duration	T_{CE}		100	50		ns
Pull-Down Current	I_{CE}			10		µA
Data-Hold Time	T_{DH}			-10	10	ns
Data Set-Up Time	T_{SU}			50	100	ns
Data-Delay Time	T_{OD}	V_{CE} = 0V, C_L = 12pF		150		ns
Driver Output Rise Time	T_R	C_L = 1000pF		1.7		µs
Driver Output Fall Time	T_F	C_L = 1000pF		2.5		µs

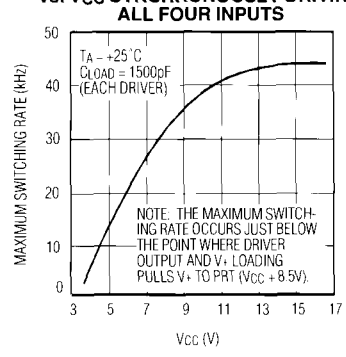
Note 1: High-Side Voltage (V+) is available only on the MAX620 and is measured with respect to GND. V+ on the MAX621 is measured at an unloaded output. Capacitor values listed in the test conditions apply to the MAX620 only.
Note 2: For V_{CC} > +13V, on the MAX620 only, use C1 = C2 = 0.01µF, C3 = 1µF.
Note 3: Power-Ready Threshold is the voltage with respect to GND at V+ when PR switches high (PR_{OH} = V_{CC}).
Note 4: For the MAX621, the Power-Ready levels are tested at wafer sort only.
Note 5: The MAX620 is tested for quiescent current at +16.5V using C1 = C2 = 0.047µF to minimize test time. In normal operation above +13V, C1 and C2 must not exceed 0.01µF.

Typical Operating Characteristics

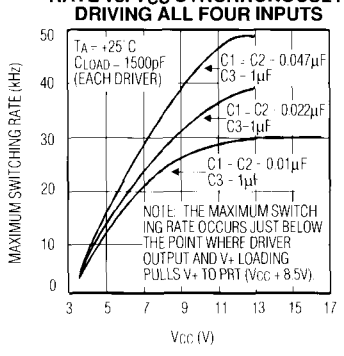
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITANCE



MAX621 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS

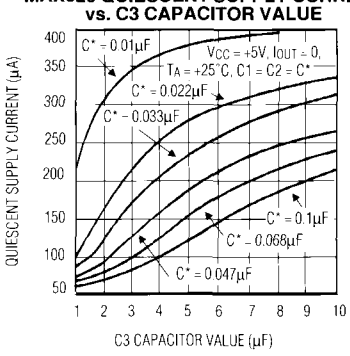


MAX620 MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS

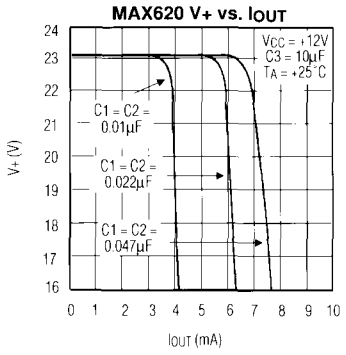


Typical Operating Characteristics (continued)

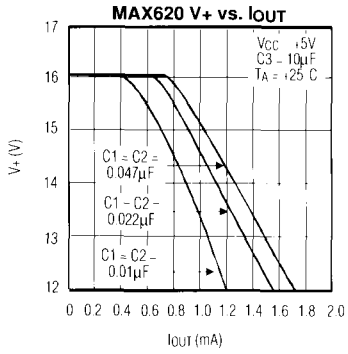
MAX620 QUIESCENT SUPPLY CURRENT vs. C3 CAPACITOR VALUE



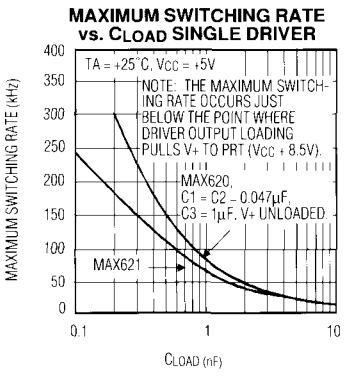
MAX620 V+ vs. IOUT



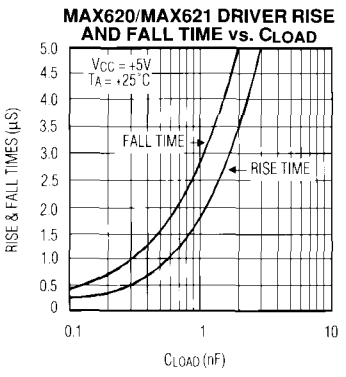
MAX620 V+ vs. IOUT



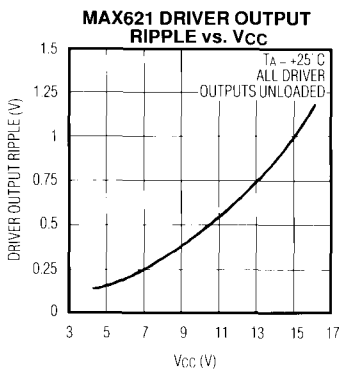
MAXIMUM SWITCHING RATE vs. CLOAD SINGLE DRIVER



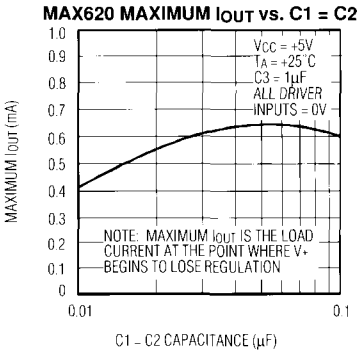
MAX620/MAX621 DRIVER RISE AND FALL TIME vs. CLOAD



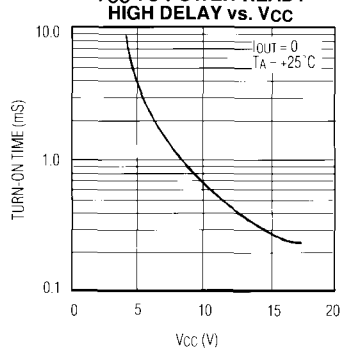
MAX621 DRIVER OUTPUT RIPPLE vs. VCC



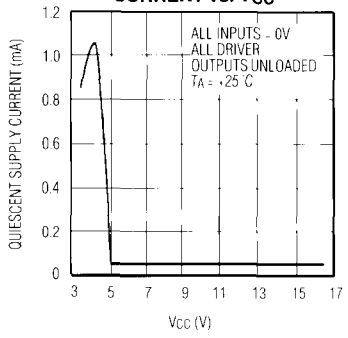
MAX620 MAXIMUM IOUT vs. C1 = C2



VCC TO POWER-READY HIGH DELAY vs. VCC

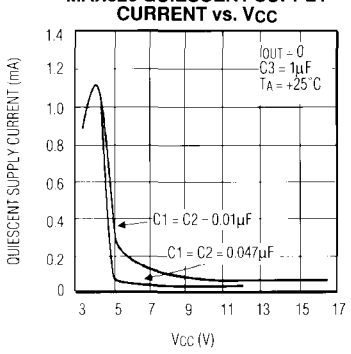


MAX621 QUIESCENT SUPPLY CURRENT vs. VCC

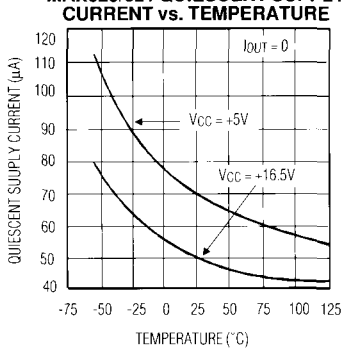


Typical Operating Characteristics (continued)

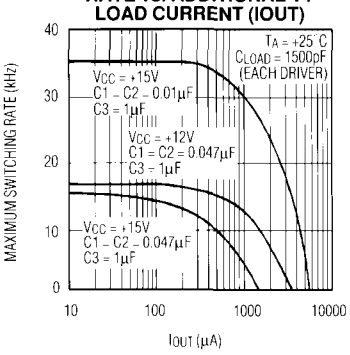
MAX620 QUIESCENT SUPPLY CURRENT vs. VCC



MAX620/621 QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

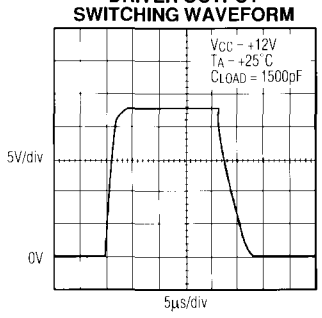


MAX620 MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (IOUT)

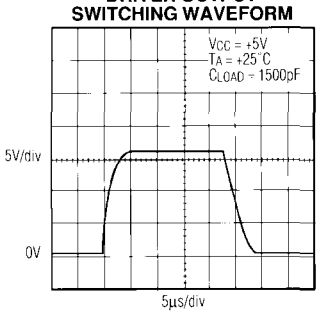


NOTE: THE MAXIMUM SWITCHING RATE OCCURS JUST BELOW THE POINT WHERE DRIVER OUTPUT AND V+ LOADING PULLS V+ TO PRT (VCC + 8.5V).

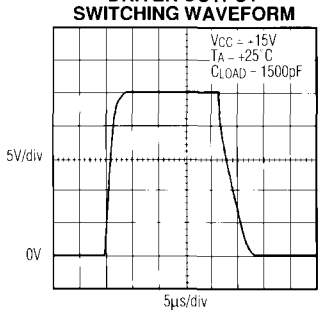
DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



DRIVER OUTPUT SWITCHING WAVEFORM



Pin Description

PIN		NAME	FUNCTION
MAX620	MAX621		
1	1	OUT4	Driver Output 4
2	2	OUT3	Driver Output 3
3	3	IN3	TTL/CMOS Compatible Input to Driver 3. Connect to GND if unused.
4	4	IN4	TTL/CMOS Compatible Input to Driver 4. Connect to GND if unused.
5	5	CE	Chip Enable. Logic high inhibits input data. Logic low transfers input data to the quad latch and driver outputs. $\overline{CE}$ pulse must be at least 100ns. Connect to GND for direct data transfer to driver outputs.
6	6	PR	Power-Ready Output is a logic high equal to V_{CC} when $V+ \geq (V_{CC}$ plus 8.5V).
7	7	GND	Ground
8		V+	High-side voltage out. Equal to approximately V_{CC} plus 11V.
	8	C2+	Internally connected to secondary charge-pump capacitor. Make no connection to this pin.
9		C2+	Positive terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	9	C1-	Internallly connected to primary charge-pump capacitor. Make no connection to this pin.
10		C1-	Negative terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
	10-12	C1+	Internally connected to primary charge-pump capacitor. Make no connection to these pins.
11		C1+	Positive terminal to primary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
12	13	V_{CC}	Supply Voltage. Connect to positive supply.
13		C2-	Negative terminal to secondary charge-pump capacitor. Connect to 0.047µF capacitor. For V_{CC} > 13V, connect to 0.01µF.
14	14	I.C.	Internal Connection. Make no connection to this pin.
15	15	IN1	TTL/CMOS Compatible Input to Driver 1. Connect to GND if unused.
16	16	IN2	TTL/CMOS Compatible Input to Driver 2. Connect to GND if unused.
17	17	OUT2	Driver Output 2
18	18	OUT1	Driver Output 1

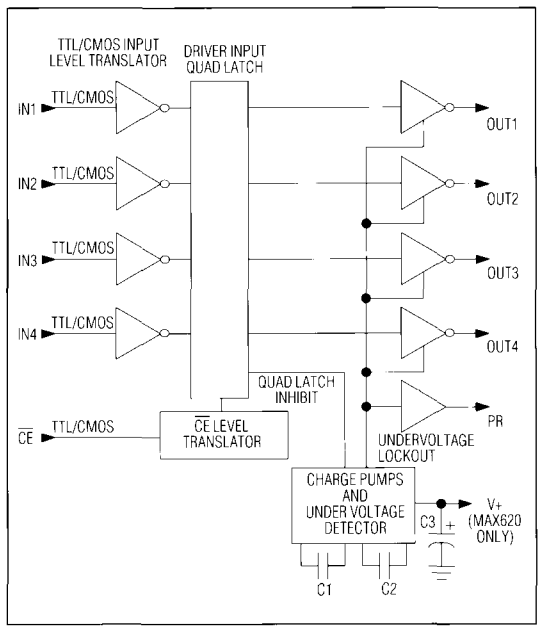


Figure 1. MAX620/MAX621 Functional Diagram

Detailed Description

Figure 1 shows the MAX620/MAX621 functional diagram. A regulated multi-stage charge pump supplies four MOSFET drivers with V_{CC} plus 11V for driving external MOSFETS (Figure 2). The logic inputs to the four drivers are stored in a quad latch. Data is latched by pulling $\overline{CE}$ high. An undervoltage lockout feature prevents the driver outputs from going high until V+ reaches the power-ready threshold (PRT) voltage (V_{CC} plus 8.5V) and V_{CC} is greater than +3V.

The Dual Charge Pump

The high-side voltage of approximately 11V above V_{CC} is generated by a multi-stage charge pump (Figure 2). Although the charge pump is capable of multiplying V_{CC} by up to four times, the output is regulated to V_{CC} plus 11V by an internal feedback circuit. The charge pump typically operates at 70kHz, but regulates by pulse-skipping. When V+ exceeds V_{CC} plus 11V, the charge pump shuts off. As V+ falls below V_{CC} plus 11V, the charge pump turns on.

The MOSFET Drivers

The four MOSFET drivers level shift TTL/CMOS input signals to output levels that switch between ground and V_{CC} plus 11V. These outputs can drive N-channel power MOSFETs in either high-side or low-side switching ap-

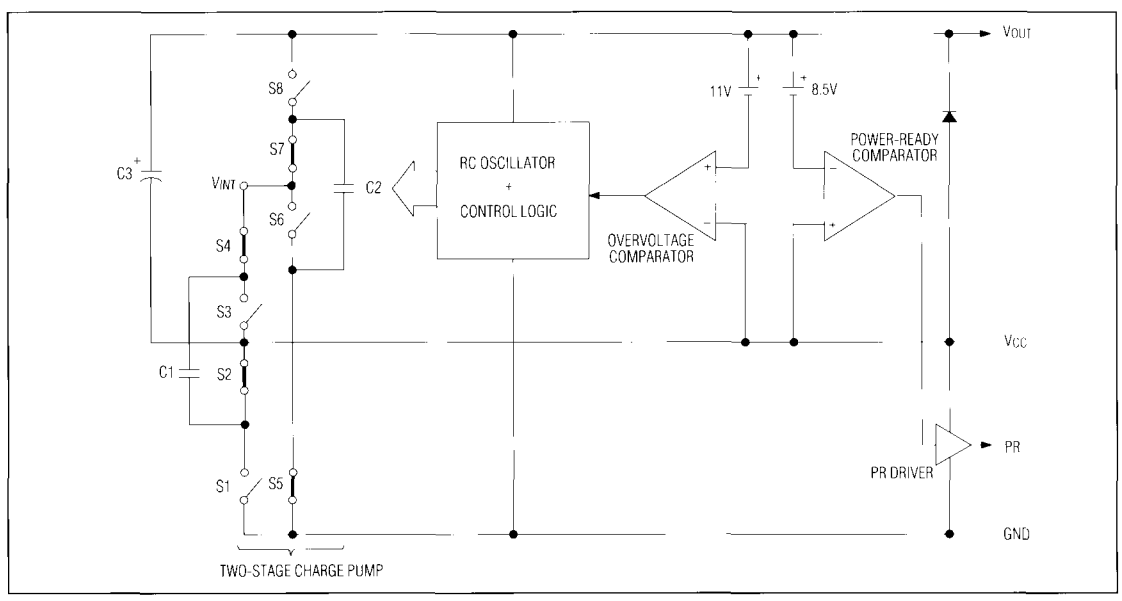


Figure 2. MAX620/MAX621 Charge Pump Block Diagram

plications (a bridge arrangement would contain two high-side and two low-side N-channel MOSFET switches—see Figure 4).

Data Input Latch

The driver outputs are separated from the data inputs by a quad latch. When $\overline{CE}$ is pulled low, the latch becomes transparent and data transfers directly to the outputs. When $\overline{CE}$ goes high, the latch enters hold mode and new input data is not transferred to the driver outputs.

Input data must be valid typically 100ns before the rising edge of $\overline{CE}$, and held for 10ns (max over temp). The minimum CE pulse width is 100ns (Figure 3). If latched operation is not required, connect $\overline{CE}$ to GND.

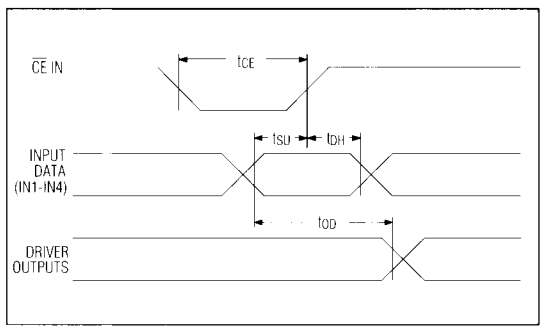


Figure 3. Digital Interface Timing Diagram

Undervoltage Latch Inhibit

If V_{CC} falls below +3V due to a power failure or while powering down, or V+ falls below V_{CC} plus 8.5V, the quad latch immediately resets, forcing the driver outputs low. The quad latch remains reset until V_{CC} rises above +3V with the high-side voltage present. This prevents the latch from being corrupted with erroneous data in a momentary power failure by ensuring that it will be reset.

Undervoltage Detector

The MAX620/MAX621 each contain an undervoltage detector, which forces all driver outputs low when the high-side voltage (V+) is less than the PRT or when V_{CC} is less than +3V. This ensures that the external N-channel MOSFET power transistors have sufficient gate drive to operate without dissipating excessive power. On power-up, the quad latch remains reset until the charge pump boosts the high-side voltage to the PRT. As soon as V+ reaches the PRT, the undervoltage lockout disables, the quad latch is enabled, and Power Ready (PR) goes high. The undervoltage lockout feature also forces the driver outputs low if V+ is pulled below PRT, e.g., if the driver output(s) or V+ are overloaded.

Power-Ready Output

The MAX620/MAX621's PR output is a direct extension of the undervoltage lockout feature. When power is applied, PR remains a logic low until V+ reaches the PRT and V_{CC} exceeds +3V. The PR output high level is V_{CC}.

Capacitor Selection for the MAX620

Capacitor type is not critical for the MAX620. However, if operation with V_{CC} exceeding +13V is expected, C1 and C2 must be no greater than 0.01µF. Larger value capacitors, with V_{CC} above +13V, dissipate excessive energy in the internal switches during charge-pump cycles.

Sourcing Current From V+ (MAX620 Only)

A small amount of current may be sourced from V+ (pin 8) to drive other circuitry. The amount of current is a function of V_{CC}, the gate capacitance of all MOSFETs being driven, and the driver switching rate ("MAX620 Maximum Switching Rate vs. Additional V+ Load Current," *Typical Operating Characteristics*).

The MAX620 V+ output is not internally short-circuit protected. In applications where V+ is susceptible to short circuiting, external output short-circuit protection must be provided. Accomplish this by connecting a resistor between V+ and the load to limit the V+ current to less than 25mA. The resistor value is determined by the following formula:

$$R_{CL} \geq \frac{V_{CC}}{25mA}$$

Application Information

Data Input Transition Time

The MAX620/MAX621 are microprocessor compatible and easy to interface. However, the driver input voltage must not remain between V_{IL} and V_{IH} for more than 500ns. In clocked data-bus systems, this is most easily accomplished by setting data on the driver input lines before clocking $\overline{CE}$ low. However, most CMOS and TTL gates meet the 500ns transition speed requirement. Connect unused driver inputs to GND.

Maximum Driver Switching Rate

The maximum driver switching rate occurs when loading causes V+ to fall to the PRT (V_{CC} plus 8.5V) and the driver outputs go low. It is a function of the total gate capacitance of all MOSFETs being driven and the maximum available charge-pump output current at a given

supply voltage. For example, for V_{CC} = +5V with no external load on V+, the maximum switching rate while driving four 1500pF loads is 15kHz for the MAX620 (C1 = C2 = 0.047µF) and 14kHz for the MAX621 ("Maximum Switching Rate vs. V_{CC}," *Typical Operating Characteristics*).

Typical Application Circuits

H-Bridge Motor Driver

Figure 4 shows a MAX620 driving an H-bridge switch that controls the direction of a +5V DC motor. By toggling between the FORWARD and REVERSE inputs as shown, each MOSFET driver-output pair turns on its associated MOSFET pair, which passes current through the motor, causing rotation in the desired direction. In order to prevent all four MOSFETs from switching on at once, the FORWARD/REVERSE inputs should be updated before clocking $\overline{CE}$ low. Of course, FORWARD and REVERSE must not be asserted simultaneously. Do not use a supply voltage that will cause the gate drive to exceed the absolute maximum gate-to-source voltage of the low-side switch.

Stepper Motor Driver

A MAX620, clock source, pulse control network, and translator logic form a complete stepper motor driver (Figure 5). TTL/CMOS signals from the logic network are translated to high-side levels that drive four N-channel power MOSFETs, supplying current to each of four stepper motor phases. Diodes provide a discharge current path for the stepper motor windings.

Logic-Controlled, +5V Regulated Power Distribution

A MAX620, LM10 reference and op-amp combination, and an IRFZ40 N-channel MOSFET comprise an ultra-low dropout +5V regulator that supplies power to four IRFZ40 high-side switches (Figure 6).

When the power switch, S_P, is closed, V+ quickly pumps up to V_{CC} plus 11V. PR remains low and holds the output of the +5V regulator near zero until V+ has reached the PRT, (V_{CC} plus 8.5V--4ms typ). At the same time, the undervoltage lockout feature of the MAX620 forces the driver outputs low until the PRT is reached. Capacitor C4 suppresses load-switching transients. Its size depends on the largest load being switched. With C4 = 1000µF, the peak transient for a 1A switched load is less than 150mV.

The circuit provides a single continuous +5V output and four switched +5V supply lines. The regulator is capable of supplying several amps with a typical dropout voltage of 28mV at 1A (Q1=IRFZ40).

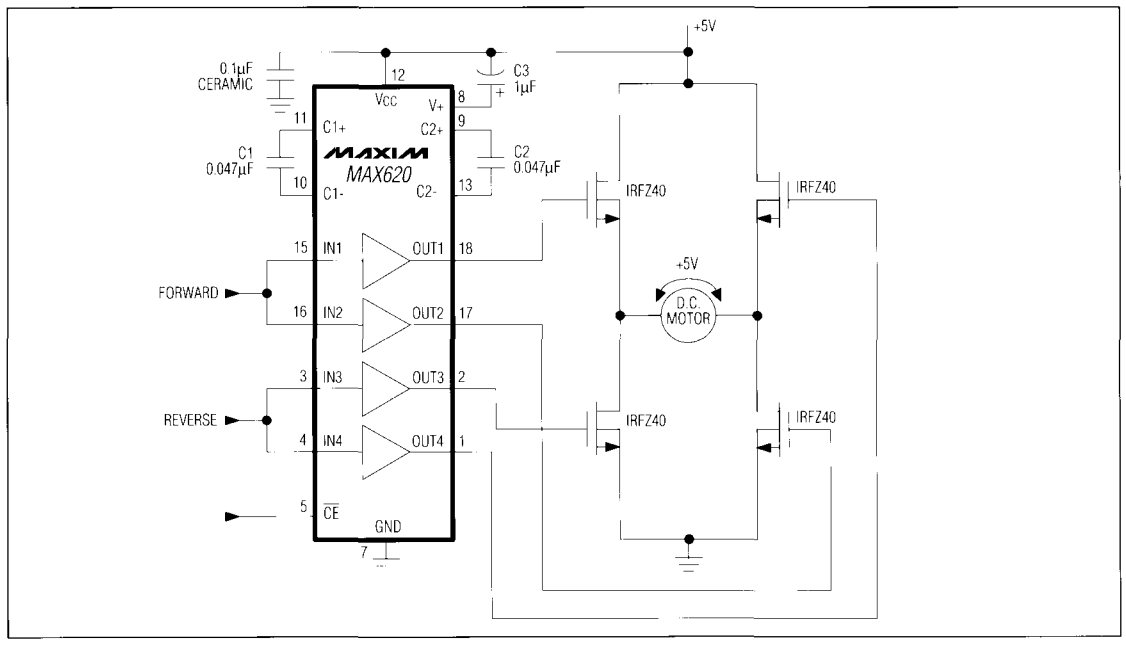


Figure 4. H-Bridge DC Motor Controller

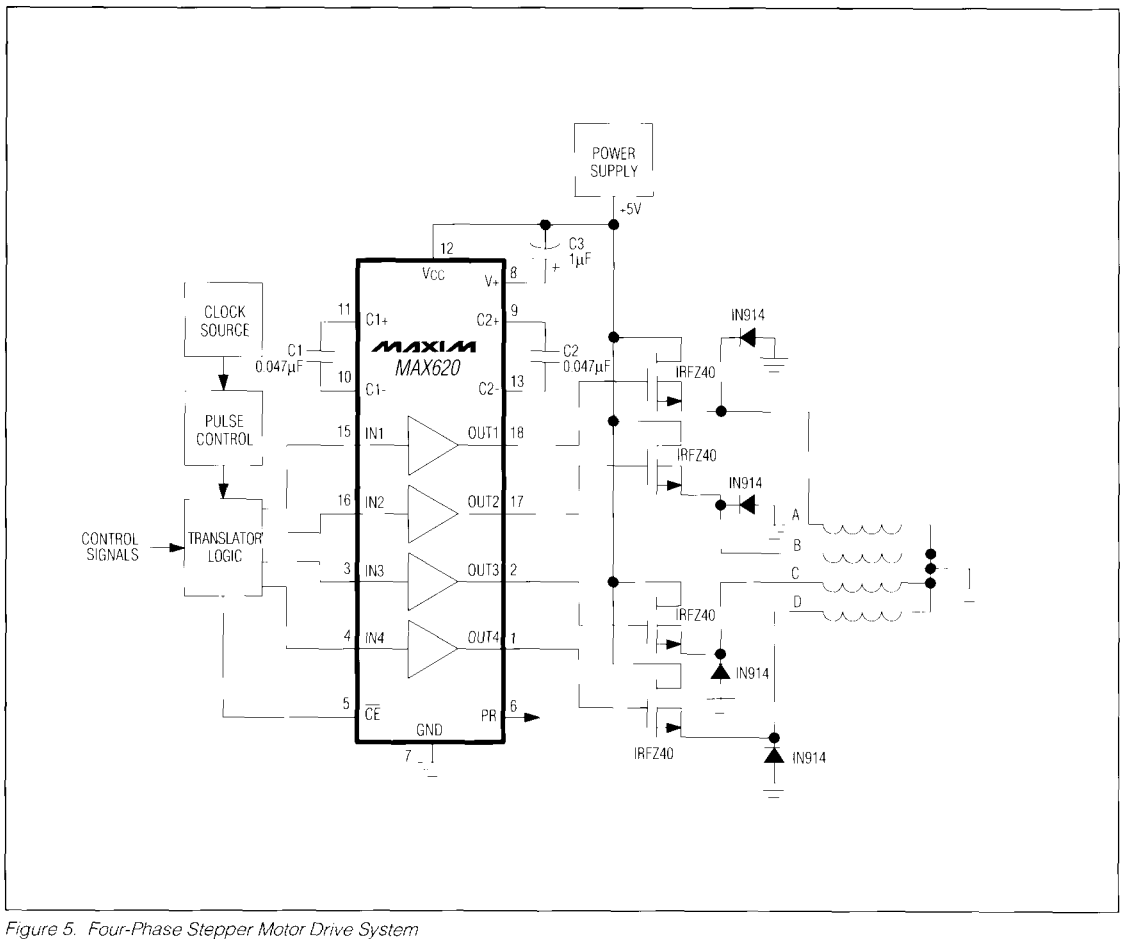


Figure 5. Four-Phase Stepper Motor Drive System

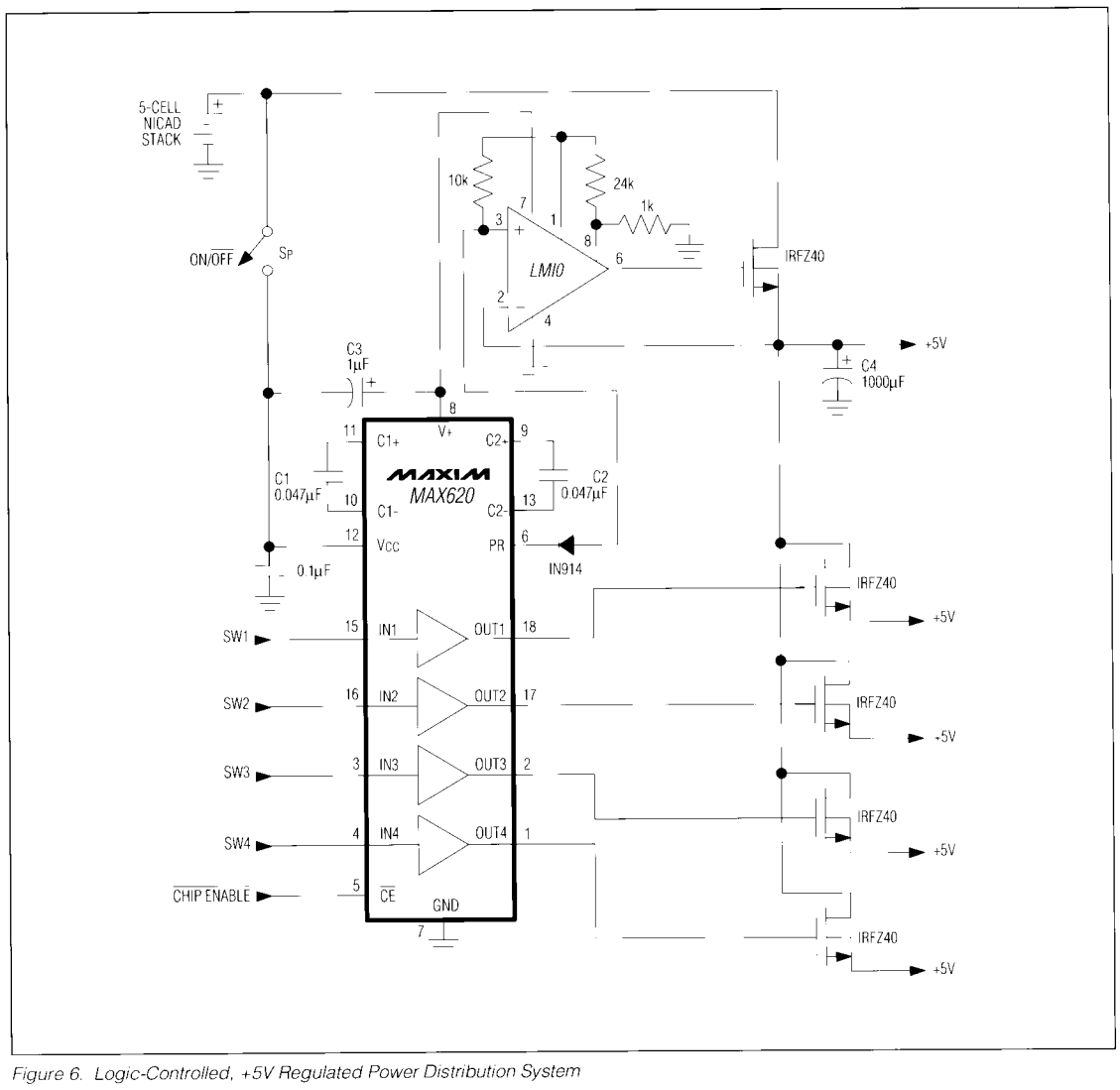
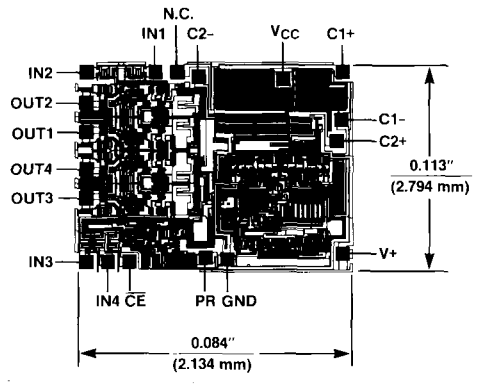


Figure 6. Logic-Controlled, +5V Regulated Power Distribution System

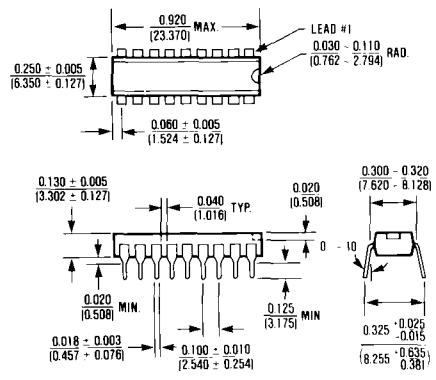
Quad, High-Side MOSFET Drivers

Chip Topography

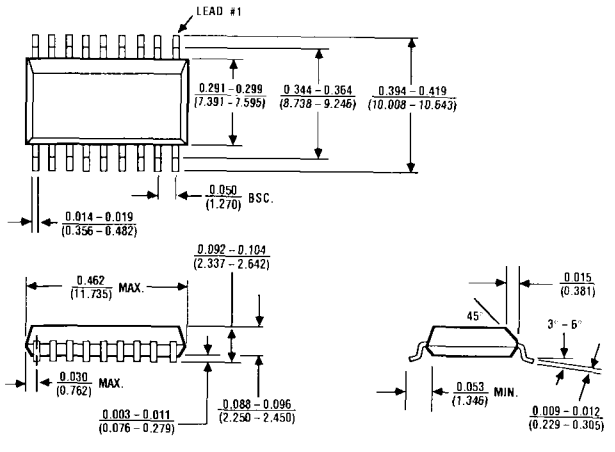


NOTE: Connect substrate to V+.
MAX620 transistor count: 303

Package Information



18 Lead Plastic DIP
θ_{JA} = 130°C/W
θ_{JC} = 60°C/W



18 Lead Small Outline, Wide
θ_{JA} = 105°C/W
θ_{JC} = 60° C/W