19-0011; Rev. 0; 6/92

NAXIN 8V CMOS Switched-Capacitor Voltage Converter

General Description

The MAX665 charge-pump voltage inverter converts a $\pm 1.5V$ to $\pm 8V$ input to a corresponding $\pm 1.5V$ to $\pm 8V$ output. Using only two low-cost capacitors to produce 100mA, the MAX665 replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX665 can also double the output voltage of an input power supply or battery, providing $\pm 9.35V$ at 100mA from a $\pm 5V$ input.

A Frequency Control (FC) pin selects either 10kHz or 45kHz operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX665 is a pin-compatible high-current upgrade of the ICL7660. For an 8-pin SO version with a 5.5V maximum input voltage, refer to the MAX660 data sheet.

The MAX665 is available in both 8-pin DIP and 16-pin wide SO packages in commercial, extended, and military temperature ranges.

Applications

- Laptop Computers Medical Instruments
- Interface Power Supplies
- Handheld Instruments
- **Op-Amp Power Supplies**
- GaAs Power-Amp Bias Supplies

_ Pin Configurations



Features

MAX665

- 0.65V Loss at 100mA Load
- 6.5Ω Output Impedance
- Pin-Compatible High-Current ICL7660 Upgrade
- ♦ Inverts or Doubles Input Supply Voltage
- Selectable Oscillator Frequency: 10kHz/45kHz
- ♦ 88% Conversion Efficiency at 100mA (IL to GND)
- ♦ 200µA Operating Current
- ♦ +1.5V to +8V Supply

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX665CPA	0°C to +70°C	8 Plastic DIP
MAX665CWE	0°C to +70°C	16 Wide SO
MAX665C/D	0°C to +70°C	Dice*
MAX665EPA	-40°C to +85°C	8 Plastic DIP
MAX665EWE	-40°C to +85°C	16 Wide SO
MAX665MJA	-55°C to +125°C	8 CERDIP

* Dice are tested at +25°C only.

Typical Operating Circuits



POSITIVE VOLTAGE DOUBLER 📃

PIN NUMBERS REFER TO DIP PACKAGE.

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<u>Maxim Integrated Products</u> 1

Call toll free 1-800-998-8800 for free samples or literature.

ABSOLUTE MAXIMUM RATINGS

Continuous Power Dissipation (TA = $+70^{\circ}$ C) 8-Pin Plastic DIP (derate 9.09mW/°C above $+70^{\circ}$ C) 727mW 16-Pin Wide SO (derate 9.52mW/°C above $+70^{\circ}$ C) 762mW 8-Pin CERDIP (derate 8.00mW/°C above +70°C) . . . 640mW

Operating Temperature Ranges:

MAX665C	· · · · · · · · · · · · · · · · · ·	0°C to +70°C
MAX665E		-40°C to +85°C
MAX665MJA		-55°C to +125°C
Storage Temperature Range		-65°C to +160°C
Lead Temperature (soldering	, 10 sec)	+300°C

Note 1: OUT may be shorted to GND for 1 sec without damage, but shorting OUT to V+ may damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, C1, C2 = 150µF, test circuit of Figure 1, FC = open, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS	
		Inverter, LV = open	3		8	v	
Operating Supply Voltage	$R_L = 1k\Omega$	Inverter, LV = GND	1.5		8		
		Doubler, LV = OUT	2.5		8		
Supply Current	No load	FC = open		0.2	0.5	- mA	
		FC = V+		1	3		
Output Current	T _A ≤ +85°C, OUT r	nore negative than -4V	100				
	TA > +85°C, OUT r	more negative than -3.8V	100		mA		
	100-1	T _A ≤ +85°C		6.5	10	- Ω	
Output Resistance (Note 3)	1L = 100mA	T _A > +85°C			12		
Oscillator Frequency	FC = open FC = V+			10		kHz	
				45			
OSC Input Current	FC = open		±1.1			- μΑ	
	FC = V+			±5			
Power Efficiency	$R_L = 1k\Omega$ connected between V+ and OUT		96	98		%	
	$R_L = 500\Omega$ connected between OUT and GND		92	96			
	IL = 100mA to GND			88			
Voltage Conversion Efficiency	No load		99	99.96		%	

Note 2: In the test circuit, capacitors C1 and C2 are 150μF, 0.2Ω maximum ESR, aluminum electrolytics (Maxim part # MAXC001). Capacitors with higher ESR may reduce output voltage and efficiency.
Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See Capacitor Selection section.

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All curves are generated using the test circuit of Figure 1 with V+ = 5V, LV = GND, FC = open, and TA = +25 $^{\circ}$ C, unless otherwise noted. The charge-pump frequency is one-half the oscillator frequency. Test results are also valid for doubler mode with GND = +5V, LV = OUT, and OUT = 0V, unless otherwise noted; however, the input voltage is restricted to +2.5V to +8V.

Typical Operating Characteristics

MAX665



Figure 1. MAX665 Test Circuit











900

800

700

EFFICIENCY (%)

200

100



0.8





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LOAD CURRENT (mA)

60

80

100

40

20



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EFFICIENCY vs. OSCILLATOR FREQUENCY



Pin Description

MAX665

PIN		NAME	FUNCTION		
DIP	WIDE SO	NAME	INVERTER	DOUBLER	
1	2	FC	Frequency Control for internal oscillator. FC = open, $f_{OSC} = 10$ kHz typ; FC = V+, $f_{OSC} = 45$ kHz typ; FC has no effect when OSC pin is driven externally.	Same as inverter	
2	4	CAP+	Positive Charge-Pump Capacitor Terminal	Same as inverter	
3	6	GND	Power-Supply Ground Input	Power-Supply Positive Volt- age Input	
4	8	CAP-	Negative Charge-Pump Capacitor Terminal	Same as inverter	
5	9	OUT	Output, Negative Voltage	Power-Supply Ground Input	
6	11	LV	Low-Voltage Operation Input. Tie LV to GND when input voltage is less than 3V. Above 3V, LV may be connected to GND or left open; when overdriving OSC, LV must be connected to GND.	LV must be tied to OUT for all input voltages.	
7	13	OSC	Oscillator Control Input. OSC is connected to an internal 15pF capacitor. An external capacitor can be added to slow the oscillator. Care must be taken to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC.	Same as inverter; however, do not overdrive OSC in voltage doubler mode.	
8	16	V+	Power-Supply Positive Voltage Input	Positive Voltage Output	
	1, 3, 5, 7, 10, 12, 14, 15	N.C.	No Connect - not internally connected	No Connect	

Detailed Description

The MAX665 capacitive charge-pump circuit either inverts or doubles the input voltage. Two external capacitors are needed in the voltage inverting mode, while two capacitors and one diode are needed for the voltage doubling mode (see Typical Operating Circuits). For highest performance, use low effective series resistance (ESR) capacitors. See Capacitor Selection section for more details.

When using the inverting mode with a supply voltage less than 3V, LV must be connected to GND. This bypasses the internal regulator circuitry and provides best performance in low-voltage applications. When using the inverter mode with a supply voltage above 3V, LV may be connected to GND or left open. The part is typically operated with LV grounded, but since LV may be left open, the substitution of the MAX665 for the ICL7660 is simplified. LV must be grounded when overdriving OSC (see Changing Oscillator Frequency section). Connect LV to OUT (for any supply voltage) when using the doubler mode.

uses only two external capacitors, C1 and C2 (see Typical Operating Circuits). In most applications these are lowcost, low-ESR, 150µF electrolytic capacitors (refer to Capacitor Selection section).

Even though its output is not actively regulated, the MAX665 is very insensitive to load current changes. A typical output source resistance of 6.5Ω means that with an input of +5V the output voltage is -5V under light load, and decreases to only -4.35V with a 100mA load. Output source resistance vs. temperature and supply voltage are shown in the Typical Operating Characteristics graphs.

Output ripple voltage is calculated by noting that the output current supplied is solely from capacitor C2 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{\text{RIPPLE}} = \frac{I_{\text{OUT}}}{2(f_{\text{PUMP}})(\text{C2})} + I_{\text{OUT}} (\text{ESR}_{\text{C2}})$$

Applications Information For a nominal fPUMP of 5kHz (one-half the nominal 10kHz oscillator frequency) where $C2 = 150\mu$ F with an **Negative Voltage Converter** ESR of 0.2Ω , ripple is approximately 90mV with a The most common application of the MAX665 is as a 100mA load current. If C2 is raised to 390μ F, the ripple charge-pump voltage inverter. The operating circuit drops to 45mV.

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Positive Voltage Doubler

The MAX665 operates in the voltage-doubling mode as shown in the *Typical Operating Circuit*. The external Schottky (1N5817) diode is for start-up only. The no-load output is 2 x VIN and is not reduced by the diode forward drop.

Changing Oscillator Frequency

Four modes control the MAX665's clock frequency, as listed below:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC = V+	Open	45kHz
Open or FC = V+	External capacitor	See Typical Operating Characteristics
Open	External clock	External clock frequency

When FC and OSC are unconnected (open), the oscillator runs at 10kHz typically. When FC is connected to V+, the charge and discharge current at OSC changes from 1.1μ A to 5 μ A, thus increasing the oscillator frequency 4.5 times. In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by 4.5 times in this mode.

In the inverter mode, OSC may also be overdriven by an external clock source that swings within 100mV of V+ and GND. Any standard CMOS logic output is suitable for driving OSC. When OSC is overdriven, FC has no effect. Also, LV must be grounded when overdriving OSC. Do not overdrive the OSC pin in the voltage doubler mode.

Note: In all modes, the frequency of the signal appearing at CAP+ and CAP- is one-half that of the oscillator. Also, an undesirable effect of lowering the oscillator frequency is the charge pump's effective output resistance. Compensate for this by increasing the value of the charge-pump capacitors (see *Capacitor Selection* section and *Typical Operating Characteristics*).

In some applications, the 5kHz output ripple frequency may be low enough to interfere with other circuitry. If desired, the oscillator frequency can then be increased by using the FC pin or an external oscillator as described above. The output ripple frequency is one-half the selected oscillator frequency. Increasing the clock frequency increases the MAX665's quiescent current, but also allows smaller capacitance values to be used for C1 and C2.

Capacitor Selection

Three factors (in addition to load current) affect the MAX665 output voltage drop from its ideal value:

MAX665 output resistance,

2) Pump (C1) and reservoir (C2) capacitor ESRs,

3) C1 and C2 capacitance.

The voltage drop caused by MAX665 output resistance is the load current times the output resistance. Similarly, the loss in C2 is the load current times C2's ESR. The loss in C1, however, is larger because it handles currents that are greater than the load current during chargepump operation. The voltage drop due to C1 is therefore about four times C1's ESR times the load current. Consequently, a low (or high) ESR capacitor has much greater impact on performance for C1 than for C2.

Generally, as the MAX665's pump frequency increases, the capacitance values required to maintain comparable ripple and output resistance diminish proportionately. Figure 2 shows the total circuit output resistance for various capacitor values (the pump and reservoir capacitors' values are equal) and oscillator frequencies. These curves assume 0.25 Ω capacitor ESRs and a 5.25 Ω MAX665 output resistance, which is why the flat portion of the curve shows a 6.5 Ω (Ro MAX665 + 4(ESRc1) + ESRc2) effective output resistance. Note: Ro = 5.25 Ω is used, rather than the typical 6.5 Ω , because the typical specification includes the effect of the capacitors' ESRs in the test circuit.

To reduce output ripple caused by the charge pump, increase reservoir capacitor C2 and/or reduce its ESR. Also, the reservoir capacitor must have low ESR if filtering high-frequency noise at the output is important.



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Figure 2. Total Output Source Resistance vs. C1 and C2 Capacitance (C1 = C2)

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Not all manufacturers guarantee the capacitor ESR range required by the MAX665. In general, capacitor ESR is inversely proportional to physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR. The capacitors used when testing the MAX665 are MAXC001 150 μ F aluminum electrolytics available from Maxim. They combine low cost, a guaranteed maximum ESR of 0.2 Ω at room temperature, and a low-temperature operating limit of -25°C. If operation at lower temperatures is required, certain tantalum capacitors provide good low-temperature ESR, but at added expense.

Manufacturers who provide low-ESR electrolytic capacitors include:

MANUFACTURER	CAPACITOR	CAPACITOR TYPE
Illinois Capacitor	RZS	Aluminum electrolytic
Mallory Capacitor	TDC & TDL	Tantalum
Nichicon	PF & PL	Aluminumelectrolytic
Sprague Electric	672D, 673D, 674D, 678D	Aluminum electrolytic
Sprague Electric	135D, 173D, 199D	Tantalum
United Chemi-Con	LXF & SXF	Aluminum electrolytic
Illinois Capacitor	(708) 675-1760	FAX (708) 673-2850
Mallory Capacitor	(317) 856-3731	FAX (317) 856-2500
Nichicon	(708) 843-7500	FAX (708) 843-2798
Sprague Electric	(508) 339-8900	FAX (508) 339-5063
United Chemi-Con	(708) 696-2000	FAX (708) 640-6341
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Cascading Devices

To produce larger negative multiplication of the initial supply voltage, the MAX665 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the



sum of the individual MAX665 ROUT values. The output voltage, where n is an integer representing the number of devices cascaded, is defined by VOUT = -n (VIN).

Paralleling Devices

Paralleling multiple MAX665s reduces the output resistance. As illustrated in Figure 4, each device requires its own pump capacitor C1, but the reservoir capacitor C2 serves all devices. C2's value should be increased by a factor of n, where n is the number of devices. Figure 4 shows the equation for calculating output resistance.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 5. In this circuit, capacitors C1 and C3 are pump and reservoir, respectively, for generating the negative voltage. Capacitors C2 and C4 are pump and reservoir for the multiplied positive voltage. This circuit configuration, however, leads to higher source impedances of the generated supplies. This is due to the common charge-pump driver's finite impedance.



Figure 4. Paralleling MAX665s to Reduce Output Resistance



Figure 3. Cascading MAX665s to Increase Output Voltage Figure 5. Combined Positive Multiplier and Negative Converter

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Figure 6. The MAX665 generates a +5V regulated output from a 3V lithium battery and operates for 16 hours with a 40mA load.



Chip Topography



SUBSTRATE CONNECTED TO V+; TRANSISTOR COUNT: 89.

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