19-2400; Rev 1; 7/93

MAXIM

Dual, Ultra-Fast ECL-Output Comparator

General Description

The MAX9687 is a dual, ultra-fast ECL comparator manufactured with a high-frequency bipolar process (f_T = 6GHz) capable of very short propagation delays. This design maintains the excellent DC matching characteristics normally found only in slower comparators.

The MAX9687 is pin-compatible with the AD9687 and Am6687, but exceeds their AC characteristics.

The MAX9687 has differential inputs and complementary outputs that are fully compatible with ECL-logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz.

A latch-enable (LE) function is provided to allow the comparator to be used in a sample/hold or track/hold mode. The latch-enable inputs are designed to be driven from the complementary outputs of a standard ECL gate. When LE is high and $\overline{LE}$ is low, the comparator functions normally. When LE is forced low and $\overline{LE}$ is high, the comparator outputs are locked in the logical states determined by the input conditions at the time of the latch transition. If the latch-enable function is not used on either of the two comparators, the appropriate LE input must be connected to ground; the companion $\overline{LE}$ input can be left open.

Applications

High-Speed A/D Converters
High-Speed Line Receivers
Peak Detectors
Threshold Detectors
High-Speed Triggers

Features

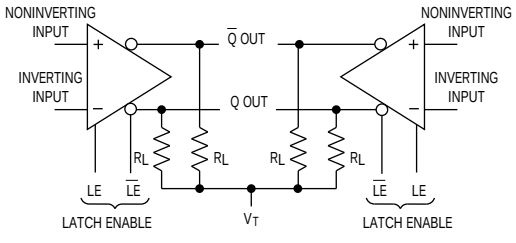
- **1.4ns Propagation Delay**
- **0.5ns Latch Setup Time**
- **2.0ns Latch-Enable Pulse Width**
- **+5V, -5.2V Power Supplies**
- **Pin-Compatible with AD9687, Am6687, SP9687**
- **Available in Commercial, Extended-Industrial, and Military Temperature Ranges**
- **Available in Narrow SO Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE*
MAX9687CPE	0°C to +70°C	16 Plastic DIP
MAX9687CSE	0°C to +70°C	16 Narrow SO
MAX9687CJE	0°C to +70°C	16 CERDIP
MAX9687C/D	0°C to +70°C	Dice**
MAX9687EPE	-40°C to +85°C	16 Plastic DIP
MAX9687ESE	-40°C to +85°C	16 Narrow SO
MAX9687MJE	-55°C to +125°C	16 CERDIP

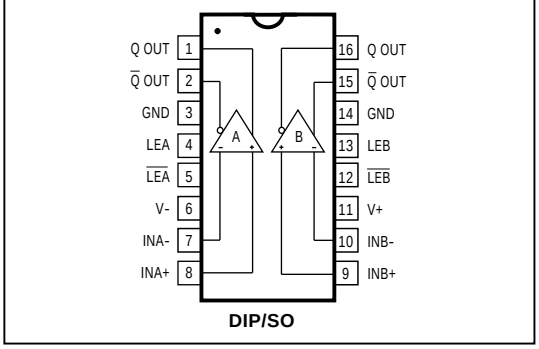
** Contact factory for availability of 20-pin PLCC.*
*** Contact factory for dice specifications.*

Functional Diagram



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO -2.0V, OR 240Ω – 2000Ω CONNECTED TO -5.2V.

Pin Configuration



DIP/SO

Dual, Ultra-Fast ECL-Output Comparator

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Output Short-Circuit Duration (Note 1) ..... Indefinite
Input Voltages ..... ±5V
Differential Input Voltages 3.5V
Output Current 30mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
  Narrow SO (derate 8.70mW/°C above +70°C) 696mW
  CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
  MAX9687C_ E ..... 0°C to +70°C
  MAX9687E_ E ..... -40°C to +85°C
  MAX9687MJE ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Continuous short-circuit protection is allowed on one comparator at a time up to case temperatures of +85°C and ambient temperatures of +30°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX9687C/E MIN	MAX9687C/E TYP	MAX9687C/E MAX	MAX9687M MIN	MAX9687M TYP	MAX9687M MAX	UNITS
Input Offset Voltage (Note 2)	V_{OS}	R_S = 100Ω	T_A = +25°C	-5		5	-5		5	mV
			$T_A = T_{MIN}$ to T_{MAX}	-7		7	-8		8	
Temperature Coefficient	$\Delta V_{OS}/\Delta T$				10			15		µV/°C
Input Offset Current	I_{OS}	T_A = +25°C				5			5	µA
		$T_A = T_{MIN}$ to T_{MAX}				8			12	
Input Bias Current	I_B	T_A = +25°C			10	20		10	20	µA
		$T_A = T_{MIN}$ to T_{MAX}				30			40	
Input Voltage Range	V_{CM}	(Note 2)		-2.5		+2.5	-2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	(Note 2)		80			80			dB
Power-Supply Rejection Ratio	PSRR				60			60		dB
Input Resistance	R_{IN}	(Note 2)		60			60			kΩ
Input Capacitance	C_{IN}				3			3		pF
Logic Output High Voltage	V_{OH}	MAX9687C, MAX9687M	$T_A = T_{MIN}$	-1.05		-0.87	-1.16		-0.89	V
			$T_A = T_{MAX}$	-0.89		-0.70	-0.88		-0.69	
			T_A = +25°C	-0.96		-0.81	-0.96		-0.81	
		MAX9687E	$T_A = T_{MIN}$	-1.14		-0.88				
			$T_A = T_{MAX}$	-0.88		-0.70				
			T_A = +25°C	-0.96		-0.81				
Logic Output Low Voltage	V_{OL}	MAX9687C, MAX9687M	$T_A = T_{MIN}$	-1.89		-1.65	-1.90		-1.65	V
			$T_A = T_{MAX}$	-1.83		-1.57	-1.82		-1.55	
			T_A = +25°C	-1.85		-1.65	-1.85		-1.65	
		MAX9687E	$T_A = T_{MIN}$	-1.90		-1.65				
			$T_A = T_{MAX}$	-1.83		-1.57				
			T_A = +25°C	-1.85		-1.65				
Positive Supply Current	I_{CC}	T_A = +25°C			30	46		30	46	mA
		$T_A = T_{MIN}$ to T_{MAX}				50			52	
Negative Supply Current	I_{EE}	T_A = +25°C			54	68		54	68	mA
		$T_A = T_{MIN}$ to T_{MAX}				72			74	

SWITCHING CHARACTERISTICS

(V_S = ±5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9687C/E			MAX9687M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output High (Notes 2, 3)	t_{pd+}	T_A = +25°C		1.4	1.9		1.4	1.9	ns
		T_A = 0°C to +70°C		1.6	2.2				
		T_A = -55°C to +125°C					1.7	2.6	
Input to Output Low (Notes 2, 3)	t_{pd-}	T_A = +25°C		1.4	1.9		1.4	1.9	ns
		T_A = 0°C to +70°C		1.6	2.2				
		T_A = -55°C to +125°C					1.9	2.6	
Latch-Enable to Output High (Notes 2, 3)	$t_{pd+}(E)$	T_A = +25°C		1.3	1.8		1.3	1.8	ns
		T_A = 0°C to +70°C		1.4	2.0				
		T_A = -55°C to +125°C					1.5	2.0	
Latch-Enable to Output Low (Notes 2, 3)	$t_{pd-}(E)$	T_A = +25°C		1.4	1.8		1.3	1.8	ns
		T_A = 0°C to +70°C		1.6	1.9				
		T_A = -55°C to +125°C					1.7	2.6	
Latch-Enable Pulse Width (Note 2)	$t_{pw}(E)$		3.0	2.0		3.0	2.0		ns
Minimum Setup Time	t_s			0.5	1.0		0.5	1.0	
Minimum Hold Time	t_h			0.5	1.0		0.5	1.0	

Note 2: Not tested, guaranteed by design.
Note 3: V_{IN} = 100mV, V_{OD} = 10mV.

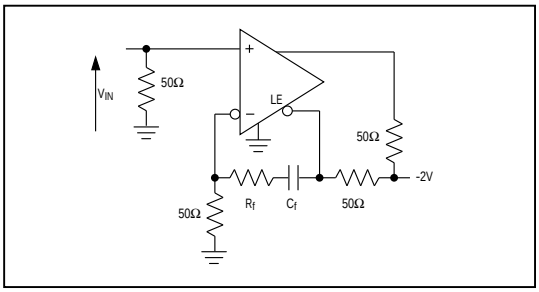


Figure 1. High-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board was used, the minimum slew rate for clean output switching is 1.6V/µs. For sine-wave inputs, this implies a minimum signal size of 360mV$_{RMS}$ at 500MHz and 90mV at 2MHz.

$$E_{RMS} = \frac{Slew\ Rate}{2\sqrt{2}\pi f}$$

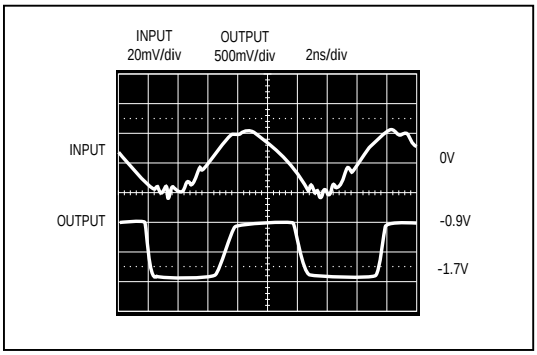


Figure 2. As a high-speed receiver, the MAX9687 is capable of processing signals in excess of 600MHz. Figure 2 is a 100MHz example with an input signal level of 14mV$_{RMS}$.

Applications Information

Layout

Because of the MAX9687's large gain-bandwidth characteristic, special precautions need to be taken if its high-speed capabilities are to be used. A PC board with a ground plane is mandatory. Mount all decoupling capacitors as close to the power-supply pins as possible, and process the ECL outputs in microstrip fashion, consistent with the load termination of 50Ω to 120Ω. For low-impedance applications, microstrip layout at the input may also be helpful. Pay close attention to the bandwidth of the decoupling and terminating components. Chip components can be used to minimize lead inductance.

Input Slew-Rate Requirement

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain

minimum slew-rate requirements. The tendency of the part to oscillate is a function of the layout and source impedance of the circuit employed. Both poor layout and larger source impedance will increase the minimum slew-rate specification.

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew-rate requirement considerably. For example, with the addition of positive feedback components Rf = 1kΩ and Cf = 10pF, the minimum slew-rate requirement can be reduced by a factor of four.

Timing Diagram

The timing diagram (Figure 3) illustrates the series of events that complete the compare function, under worst-case conditions.

The top line of the diagram illustrates two latch-enable (LE) pulses; each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function in which part of the input action takes place during the compare mode. The second pulse demonstrates a compare-function interval during which there is no change in the input.

The leading edge of the input signal (illustrated as a large-amplitude, small-overdrive pulse) switches the comparator after time interval t_{pd}. Outputs Q and $\overline{Q}$ are similar in timing. The input signal must occur at time t_S before the latch falling edge and, to be acquired, must be maintained for time t_h after the edge. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{pw}(E)$ is needed for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

Definition of Terms

V_{OS} — Input Offset Voltage—The voltage required between the input terminals to obtain 0V differential at the output.

V_{IN} — Input Voltage Pulse Amplitude

V_{OD} — Input Voltage Overdrive

t_{pd+} — Input to Output High Delay—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low-to-high transition.

t_{pd-} — Input to Output Low Delay—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high-to-low transition.

$t_{pd+}(E)$ — Latch-Enable to Output High Delay—The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output low-to-high transition.

$t_{pd-}(E)$ — Latch-Enable to Output Low Delay—The propagation delay measured from the 50% point of the latch-enable signal low-to-high transition to the 50% point of an output high-to-low transition.

$t_{pw}(E)$ — Minimum Latch-Enable Pulse Width—The minimum time the latch-enable signal must be high to acquire and hold an input signal.

t_S — Minimum Setup Time—The minimum time before the negative transition of the latch-enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h — Minimum Hold Time—The minimum time after the negative transition of the latch-enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

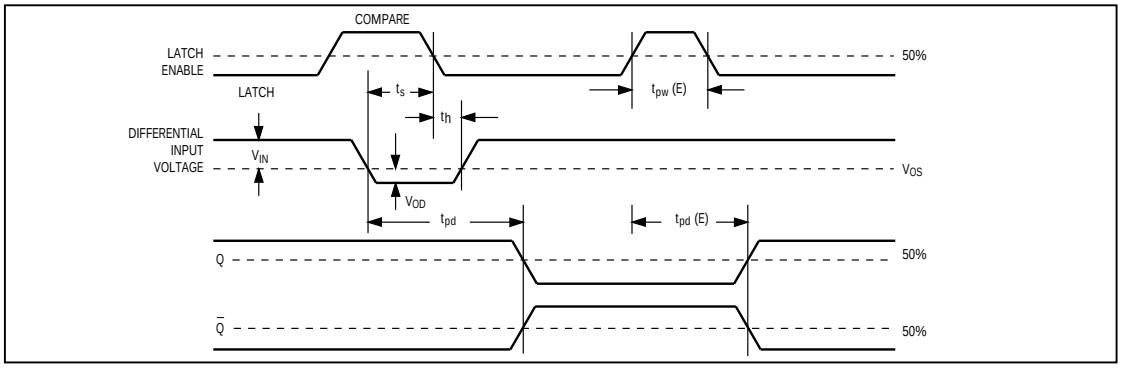


Figure 3. Timing Diagram