

# MC10E131, MC100E131

## 5V ECL 4-Bit D Flip-Flop

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock ( $C_C$ ) LOW and using the Clock Enable ( $\overline{CE}$ ) inputs for clocking. Common clocking is achieved by holding the  $\overline{CE}$  inputs LOW and using  $C_C$  to clock all four flip-flops. In this case, the  $\overline{CE}$  inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both  $C_C$  and  $\overline{CE}$  are LOW, and transfers to the slave when either  $C_C$  or  $\overline{CE}$  (or both) go HIGH.

The 100 Series contains temperature compensation.

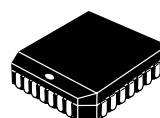
- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- PECL Mode Operating Range:  $V_{CC}= 4.2\text{ V to } 5.7\text{ V}$  with  $V_{EE}= 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC}= 0\text{ V}$  with  $V_{EE}= -4.2\text{ V to } -5.7\text{ V}$
- Internal Input Pulldown Resistors
- Metastability Time Constant is 200 ps.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection:  $> 2\text{ KV HBM, } > 200\text{ V MM}$
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 240 devices



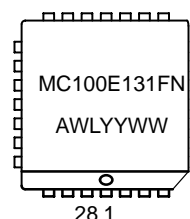
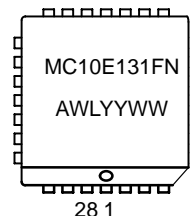
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### MARKING DIAGRAMS



PLCC-28  
FN SUFFIX  
CASE 776



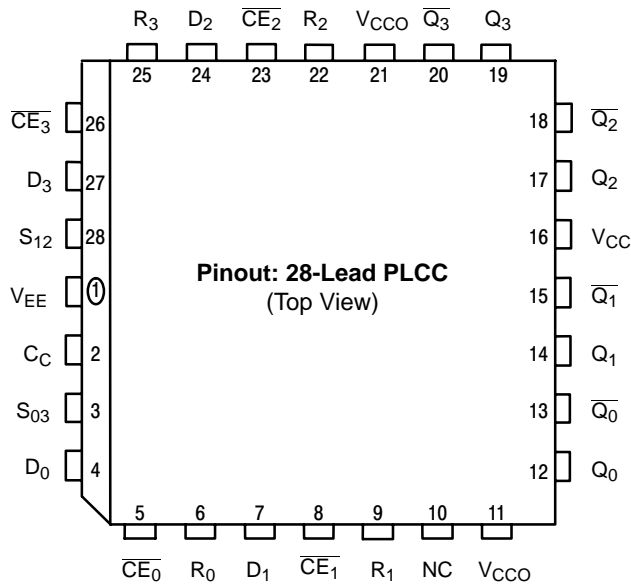
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10E131FN	PLCC-28	37 Units/Rail
MC10E131FNR2	PLCC-28	500 Units/Reel
MC100E131FN	PLCC-28	37 Units/Rail
MC100E131FNR2	PLCC-28	500 Units/Reel

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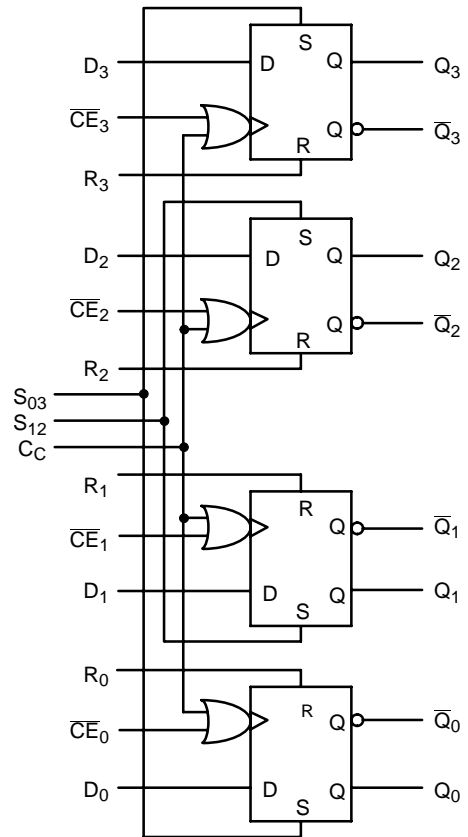
## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



\* All  $V_{CC}$  and  $V_{CC0}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CC0}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

## LOGIC DIAGRAM



## PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_3$	ECL Data Inputs
$\overline{CE}_0 - \overline{CE}_3$	ECL Clock Enables (Individual)
$R_0 - R_3$	ECL Resets
$C_C$	ECL Common Clock
$S_{03}, S_{12}$	ECL Sets (paired)
$Q_0 - Q_3, \overline{Q}_0 - \overline{Q}_3$	ECL Differential Outputs
$V_{CC}, V_{CC0}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect

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## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V <sub>EE</sub>	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V V
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 10E SERIES PECL DC CHARACTERISTICS V<sub>CCx</sub>= 5.0 V; V<sub>EE</sub>= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V <sub>IH</sub>	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V <sub>IL</sub>	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I <sub>IH</sub>	Input HIGH Current			350 450 300 150			350 450 300 150			350 450 300 150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.06 V.
- Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

## 10E SERIES NECL DC CHARACTERISTICS V<sub>CCx</sub>= 0.0 V; V<sub>EE</sub>= -5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2.)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2.)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V <sub>IH</sub>	Input HIGH Voltage	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V <sub>IL</sub>	Input LOW Voltage	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
I <sub>IH</sub>	Input HIGH Current			350 450 300 150			350 450 300 150			350 450 300 150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.06 V.
- Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

# MC10E131, MC100E131

## 100E SERIES PECL DC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$ ; $V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		58	70		58	70		67	81	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
$V_{IH}$	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
$V_{IL}$	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
$I_{IH}$	Input HIGH Current			350 450 300 150			350 450 300 150			350 450 300 150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

## 100E SERIES NECL DC CHARACTERISTICS $V_{CCx}=0.0\text{ V}$ ; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		58	70		58	70		67	81	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
$V_{IH}$	Input HIGH Voltage	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
$V_{IL}$	Input LOW Voltage	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
$I_{IH}$	Input HIGH Current			350 450 300 150			350 450 300 150			350 450 300 150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

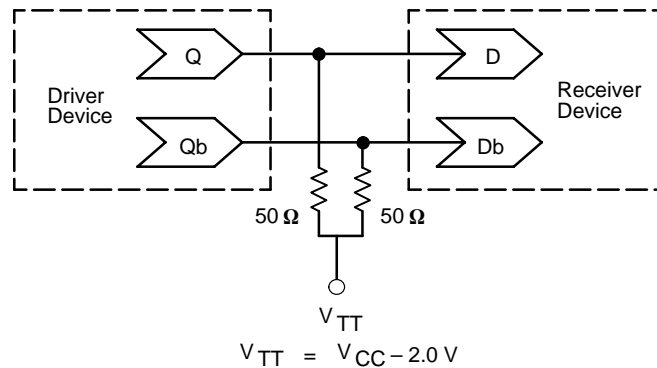
1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

# MC10E131, MC100E131

**AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1.)

Symbol	Characteristic		-40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency			TBD			TBD		TBD		MHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	$\overline{CE}$ $C_C$ R S	310 275 300 300	600 600 625 550	750 725 775 775	360 325 350 350	500 500 550 550	700 675 725 725	360 325 350 350	500 500 550 550	700 675 725 725	ps
$t_S$	Setup Time (Note 2.)	D	200	20		150	20		150	20		ps
$t_H$	Hold Time (Note 2.)	D	225	-20		175	-20		175	-20		ps
$t_{RR}$	Reset Recovery Time		450	150		400	150		400	150		ps
$t_{PW}$	Minimum Pulse Width	CLK R, S	400 400			400 400			400 400			ps
$t_{SKEW}$	Within-Device Skew (Note 3.)			60			60			60		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter			TBD			TBD			TBD		ps
$t_r/t_f$	Rise/Fall Time (20–80%)		275	460	725	300	480		300	480	675	ps

- 10 Series:  $V_{EE}$  can vary +0.46 V / -0.06 V.  
100 Series:  $V_{EE}$  can vary +0.46 V / -0.8 V.
- Setup/hold times guaranteed for both  $C_C$  and  $\overline{CE}$ .
- Within-device skew is defined as identical transitions on similar paths through a device.



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

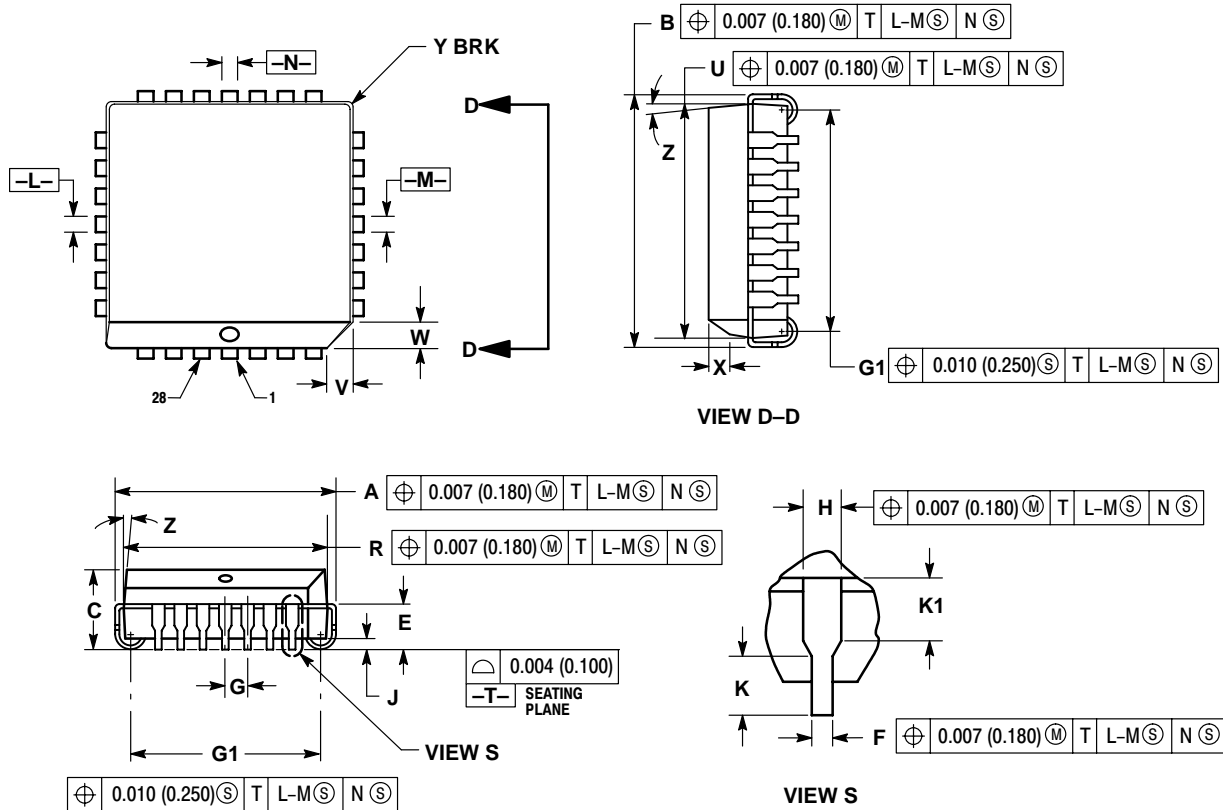
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non–Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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