

# MC10EP32, MC100EP32

## 3.3V / 5V ECL ÷ 2 Divider

The MC10/100EP32 is an integrated ÷2 divider with differential CLK inputs.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP32's in a system.

The 100 Series contains temperature compensation.

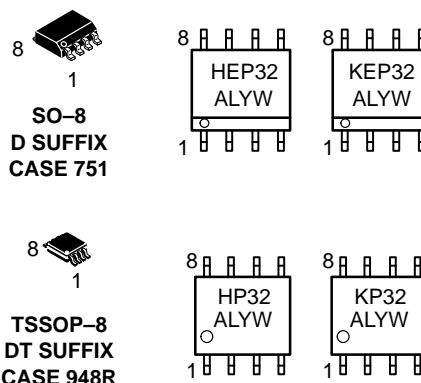
- 350 ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical (See Graph)
- PECL Mode Operating Range:  $V_{CC}$  = 3.0 V to 5.5 V with  $V_{EE}$  = 0 V
- NECL Mode Operating Range:  $V_{CC}$  = 0 V with  $V_{EE}$  = -3.0 V to -5.5 V
- Internal Input Resistors: Pulldown on D,  $\bar{D}$
- Q Output will default LOW with inputs open or at  $V_{EE}$
- ESD Protection: >4 KV HBM, >200 V MM, >2 KV CDM
- $V_{BB}$  Output
- New Differential Input Common Mode Range
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 78 devices



ON Semiconductor™

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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
K = MC100                    Y = Year  
A = Assembly Location      W = Work Week

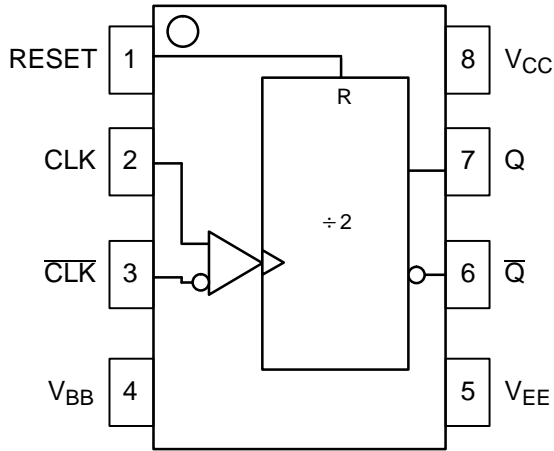
\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC10EP32D	SO-8	98 Units/Rail
MC10EP32DR2	SO-8	2500 Tape & Reel
MC100EP32D	SO-8	98 Units/Rail
MC100EP32DR2	SO-8	2500 Tape & Reel
MC10EP32DT	TSSOP-8	98 Units/Rail
MC10EP32DTR2	TSSOP-8	2500 Tape & Reel
MC100EP32DT	TSSOP-8	98 Units/Rail
MC100EP32DTR2	TSSOP-8	2500 Tape & Reel

# MC10EP32, MC100EP32

## 8-Lead Pinout (Top View) and Logic Diagram



## PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{\text{CLK}}$	ECL Clock Inputs
Reset	ECL Asynchronous Reset
$V_{\text{BB}}$	Reference Voltage Output
Q, $\overline{\text{Q}}$	ECL Data Outputs
$V_{\text{CC}}$	Positive Supply
$V_{\text{EE}}$	Negative Supply

## TRUTH TABLE

CLK	$\overline{\text{CLK}}$	RESET	Q	$\overline{\text{Q}}$
X	X	Z	L	H
Z	Z	L	F	F

Z = LOW to HIGH Transition  
 $\overline{\text{Z}}$  = HIGH to LOW Transition  
 F = Divide by 2 Function

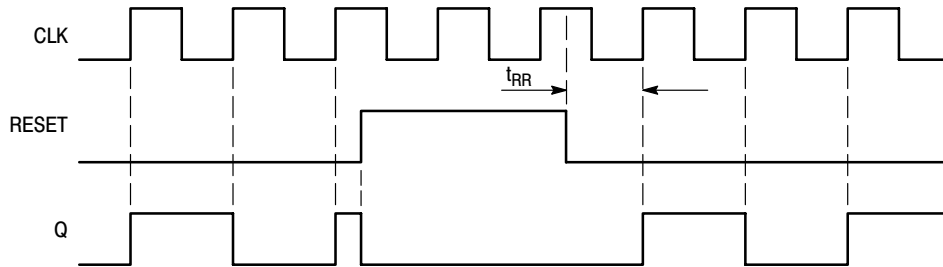


Figure 1. Timing Diagram

## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
$V_{\text{CC}}$	PECL Mode Power Supply	$V_{\text{EE}} = 0 \text{ V}$		6	V
$V_{\text{EE}}$	NECL Mode Power Supply	$V_{\text{CC}} = 0 \text{ V}$		-6	V
$V_{\text{I}}$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{\text{EE}} = 0 \text{ V}$ $V_{\text{CC}} = 0 \text{ V}$	$V_{\text{I}} \leq V_{\text{CC}}$ $V_{\text{I}} \geq V_{\text{EE}}$	6 -6	V V
$I_{\text{out}}$	Output Current	Continuous Surge		50 100	mA mA
$I_{\text{BB}}$	$V_{\text{BB}}$ Sink/Source			$\pm 0.5$	mA
TA	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{\text{JA}}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{\text{JC}}$	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	$^{\circ}\text{C}/\text{W}$
$\theta_{\text{JA}}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{\text{JC}}$	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	$^{\circ}\text{C}/\text{W}$
$T_{\text{sol}}$	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which device damage may occur.

## MC10EP32, MC100EP32

### 10EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	23	30	37	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
$V_{BB}$	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

### 10EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	23	30	37	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{BB}$	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

### 10EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ ; $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	23	30	37	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## MC10EP32, MC100EP32

### 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	26	33	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
$V_{BB}$	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

### 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	26	33	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
$V_{BB}$	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

### 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ ; $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	23	30	37	26	33	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{BB}$	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP32, MC100EP32

**AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 1. $F_{max}/JITTER$ )		3	> 4		3	> 4		3	> 4	GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential 10 Series 100 Series										ps
	CLK to Q, $\bar{Q}$	250	330	420	270	350	450	320	400	480	
	RESET to Q, $\bar{Q}$	220	290	390	250	300	390	320	380	460	
	RESET to Q, $\bar{Q}$	320	400	480	320	400	480	375	450	525	
$t_{RR}$	Set/Reset Recovery	200	175		200	175		200	175		ps
$t_{PW}$	Minimum Pulse width RESET	550	475		550	475		550	475		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (See Figure 1. $F_{max}/JITTER$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) Q, $\bar{Q}$	50	100	150	70	120	170	70	130	200	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC} = 2.0\text{ V}$ .

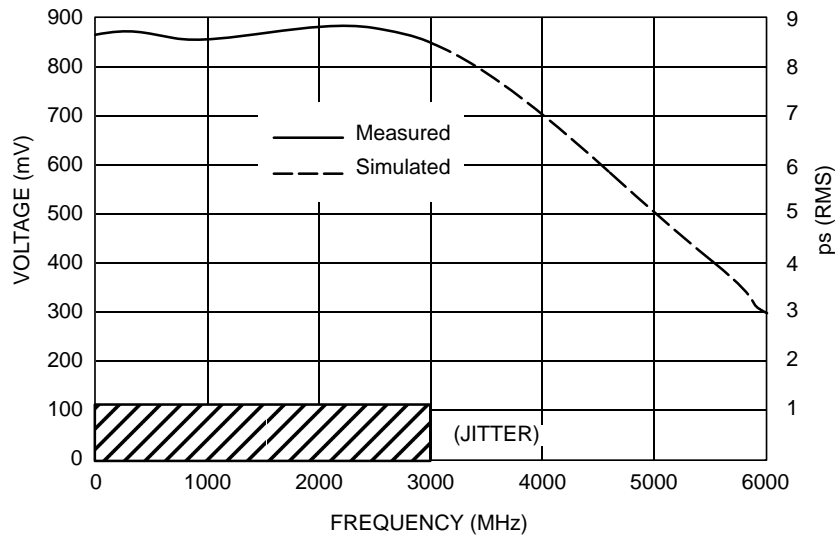
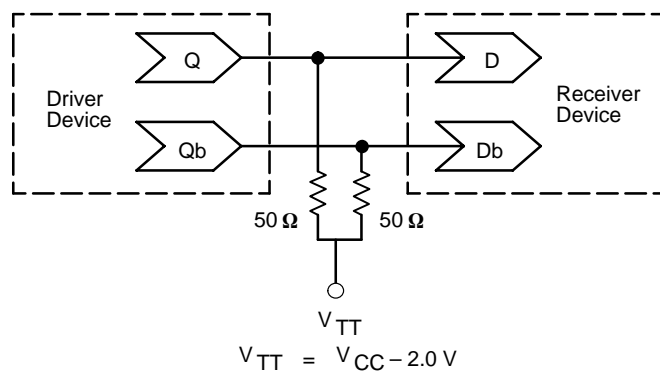


Figure 2.  $F_{max}/Jitter$

## MC10EP32, MC100EP32



**Figure 3 Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

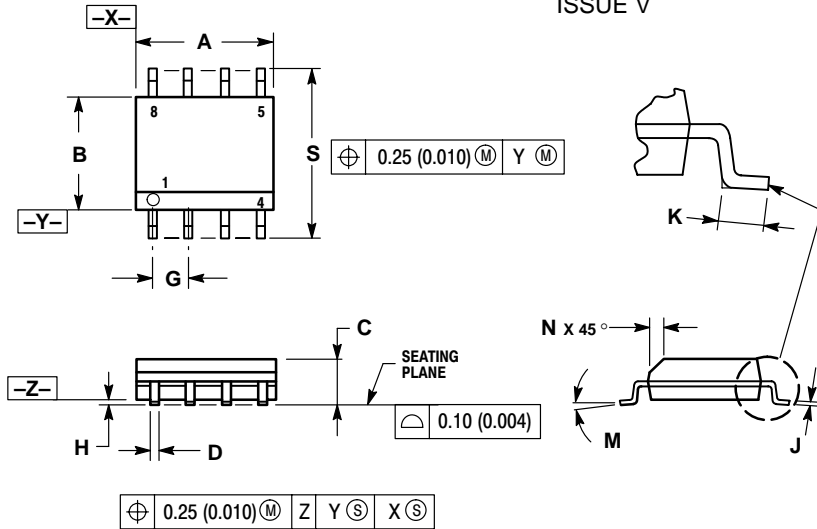
### Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

# MC10EP32, MC100EP32

## PACKAGE DIMENSIONS

### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE V

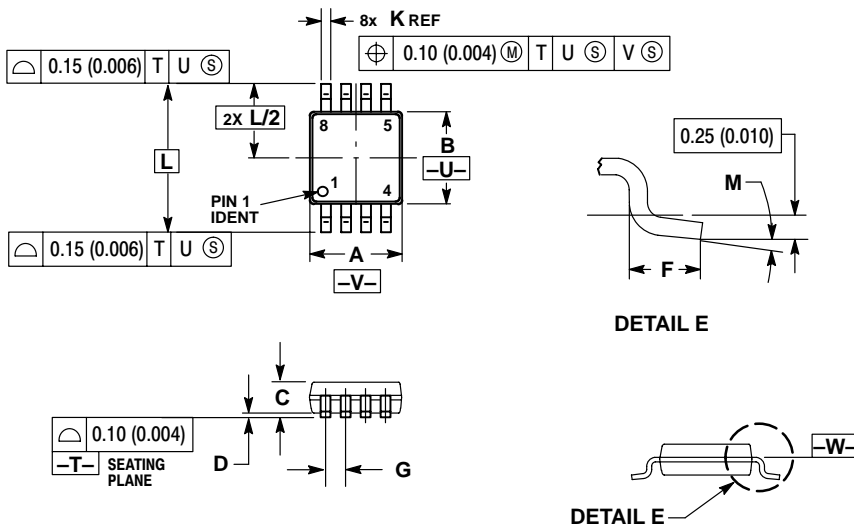


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### TSSOP-8 DT SUFFIX CASE 948R-02 ISSUE A



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC10EP32, MC100EP32

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