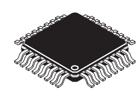
Order Number: MC100ES6254/D
Rev 1, 05/2002

2.5/3.3V Differential LVPECL 2x2 Clock Switch and Fanout Buffer

MC100ES6254

2.5V/3.3V DIFFERENTIAL LVPECL 2x2 CLOCK SWITCH AND FANOUT BUFFER



FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A

The Motorola MC100ES6254 is a bipolar monolithic differential 2x2 clock switch and fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6254 supports various applications that require to drive precisely aligned clock signals. The device is capable of driving and switching differential LVPECL signals. Using SiGe technology and a fully differential architecture, the device offers superior digitial signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock/data switching, clock distribution or data loopback in computing, networking and telecommunication systems.

Features:

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation[1] of clock or data signals
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- 50 ps maximum device skew[1]
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range

Functional Description

MC100ES6254 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6254 are primary clock distribution, switching and loopback systems of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems. Primary purpose of the MC100ES6254 is high–speed clock switching applications. In addition, the MC100ES6254 can be configured as single 1:6 or dual 1:3 LVPECL fanout buffer for clock signals, or as loopback device in high–speed data applications.

The MC100ES6254 can be operated from a 3.3V or 2.5V positive supply without the requirement of a negative supply line.

1. The device is functional up to 3 GHz and characterized up to 2.7 GHz.

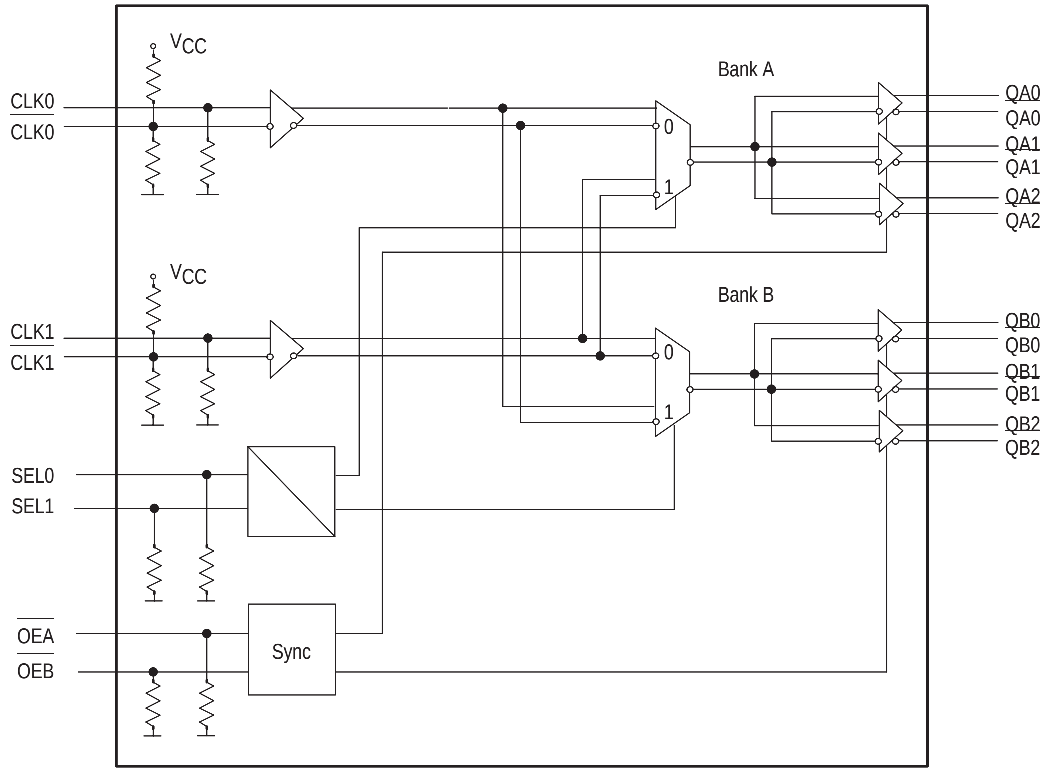


Figure 1. MC100ES6254 Logic Diagram

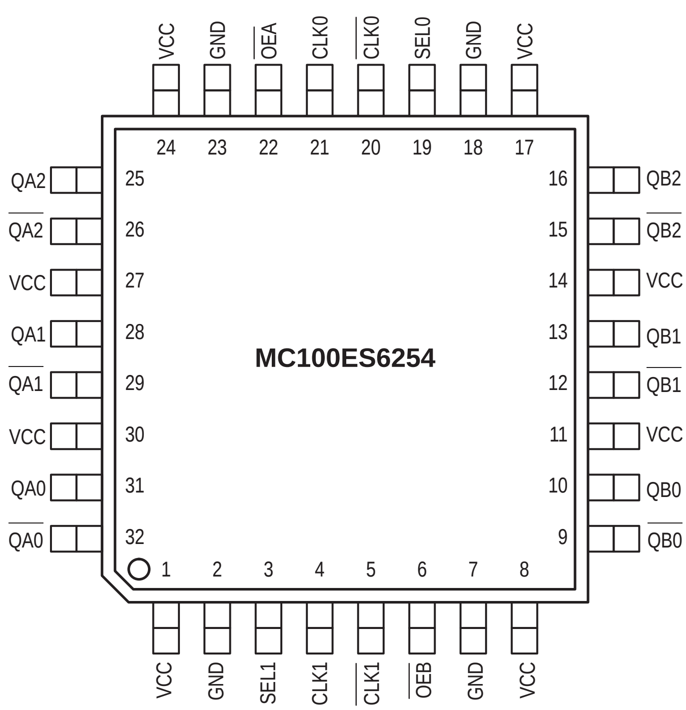


Figure 2. 32–Lead Package Pinout (Top View)

TABLE 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	LVPECL	Differential reference clock signal input 0
CLK1, $\overline{\text{CLK1}}$	Input	LVPECL	Differential reference clock signal input 1
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	Input	LVCMOS	Output enable
SEL0, SEL1	Input	LVCMOS	Clock switch select
QA[0-2], $\overline{\text{QA[0-2]}}$ QB[0-2], QB[0-2]	Output	LVPECL	Differential clock outputs (banks A and B)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	VCC	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation

TABLE 2: FUNCTION TABLE

Control	Default	0	1
$\overline{\text{OEA}}$	0	QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	QA[0-2] = L, $\overline{\text{QA[0-2]}}$ =H (outputs disabled). Assertion of OE can be asynchronous to the reference clock without generation of output runt pulses
$\overline{\text{OEB}}$	0	QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	QA[0-2] = L, $\overline{\text{QA[0-2]}}$ =H (outputs disabled). Assertion of OE can be asynchronous to the reference clock without generation of output runt pulses
SEL0, SEL1	00	See Table 3	

TABLE 3: CLOCK SELECT CONTROL

SEL0	SEL1	CLK0 routed to	CLK1 routed to	Application Mode
0	0	QA[0:2] and QB[0:2]	—	1:6 fanout of CLK0
0	1	—	QA[0:2] and QB[0:2]	1:6 fanout of CLK1
1	0	QA[0:2]	QB[0:2]	Dual 1:3 buffer
1	1	QB[0:2]	QA[0:2]	Dual 1:3 buffer (crossed)

TABLE 4: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

TABLE 5: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} - 2[a]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1500			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature[b] (continuous operation) MTBF = 9.1 years			110	°C	
T_{Func}	Functional temperature range	T_A=–40		T_J=+110	°C	

a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase.
b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6254 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6254 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

TABLE 6: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_J = 0° to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{OEA}$, $\overline{OEB}$, SEL0, SEL1)						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current[a]			±100	µA	$V_{IN} = V_{CC}$ or V_{IN} = GND
LVPECL clock inputs (CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$)						
V_{PP}	AC differential input voltage[b]	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[c]	1.0		V_{CC}-0.3	V	Differential operation
LVPECL clock outputs (QA0-2, $\overline{QA0-2}$, QB0-2, $\overline{QB0-2}$)						
V_{OH}	Output High Voltage	V_{CC}-1.2	V_{CC}-1.005	V_{CC}-0.7	V	I_{OH} = –30 mA[d]
V_{OL}	Output Low Voltage V_{CC}=3.3V±5% V_{CC}=2.5V±5%	V_{CC}-1.9 V_{CC}-1.9	V_{CC}-1.705 V_{CC}-1.705	V_{CC}-1.5 V_{CC}-1.3	V	I_{OL} = –5 mA[e]
I_{GND}	Maximum Quiescent Supply Current without output termination current		52	85	mA	GND pin

a. Input have internal pullup/pulldown resistors which affect the input current.
b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
d. Equivalent to a termination 50Ω to V_{TT}.
e. I_{CC} calculation: I_{CC} = (number of differential output pairs used) * ($I_{OH} + I_{OL}$) + I_{GND}
I_{CC} = (number of differential output pairs used) * (V_{OH}–V_{TT}) ÷ R_{load} +(V_{OL}–V_{TT}) ÷ R_{load}) + I_{GND}

TABLE 7: AC CHARACTERISTICS (V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_J = 0° to +110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential input voltage[b] (peak-to-peak)	0.3		1.3	V	
V_{CMR}	Differential input crosspoint voltage[c]	1.2		V_{CC}-0.3	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) f_O < 1.1 GHz f_O < 2.5 GHz f_O < 3.0 GHz	 0.45 0.35 0.20	 0.7 0.55 0.35		 V V V	
f_{CLK}	Input Frequency	0		3000[d]	MHz	
t_{PD}	Propagation delay CLK, 1 to QA[] or QB[]	485	360	610	ps	Differential
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			250	ps	Differential
$t_{SK(P)}$ DC_O	Output pulse skew[e] Output duty cycle t_{REF}<100 MHz t_{REF}<800 MHz	 49.4 45.2		60 50.6 54.8	ps % %	 DC_{fref}= 50% DC_{fref}= 50%
$t_{JIT(CC)}$	Output cycle-to-cycle jitter (SEL0 ≠ SEL1)			TBD		
t_r, t_f	Output Rise/Fall Time	0.05		300	ps	20% to 80%
t_{PDLf}	Output disable time	2.5·T + t_{PD}		3.5·T + t_{PD}	ns	T=CLK period
t_{PLDg}	Output enable time	3·T + t_{PD}		4·T + t_{PD}	ns	T=CLK period

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
d. The MC100ES6254 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
e. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.
f. Propagation delay OE deassertion to differential output disabled (differential low: true output low, complementary output high).
g. Propagation delay OE assertion to output enabled (active).

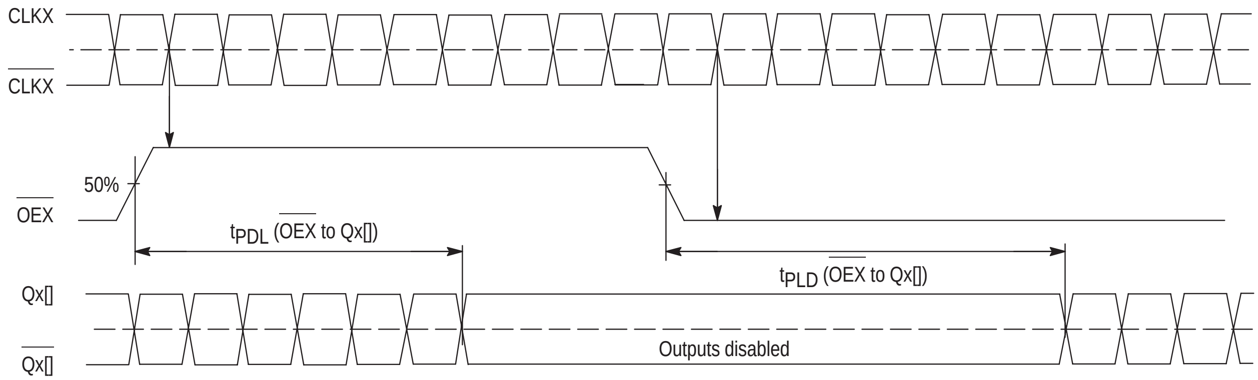


Figure 3. MC100ES6254 output disable/enable timing

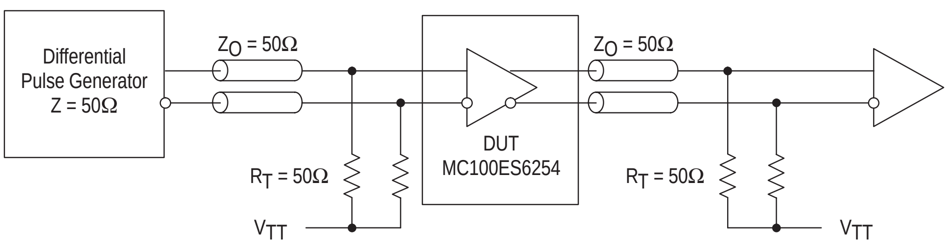
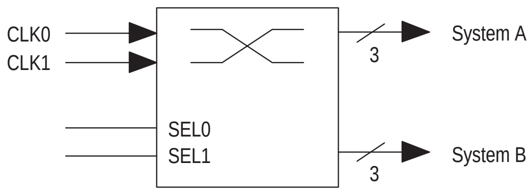


Figure 4. MC100ES6254 AC test reference

APPLICATIONS INFORMATION

Example Configurations

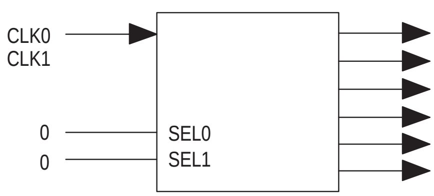
2x2 clock switch



MC100ES6254

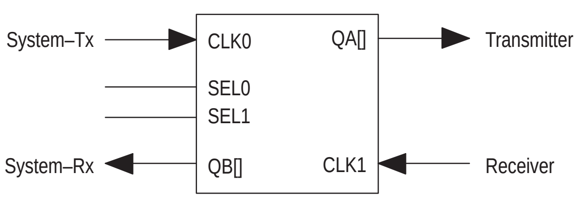
SEL0	SEL1	Switch configuration
0	0	CLK0 clocks system A and system B
0	1	CLK1 clocks system A and system B
1	0	CLK0 clocks system A and CLK1 clocks system B
1	1	CLK1 clocks system B and CLK1 clocks system A

1:6 Clock Fanout Buffer



MC100ES6254

Loopback device



MC100ES6254

SEL0	SEL1	Switch configuration
0	0	System loopback
0	1	Line loopback
1	0	Transmit / Receive operation
1	1	System and line loopback

Understanding the junction temperature range of the MC100ES6254

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6254, the MC100ES6254 is specified, characterized and tested for the junction temperature range of T_J=0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4 °C/W (2s2p board, 200 ft/min airflow, see table 4) and a typical power consumption of 467 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC}=3.3V, frequency independent), the junction temperature of the MC100ES6254 is approximately T_A + 24.5 °C, and the minimum ambient temperature in this example case calculates to -24.5 °C (the maximum ambient temperature is 85.5 °C. See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6254 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6254 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8: Ambient temperature ranges (P_{tot} = 467 mW)

R_{thja} (2s2p board)		$T_{A, min}$[a]	$T_{A, max}$
Natural convection	59.0 °C/W	-28 °C	82 °C
100 ft/min	54.4 °C/W	-25 °C	85 °C
200 ft/min	52.5 °C/W	-24.5 °C	85.5 °C
400 ft/min	50.4 °C/W	-23.5 °C	86.5 °C
800 ft/min	47.8 °C/W	-22 °C	88 °C

a. The MC100ES6254 device function is guaranteed from T_A=-40 °C to T_J=110 °C

Maintaining Lowest Device Skew

The MC100ES6254 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6254 is a mixed analog/digital product. The differential architecture of the MC100ES6254 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

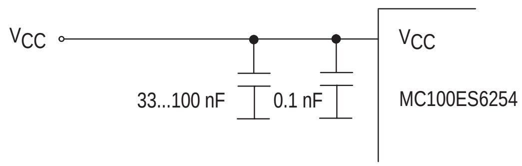
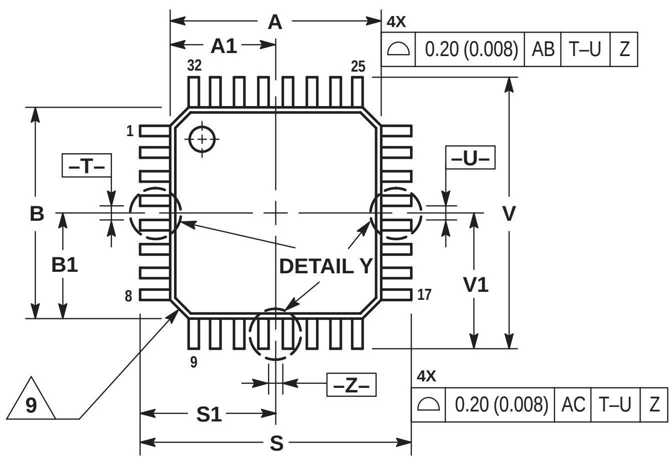
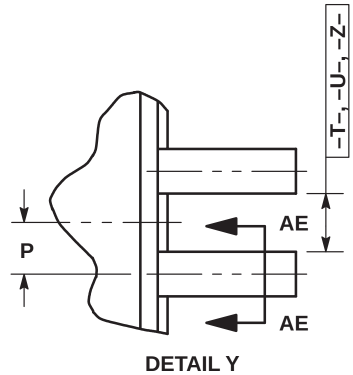


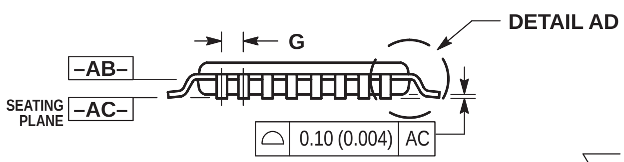
Figure 5. V_{CC} Power Supply Bypass

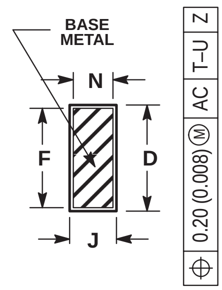
OUTLINE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 873A-02
ISSUE A

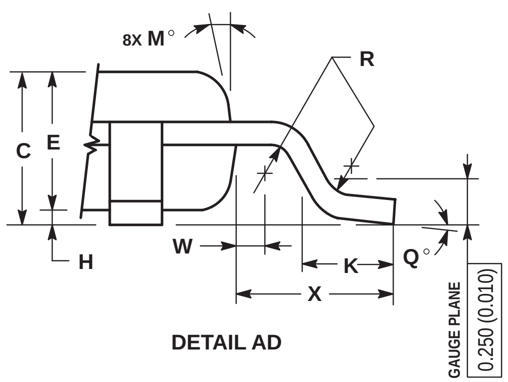








SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

NOTES

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