

### Quad Bus Receiver

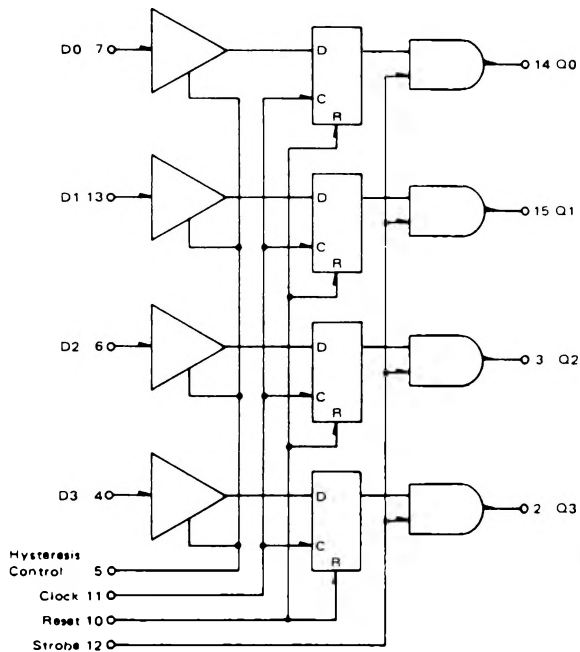
The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept MTTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches

will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to  $V_{CC}$  or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pull-down resistors to  $V_{EE}$ . They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.



TRUTH TABLE

| D      | C      | STROBE | RESET  | $Q_{n+1}$ |
|--------|--------|--------|--------|-----------|
| $\phi$ | $\phi$ | L      | $\phi$ | L         |
| L      | L      | H      | $\phi$ | L         |
| H      | H      | L      | $\phi$ | L         |
| $\phi$ | $\phi$ | H      | $\phi$ | $Q_n$     |

$\phi$  = Don't Care

$V_{CC}$  = Pin 9  
 Gnd = Pins 1 and 16  
 $V_{EE}$  = Pin 8

$P_D$  = 750 mW typ/pkg (No Load)  
 $t_{pd}$  = 10 ns typ

MC10129

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