TRUTH TABLE

$D = (A \cdot D11) + (A \cdot D12)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

Dual Multiplexer with Latch and Common Reset

The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

MC10132

LATCHES