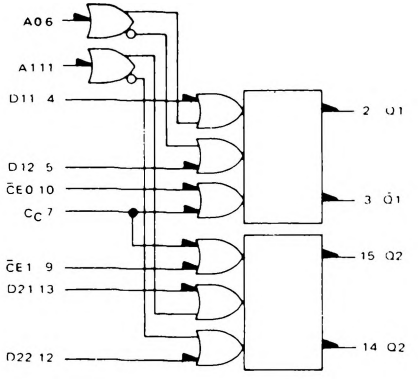

TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	Φ	L
L	L	H	Φ	H
L	H	Φ	L	L
L	H	Φ	H	H
H	Φ	Φ	Φ	Q_n

Φ = Don't Care
C = C̄E • CC

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

Dual Multiplexer with Latch

The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable (C̄E) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (CC).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.