CLOCK J-K TRUTH TABLE*

J	K	Q_{n+1}
L	L	Q_n
H	L	L
L	H	H
H	H	$\overline{Q}_n$

*Output states change on positive transition of clock for J-K input condition present.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. Not Defined

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D — 280 mW typ/pkg (No Load)
f_{Tog} — 140 MHz typ

Dual J-K Master-Slave Flip-Flop

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs overide the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.