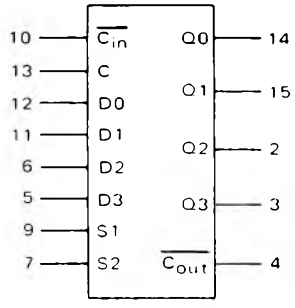
Universal Decade Counter

The MC10137 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This decade counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the present mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excersion will depend on the condition of Q1 and/or Q2.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open.) The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is a shown in the State Diagrams.

A prescaler can be constructed using the MC10137 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 1000 MHz prescaler is possible using an MC1699 1GHz divide by 4, an MC12013 500 MHz divide by 10-11, and the MC10137



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	◌	H	H	H	H	L	H
L	H	◌	◌	◌	◌	L	H	L	L	L	H	H
L	H	◌	◌	◌	◌	L	H	H	L	L	H	L
L	H	◌	◌	◌	◌	L	H	L	L	L	L	H
L	H	◌	◌	◌	◌	L	H	H	L	L	L	H
L	H	◌	◌	◌	◌	H	L	H	L	L	L	H
L	H	◌	◌	◌	◌	H	H	H	L	L	L	H
H	H	◌	◌	◌	◌	◌	H	H	L	L	L	H
L	L	H	H	L	L	◌	H	H	H	L	L	H
H	L	◌	◌	◌	◌	L	H	L	H	L	L	H
H	L	◌	◌	◌	◌	L	H	H	L	L	L	H
H	L	◌	◌	◌	◌	L	H	L	L	L	L	L

◌ Don't care

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom

** A clock H is defined as a clock input transition from a low to a high logic level

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 Mhz typ

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)