

Error Detection-Correction Circuit

The MC10163 and the MC10193 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for mainframe and add-on memory systems. For example, using eight MC10163's together with eight 12-bit parity checkers (MC10160), single-bit error

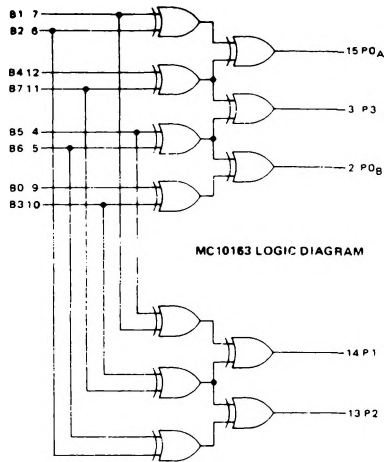
detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B0-B7) need be added to the word. A useful feature of this building block is that the MC10193 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

IBM CODE

P0_A = B1, B2, B4, B7
P0_B = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7

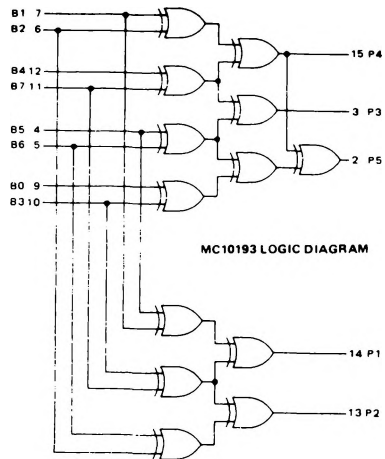
MOTOROLA CODE

P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0, 1, 2, 3, 4, 5, 6, 7)



MC10163 LOGIC DIAGRAM

V_{CC1} = Pin 1
 V_{CC2} = Pin 16
 V_{EE} = Pin 8
 P_D = 250 mW typ/pkg (No Load)
 t_{pd} = 7.5 ns typ (pin 7 to pin 2)



MC10193 LOGIC DIAGRAM

V_{CC1} = Pin 1
 V_{CC2} = Pin 16
 V_{EE} = Pin 8
 P_D = 520 mW typ/gate (No Load)
 t_{pd} = 5.0 ns typ

MC10163 • MC10193

MISCELLANEOUS