MC145146-2

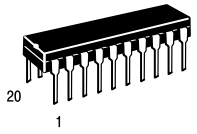
4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

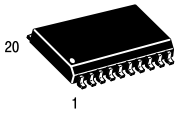
The MC145146–2 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 10–bit programmable divide–by–N counter, 7–bit divide–by–A counter, and the necessary latch circuitry for accepting the 4–bit input data. When combined with a loop filter and VCO, the MC145146–2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a dual–modulus prescaler can be used between the VCO and the MC145146–2.

The MC145146–2 is an improved performance drop–in replacement for the MC145146–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- On– or Off–Chip Reference Oscillator Operation
- Dual–Modulus 4–Bit Data Bus Programming
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- “Linearized” Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  Single–Ended (Three–State)
  Double–Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 738

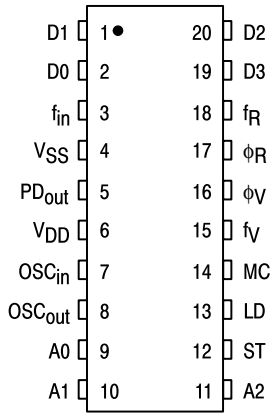


DW SUFFIX
SOG PACKAGE
CASE 751D

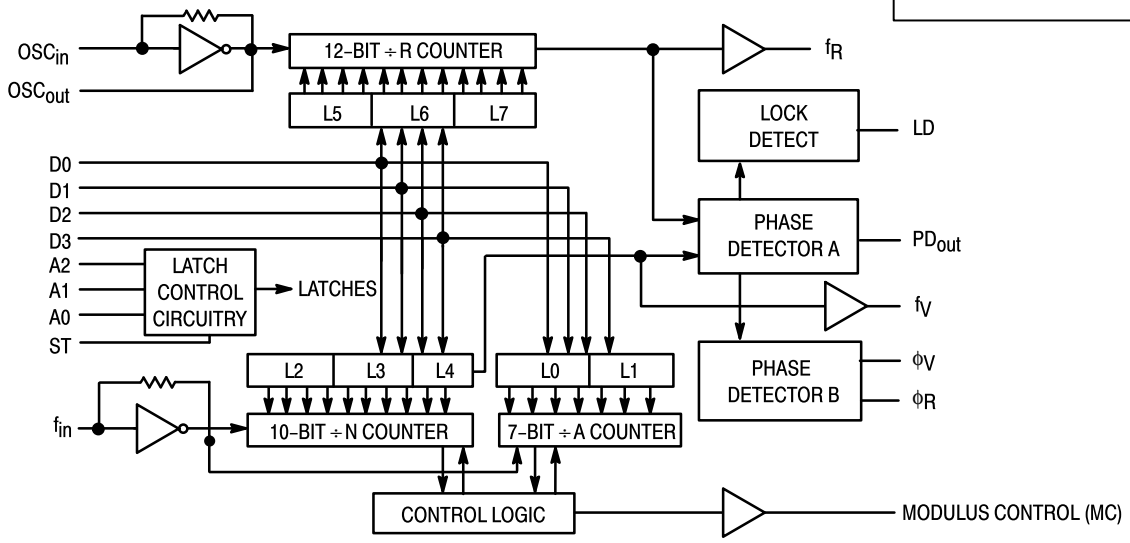
ORDERING INFORMATION

MC145146P2	Plastic DIP
MC145146DW2	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



REV 1
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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: –12 mW/°C from 65 to 85°C
SOG Package: –7.0 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD} V	–40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{SS}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc $V_{out} \ge 3.5$ V coupled $V_{out} \ge 6.3$ V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc $V_{out} \le 1.5$ V coupled $V_{out} \le 2.7$ V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9.0	± 2.0	± 50	± 2.0	± 25	± 2.0	± 22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{SS}$	9.0	—	–0.3	—	–0.1	—	–1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ μA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ μA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low–Level Sinking Current — Modulus Control (MC)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	1.3 1.9 3.8	— — —	1.1 1.7 3.3	— — —	0.66 1.08 2.1	— — —	mA
I_{OH}	High–Level Sourcing Current — Modulus Control (MC)	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.6 −0.9 −1.5	— — —	−0.5 −0.75 −1.25	— — —	−0.3 −0.5 −0.8	— — —	mA
I_{OL}	Low–Level Sinking Current — Lock Detect (LD)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Lock Detect (LD)	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	± 0.3	—	± 0.1	—	± 1.0	μA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC	1, 6	3.0 5.0 9.0	110 60 35	120 70 40	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	2, 6	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	3, 6	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	3, 6	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Set–Up Time, Data to ST	4	3.0 5.0 9.0	10 10 10	— — —	ns
t_{su}	Minimum Set–Up Time, Address to ST	4	3.0 5.0 9.0	25 20 15	— — —	ns

(continued)

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit –40°C to 85°C	Unit
t_h	Minimum Hold Time, Address to ST	4	3.0 5.0 9.0	10 10 10	— — —	ns
t_h	Minimum Hold Time, Data to ST	4	3.0 5.0 9.0	25 20 15	— — —	ns
t_w	Minimum Input Pulse Width, ST	5	3.0 5.0 9.0	40 30 20	— — —	ns

SWITCHING WAVEFORMS

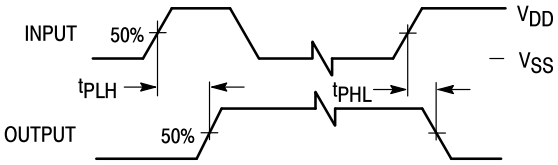
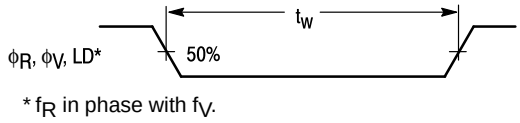


Figure 1.



* f_R in phase with f_V.

Figure 2.

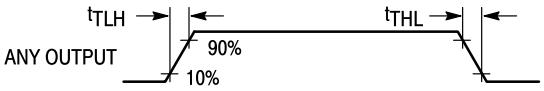


Figure 3.

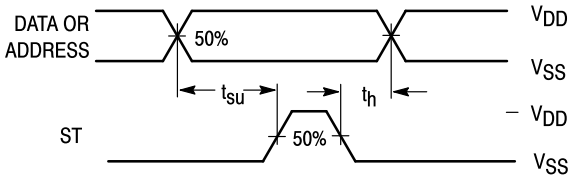


Figure 4.

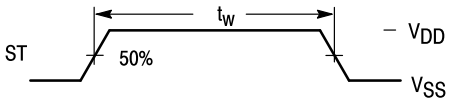
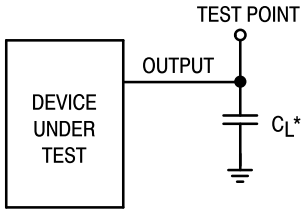


Figure 5.



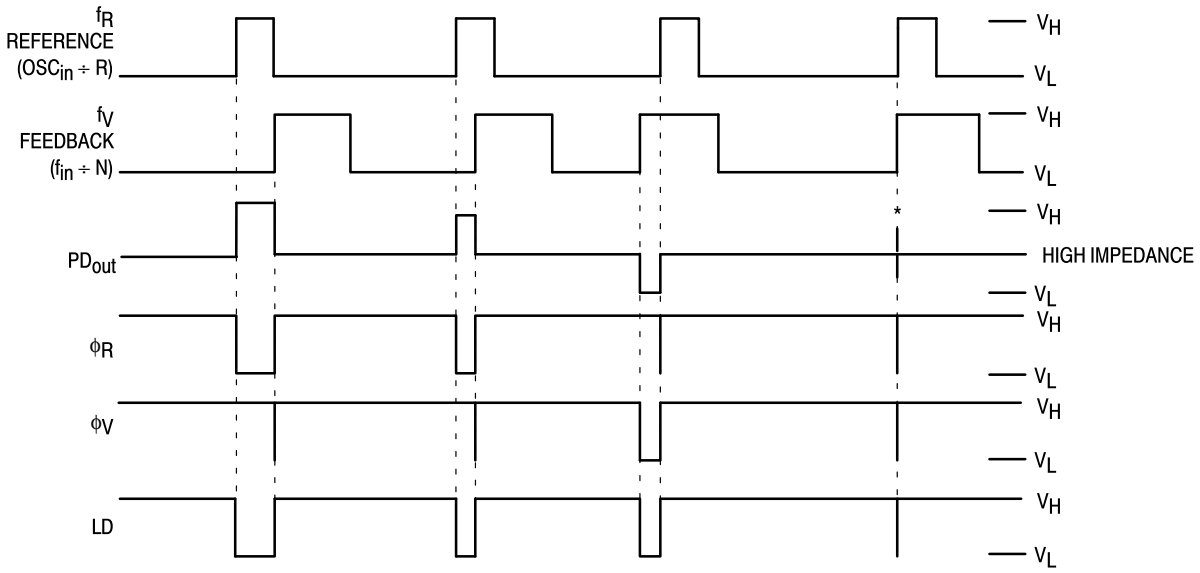
* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise specified)

Symbol	Parameter	Test Conditions	V_{DD} V	–40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1.0 V p–p ac coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 $V_{in} = V_{DD}$ to V_{SS} dc coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the set–up time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_p + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual–modulus prescaler ratios, t_p is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler set–up time in seconds. For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the set–up time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_p + t_{set}) = 64/(70 + 16) = 744$ MHz.



V_H = High voltage level.
V_L = Low voltage level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

INPUT PINS

D0 – D3
Data Inputs (Pins 2, 1, 20, 19)

Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 (Pin 19) is the most significant bit.

f_{in}
Frequency Input (Pin 3)

Input to ÷N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into Pin 3. For larger amplitude signals (standard CMOS–logic levels) dc coupling may be used.

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 7 and 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS–logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

A0 – A2
Address Inputs (Pins 9, 10, 11)

A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷ A Bits	0	1	2	3
0	0	1	Latch 1	÷ A Bits	4	5	6	—
0	1	0	Latch 2	÷ N Bits	0	1	2	3
0	1	1	Latch 3	÷ N Bits	4	5	6	7
1	0	0	Latch 4	÷ N Bits	8	9	—	—
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST
Strobe Transfer (Pin 12)

The rising edge of strobe transfers data into the addressed latch. The falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector Output (Pin 5)

Three–state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

LD
Lock Detector (Pin 13)

High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MC
Modulus Control (Pin 14)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter.

f_V
÷N Counter Output (Pin 15)

This pin is the output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

ϕ_V, ϕ_R
Phase Detector Outputs (Pins 16 and 17)

These phase detector outputs can be combined externally for a loop error signal. A single–ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R
÷R Counter Output (Pin 18)

This is the output of the ÷ R counter that is internally connected to the phase detector input. With this output available, the ÷ R counter can be used independently.

POWER SUPPLY PINS

V_{SS}
Ground (Pin 4)

Circuit Ground.

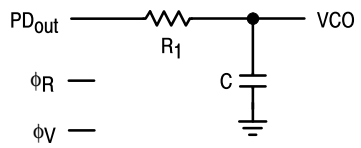
V_{DD}
Positive Power Supply (Pin 6)

The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

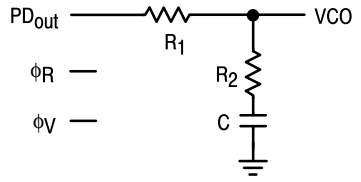


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

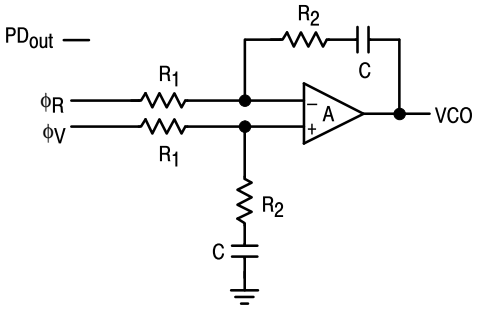


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)\,sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input)

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

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Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

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DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 8.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

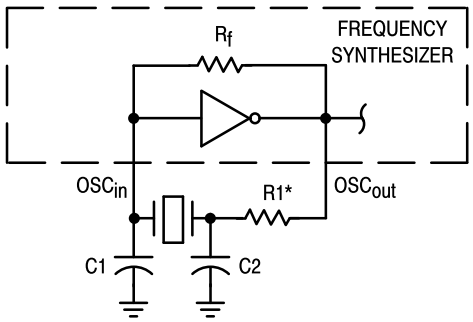
C_{in} = 5.0 pF (see Figure 9)
C_{out} = 6.0 pF (see Figure 9)
C_a = 1.0 pF (see Figure 9)
C_O = the crystal's holder capacitance (see Figure 10)
C1 and C2 = external capacitors (see Figure 8)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 10. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 8 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 ohms).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.



* May be deleted in certain cases. See text.

Figure 8. Pierce Crystal Oscillator Circuit

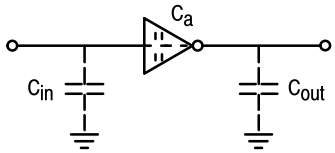
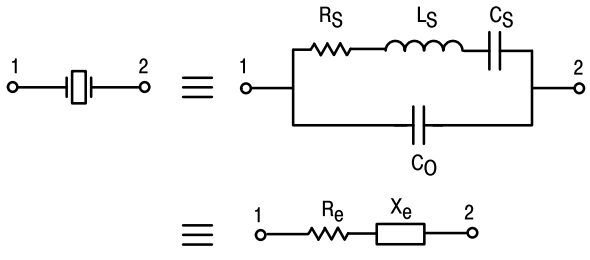


Figure 9. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 10. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145146–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.,

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1) P + A$ or $(P - 1) P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

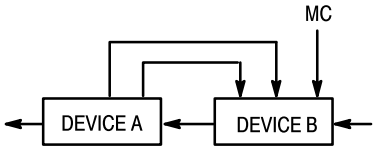
1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, NT, now results when the value of NT in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 11).

APPLICATIONS

The features of the MC145146–2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor–controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

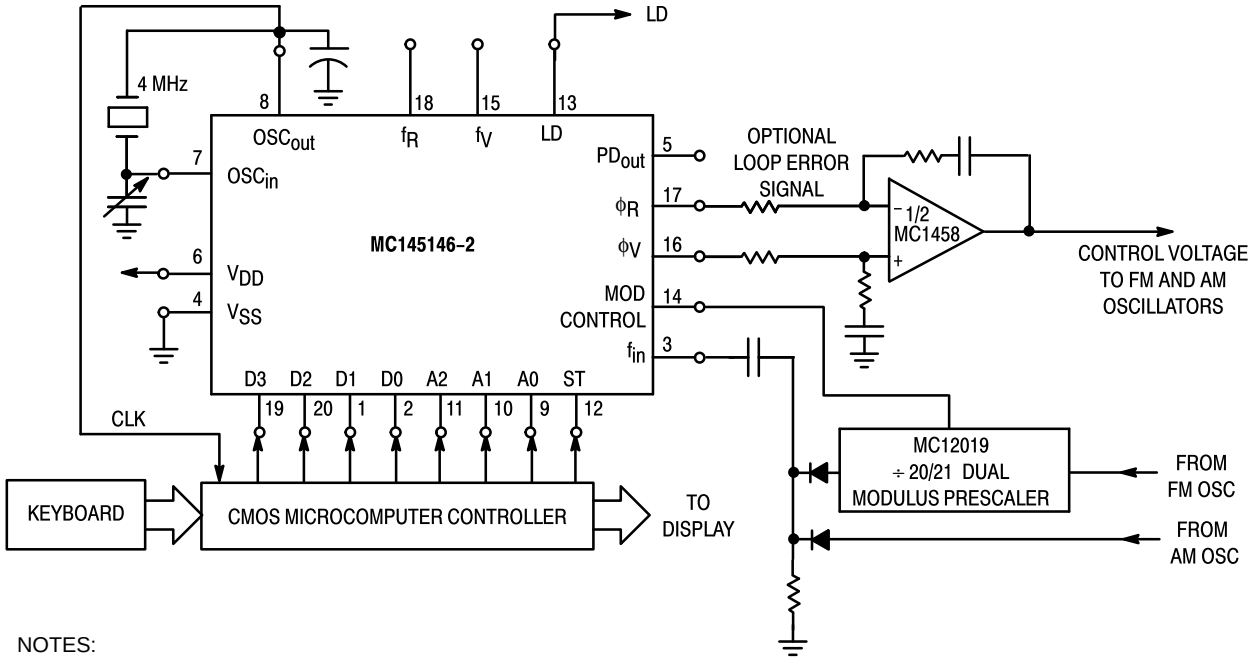
The device architecture allows the user to establish any integer reference divide value between 3 and 4095. The wide selection of +R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that take advantage of these MC145146–2 features including the dual modulus capability are shown in Figures 12, 13, and 14.



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 OR ÷ 80/÷ 81	÷ 64/÷ 65 OR ÷ 128/÷ 129	÷ 80/÷ 81

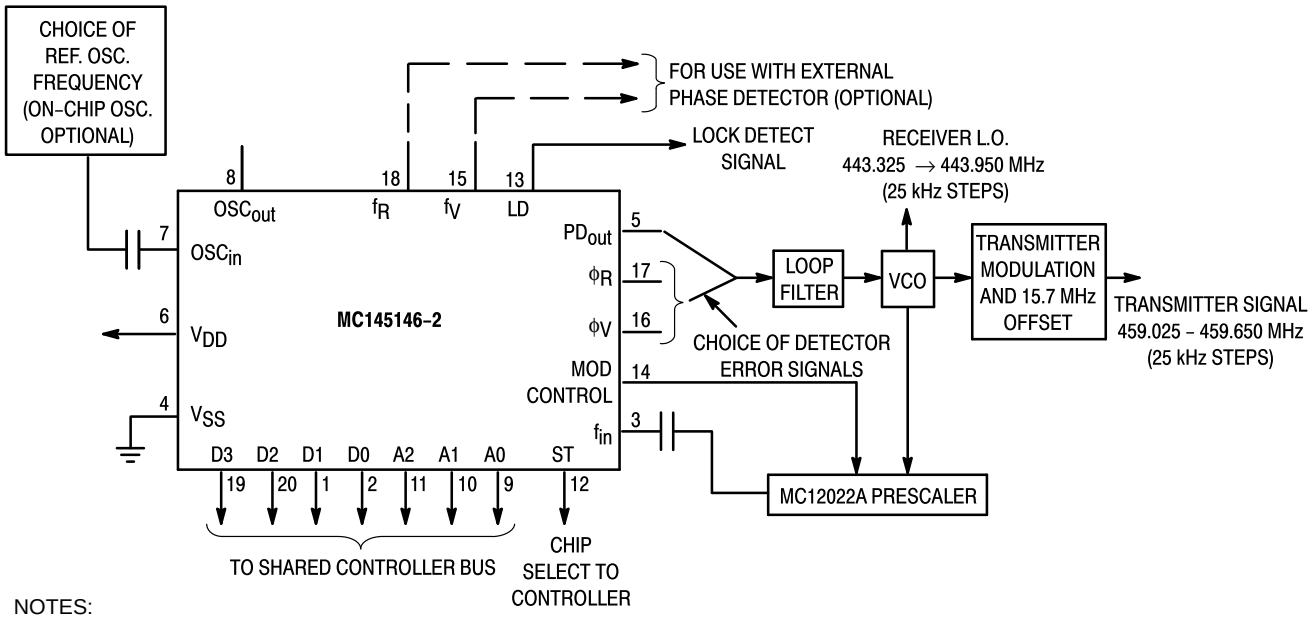
NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 11. Dual Modulus Values



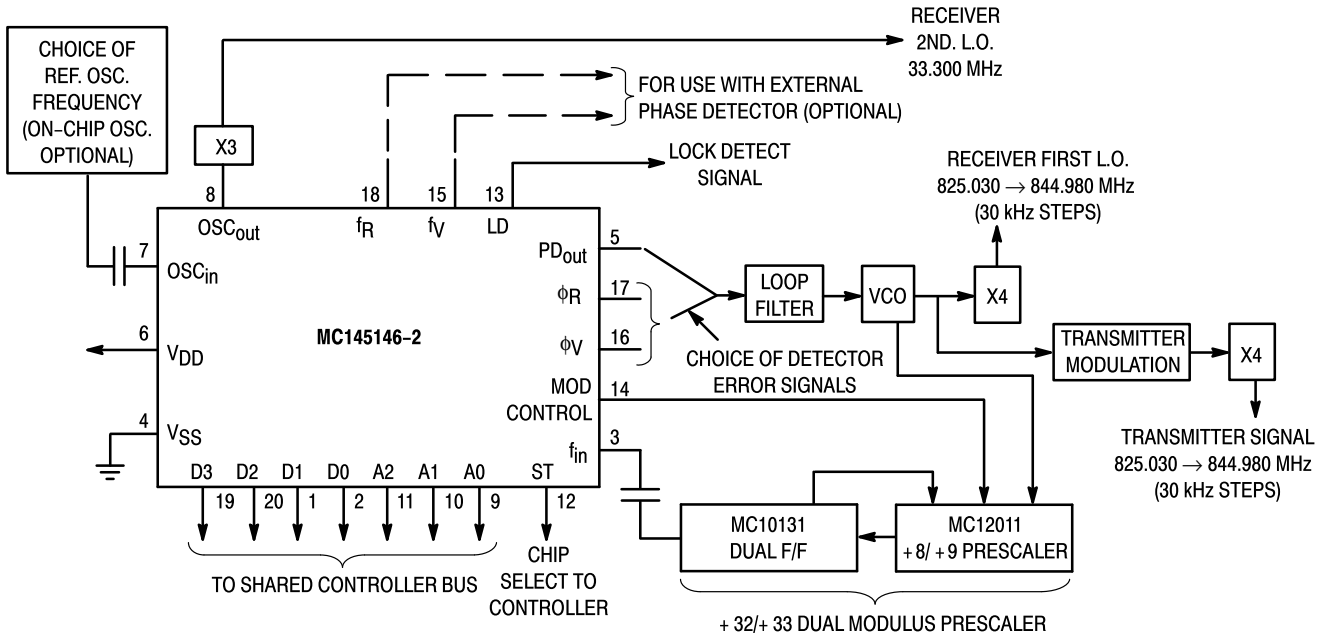
NOTES:
1. For FM: Channel spacing = f_R = 25 kHz, R = 160.
   For AM: Channel spacing = f_R = 1 kHz, R = 4000.
2. Various channel spacings and reference oscillator frequencies can be chosen since any R value from 3 to 4095 can be established.
3. Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

Figure 12. FM/AM Broadcast Radio Synthesizer



NOTES:
1. Receiver I.F. = 10.7 MHz, low side injection.
2. Duplex operation with 5 MHz receive/transmit separation.
3. f_R = 25 kHz, ÷ R chosen to correspond with desired reference oscillator frequency.
4. N_{total} = 17,733 to 17,758 = N • P + A; N = 277, A = 5 to 30 for P = 64.

Figure 13. Synthesizer for UHF Mobile Radio Telephone Channels Demonstrates Use of the MC145146–2 in Microprocessor/Microcomputer Controlled Systems Operating to Several Hundred MHz

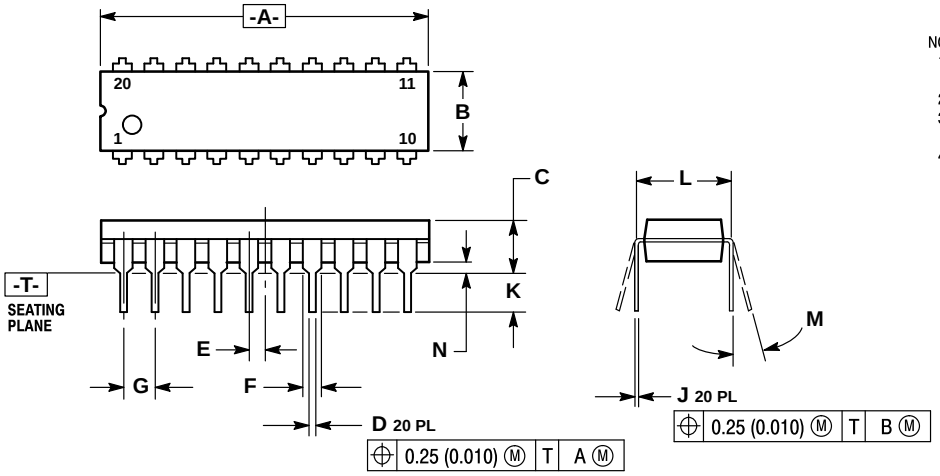


NOTES:
1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receive/transmit separation.
3. f_R = 7.5 kHz, ÷ R = 1480.
4. N_{total} = N • 32 + A = 27,501 to 28,166; N = 859 to 880; A = 0 to 31.
5. Only one implementation is shown. Various other configurations and dual–modulus prescaling values to ÷ 128/÷ 129 are possible.

Figure 14. 666 Channel, Computer Controlled, Mobile Radio Telephone Synthesizer for 800 MHz Cellular Radio Systems

PACKAGE DIMENSIONS

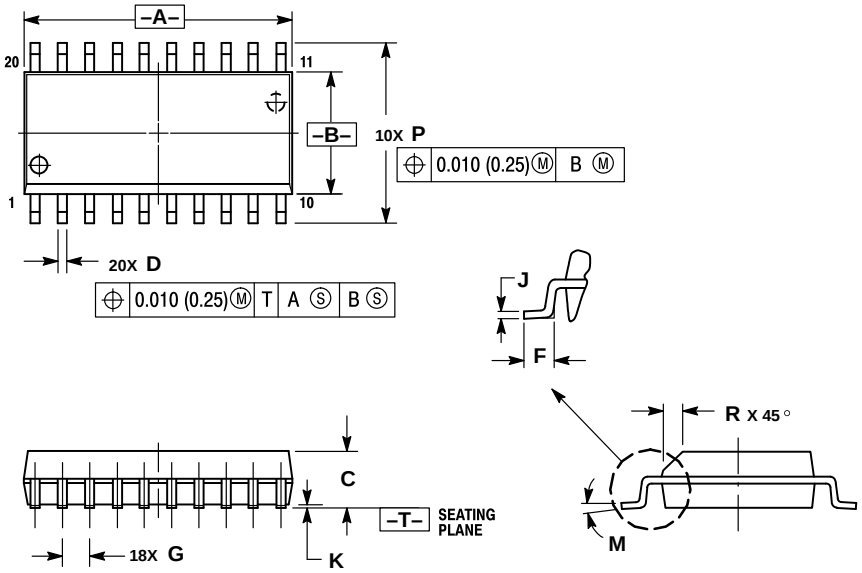
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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