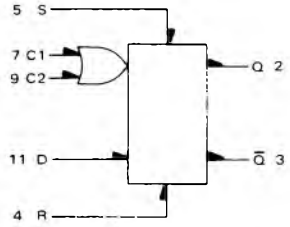

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	◇	◇	H
H	L	◇	◇	L
H	H	◇	◇	ND
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

◇ Don't Care
ND = Not Defined
C = C1 + C2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

Master-Slave
Type D Flip-Flop

The MC1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.