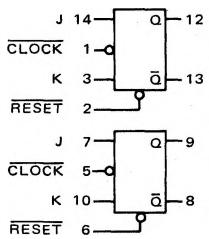
DUAL J-K FLIP-FLOP

MC3163F • MC3063F
MC3163L • MC3063L,P
(54H73) (74H73)



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

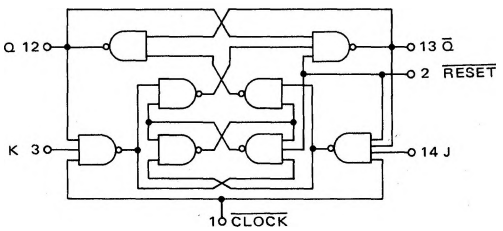
Input Loading Factor:
J, K = 1
RESET, CLOCK = 2

Output Loading Factor = 10

Total Power Dissipation = 176 mW typ/pkg
Propagation Delay Time = 10 ns typ
Operating Frequency = 30 MHz typ

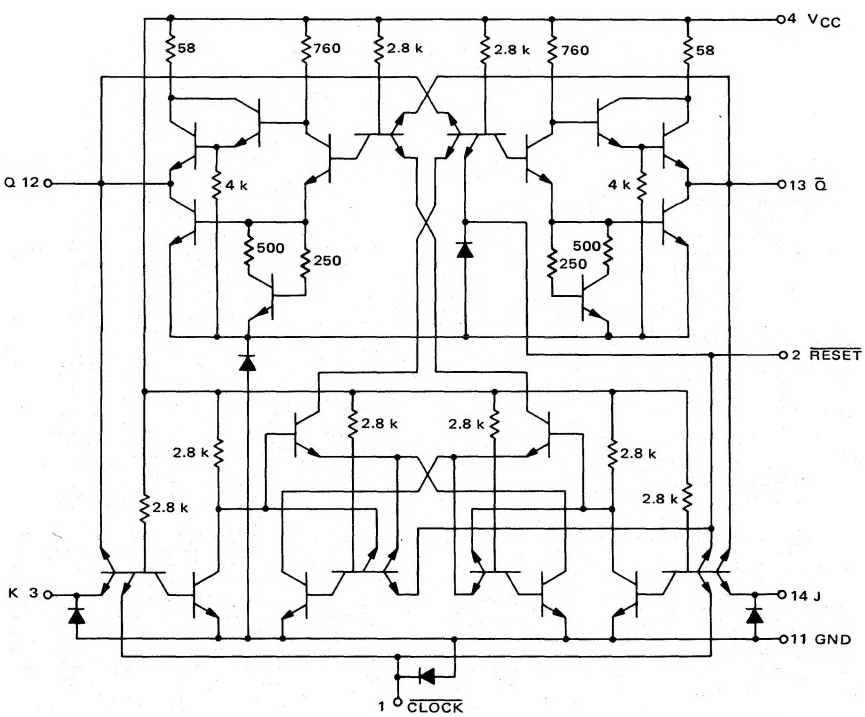
The MC3163/3063 dual J-K master-slave flip-flop is useful in simple register and counter designs, or where relatively slow rise times may be encountered. A similar function, the MC3155/3055 (MC54H72/74H72) AND input J-K flip-flop is available for applications requiring multiple ANDed inputs.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



Pin numbers for the 54H73F/74H73F device are the same as the pin numbers for the MC3163F,L/3063F,L,P.
These devices are available on special request.

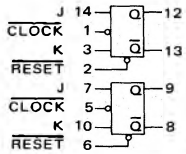
CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts										
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}		
MC3163	20	-0.5	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5		
MC3063	20	-0.5	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25		

Characteristic	Symbol	Pin Under Test	MC3163 Test Limits −55 to +125°C Min	MC3163 Max	MC3163 Unit	MC3063 Test Limits 0 to +75°C Min	MC3063 Max	MC3063 Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	**	Gnd
Input																					
Forward Current J	I_F	14	-	-2.0	mAdc	-	-2.0	mAdc	-	-	14	-	-	1,2,3	-	-	-	-	4	12	11*
K		3	-	-2.0	↓	-	-2.0	↓	-	-	3	-	-	1,2,14	-	-	-	-	↓	13	11*
$\overline{\text{Reset}}$		2	-	-4.0		-	-4.0		-	-	2	-	-	1,14	-	-	-	-		-	
$\overline{\text{Clock}}$		1	-	-2.0		-	-2.0		-	-	1	-	-	2,3,14	-	-	-	-		2	↓
Leakage Current J	I_{R1}	14	-	50	μAdc	-	50	μAdc	-	-	-	14	-	-	-	-	-	-	4	-	1,2,11*
K		3	-	50	↓	-	50	↓	-	-	-	3	-	2	-	-	-	-	↓	2	1,11*
$\overline{\text{Reset}}$		2	-	100		-	100		-	-	-	2	-	-	-	-	-	-		-	1,3,11,13,14*
$\overline{\text{Clock}}$		1†	-	50		-	50		-	-	-	1	-	-	-	-	-	-		-	2,3,11,14*
J	I_{R2}	14	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	14	-	-	-	-	-	4	-	1,2,11*
K		3	-	↓	↓	-	↓	↓	-	-	-	-	3	2	-	-	-	-	↓	2	1,11*
$\overline{\text{Reset}}$		2	-			-			-	-	-	-	2	-	-	-	-	-		-	1,3,11*,13,14
$\overline{\text{Clock}}$		1	-			-			-	-	-	-	1	-	-	-	-	-		-	2,3,11,14*
Output																					
Output Voltage	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	-	2	-	4	-	-	1,3,11,14*
		13	-	0.4	Vdc	-	0.4	Vdc	13	-	-	-	-	1,3,14	2	-	-	4	-	13	11*
	V_{OH}	12	2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	1,3	2	-	-	4	-	13	11,14*
		13	2.4	-	Vdc	2.4	-	Vdc	-	13	-	-	-	-	-	2	-	4	-	-	1,3,11,14*
Short-Circuit Current	I_{SC}	12‡	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,3,14	-	-	-	-	4	-	11,12,13*
		13	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,3,14	-	-	-	-	4	-	2,11,13*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	4	-	50	mAdc	-	50	mAdc	-	-	-	-	-	1, 2, 5# 6, 7, 14	-	-	-	-	4	-	3, 10, 11

*Ground inputs to flip-flop not under test.

**Momentarily ground pin prior to taking measurement to set flip-flop in the desired state. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

‡Test duration ≤ 100 ms.

†Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

#Apply momemtarily 4.5 V, then ground to clock.

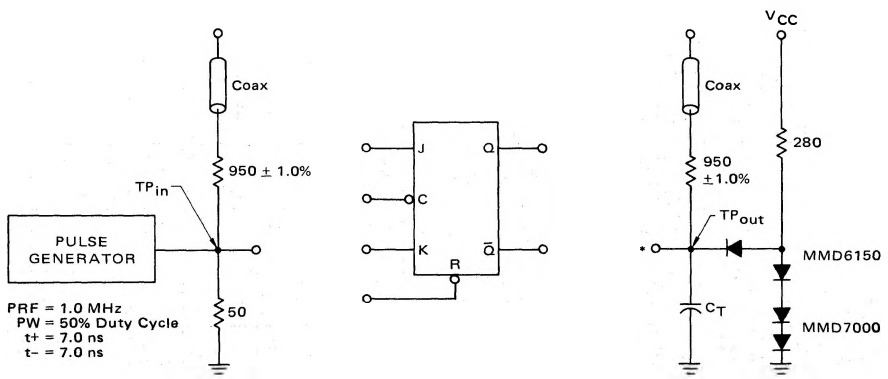
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\bar{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation, Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



Two pulse generators are required and must be slaved together for t_{sd} tests.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

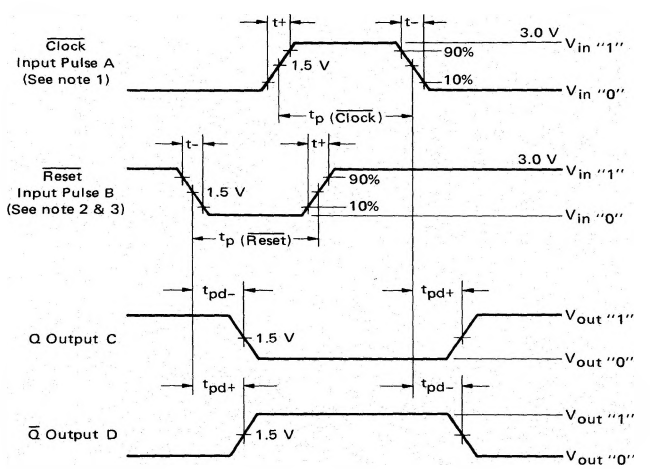
The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

TEST PROCEDURES

TEST	SYMBOL	INPUT			Q	$\bar{Q}$	LIMITS		
		$\bar{C}$	J,K	$\bar{R}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	2.4 V	5.0 V	†	†	25	–	MHz
Turn-On Delay– Clock to Output	t_{pd+}	A	2.4 V	2.4 V	C	D	–	21	ns
Turn-Off Delay– Clock to Output	t_{pd-}	A	2.4 V	2.4 V	C	D	–	27	ns
*Turn-On Delay– Reset to Output	t_{pd+}	A	2.4 V	B	C	D	–	13	ns
*Turn-Off Delay– Reset to Output	t_{pd-}	A	2.4 V	B	C	D	–	24	ns

Letters shown in test columns refer to waveforms shown.
*Clock pulse negative edge must occur when reset pulse is in "1" state.
†Output shall toggle with each input pulse.

VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES

1. When testing f_{Tog}, $\overline{Clock}$ characteristics are t+ = t- ≤3.0 ns, $t_{p\ (\overline{Clock})}$ = 12 ns, PRF = 25 MHz.
   When testing t_{pd+}, t_{pd-}, $\overline{Clock}$ characteristics are t+ = t- ≤7.0 ns, $t_{p\ (\overline{Clock})}$ = 20 ns, PRF = 1.0 MHz.
2. $\overline{Reset}$ input dominates regardless of state of clock or J-K inputs.
3. $\overline{Reset}$ pulse characteristics t+ = t- ≤7.0 ns, $t_{p\ (\overline{Reset})}$ = 16 ns, PRF = 1.0 MHz