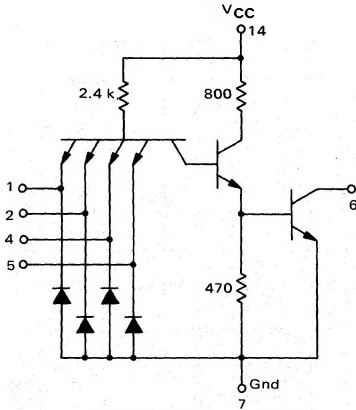


DUAL 4-INPUT "NAND" GATE
(Open Collector)

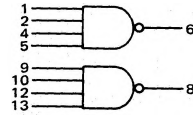
MC3100/MC3000 series

MC3112F • MC3012F
MC3112L • MC3012L,P
(54H22J) (74H22J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.



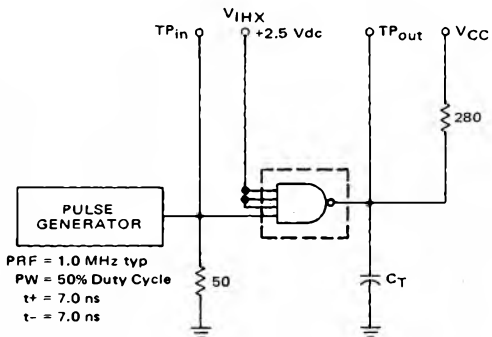
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H22F/74H22F device are shown in the chart. These devices are available on special request.

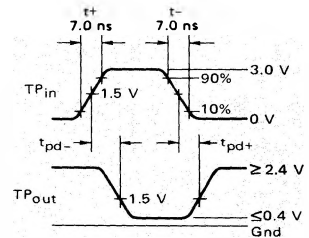
DEVICE	PIN NUMBERS													
MC3112F,L/3012F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H22F/74H22F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PRF = 1.0 MHz typ
PW = 50% Duty Cycle
 $t^+ = 7.0$ ns
 $t^- = 7.0$ ns

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

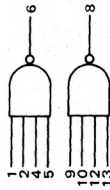


See General Information section for packaging.

MC3112, MC3012 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3112 Test Limits						MC3012 Test Limits						TEST CURRENT / VOLTAGE VALUES																						
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		mA		Volts																				
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	V _{OH}	V _{OL}	V _{IH}	V _{IL}	V _{FH}	V _{FL}	V _R	V _{FB}	V _{CEX}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHX}							
Input																																					
Forward Current	I _F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
Leakage Current	I _L	1	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
Breakdown Voltage	BV _{in}	1	-	-	-	5.5	-	-	-	5.5	-	-	-	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	-	-	-	-	-	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
Output																																					
Output Voltage	V _{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Output Leakage Current	I _{CEX}	-	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Power Requirements (Total Device)																																					
Maximum Power Supply Current	I _{max}	14	-	-	-	12.5	-	-	-	12.5	-	-	-	12.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Power Supply Drain	I _{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	-	20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{PDL}	14	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Switching Parameters																																					
Turn-On Delay	t _{pd+}	1,6	-	-	-	14	-	-	-	14	-	-	-	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Turn-Off Delay	t _{pd-}	1,6	-	-	-	20	-	-	-	20	-	-	-	20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.