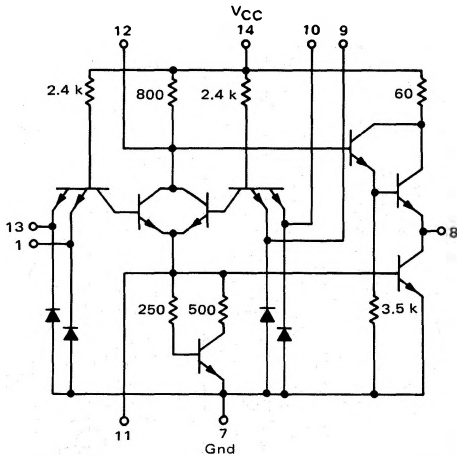


EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC3100/MC3000 series

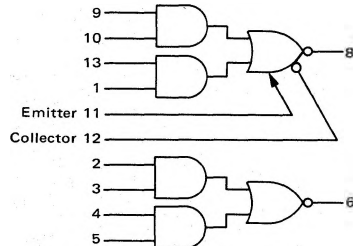
MC3120F • MC3020F
MC3120L • MC3020L,P
(54H50J) (74H50J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN†



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORING nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030/3130 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$8 = (9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})$$

Negative Logic:

$$8 = (9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})$$

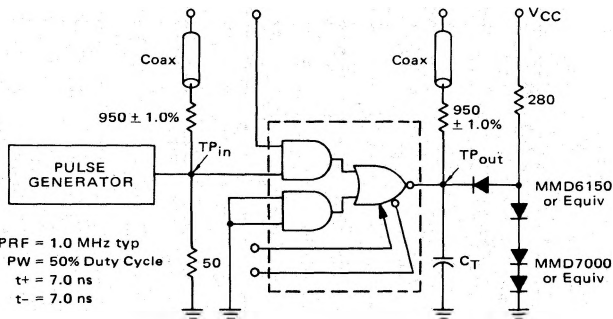
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 62.5 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Expander pins should be left open when measuring switching times.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

