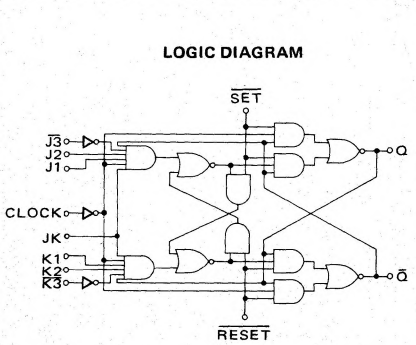
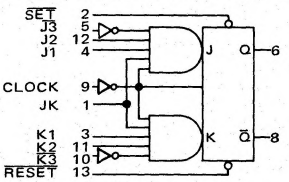
MC3152F • MC3052F
MC3152L • MC3052L,P

This is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a $\overline{J}$-input ANDed together and two K-inputs and a $\overline{K}$-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J, K and K) or an additional logic input (JK) for use in counters or certain other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to enable presetting data into the flip-flop such as initial conditions. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

LOGIC DIAGRAM





$J = J1 \cdot J2 \cdot \overline{J3} \cdot JK$

$K = K1 \cdot K2 \cdot \overline{K3} \cdot JK$

TRUTH TABLE

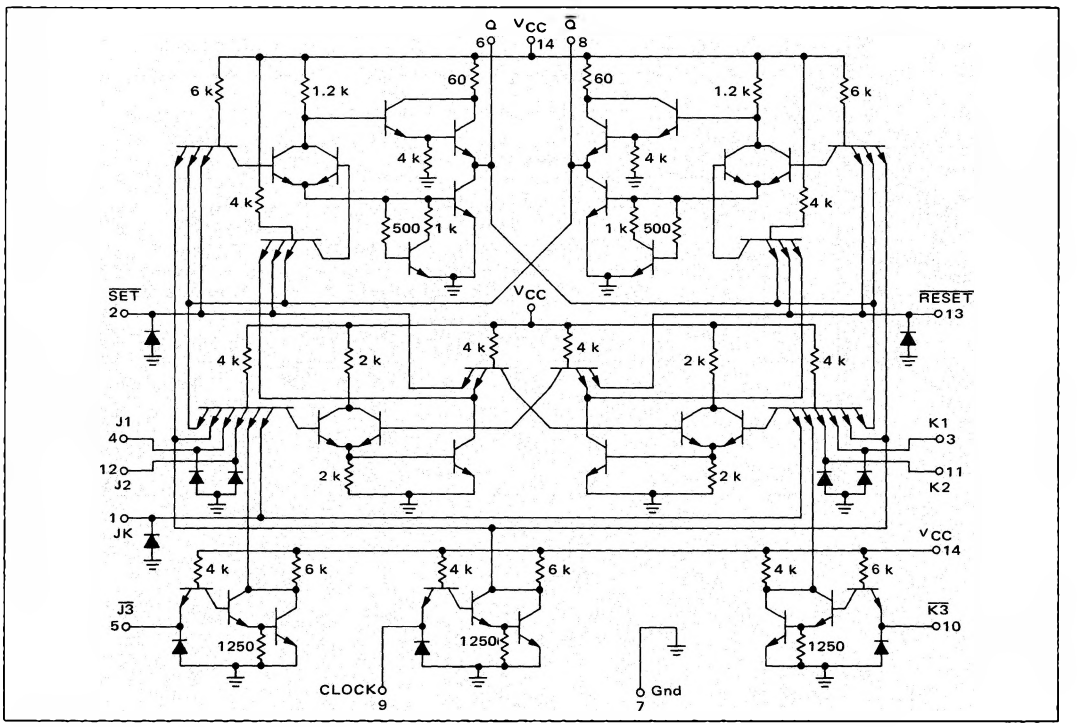
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
JK = 1.5
J, K, CLOCK = 0.75
$\overline{SET}$, $\overline{RESET}$ = 2.25

Output Loading Factor = 10

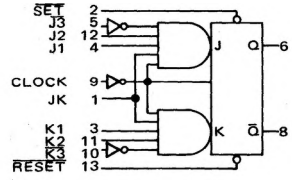
Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 75 mW/pkg
Toggle Frequency = 40 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Hold Time = 8.0 ns
t_{pd-} = 20 ns
t_{pd+} = 12 ns



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES: mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
MC3152 −55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3152 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5
MC3152 +125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5
MC3052 0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.75
MC3052 +25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.75
MC3052 +75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.75

Characteristic	Symbol	Pin Under Test	MC3152 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3052 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	$-V_{IH}$	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_T*	Gnd
Input																														
Forward Current	I_{FJ}	4	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	4	-	1,12	-	-	-	14	-	5,7,9,13
		12	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	12	-	1,4	-	-	-	14	-	5,7,9,13
	I_{FK}	3	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	3	-	1,11	-	-	-	14	-	2,7,9,10
		11	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	11	-	1,3	-	-	-	14	-	2,7,9,10
	$I_{F\overline{J}}$	5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	5	-	-	-	-	-	14	-	7
	$I_{F\overline{K}}$	10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	10	-	-	-	-	-	14	-	7
	I_{FC}	9	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	-	2,5,7,9,10,13
	$I_{F\overline{S}}$	2	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	2	-	-	-	-	-	14	-	7,9,13
	$I_{F\overline{R}}$	13	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	13	-	-	-	-	-	14	-	2,7,9
Leakage Current	I_{RJ}	4	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	4	5,9	-	-	-	14	-	1,2,7,12
		12	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	12	5,9	-	-	-	14	-	1,2,4,7
	I_{RK}	3	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	3	9,10	-	-	-	14	-	1,7,11,13
		11	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	11	9,10	-	-	-	14	-	1,3,7,13
	$I_{R\overline{J}}$	5	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	5	-	-	-	-	14	-	7
	$I_{R\overline{K}}$	10	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	10	-	-	-	-	14	-	7
	I_{RC}	9	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	9	-	-	-	-	14	-	7
	I_{RJK}	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	5,9,10	-	-	-	14	-	3,4,6,7,8,11,12
	$I_{R\overline{S}}$	2	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	-	2	1,4,10,12,13	-	-	-	14	9	3,5,7,11
	$I_{R\overline{R}}$	13	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	-	13	1,2,3,5,11	-	-	-	14	9	4,7,10,12
Breakdown Voltage	BV_{in}	4	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	4	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
		12	-	-		-	-	-	-	-		-	-	-		-	-	12	-	-	-	-	-	5,9	-	-	-		-	1,2,4,7
		3	-	-		-	-	-	-	-		-	-	-		-	-	3	-	-	-	-	-	9,10	-	-	-		-	1,7,11,13
		11	-	-		-	-	-	-	-		-	-	-		-	-	11	-	-	-	-	-	9,10	-	-	-		-	1,3,7,13
		1	-	-		-	-	-	-	-		-	-	-		-	-	1	-	-	-	-	-	2,5,9,10,13	-	-	-		-	3,4,6,7,8,11,12
		2	-	-		-	-	-	-	-		-	-	-		-	-	2	-	-	-	-	-	1,4,10,12,13	-	-	-		9	3,5,7,11
		13	-	-		-	-	-	-	-		-	-	-		-	-	13	-	-	-	-	-	1,2,3,5,11	-	-	-		9	4,7,10,12
		5	-	-		-	-	-	-	-		-	-	-		-	-	5	-	-	-	-	-	-	-	-	-		-	7
		9	-	-		-	-	-	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-	-		-	7
		10	-	-	▼	-	-	-	-	-	▼	-	-	-	▼	-	-	10	-	-	-	-	-	-	-	-	-	▼	-	7
Clamp Voltage	V_D	4	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	4	-	-	-	-	-	-	-	-	14	-	-	7
		12	-	-	-		-	-	-	-	-		-	-		-	-	-	12	-	-	-	-	-	-	-	-		-	-	
		3	-	-	-		-	-	-	-	-		-	-		-	-	-	3	-	-	-	-	-	-	-	-		-	-	
		11	-	-	-		-	-	-	-	-		-	-		-	-	-	11	-	-	-	-	-	-	-	-		-	-	
		5	-	-	-		-	-	-	-	-		-	-		-	-	-	5	-	-	-	-	-	-	-	-		-	-	
		10	-	-	-		-	-	-	-	-		-	-		-	-	-	10	-	-	-	-	-	-	-	-		-	-	
		9	-	-	-		-	-	-	-	-		-	-		-	-	-	9	-	-	-	-	-	-	-	-		-	-	
		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-	-	-	-		-	-	
		2	-	-	-		-	-	-	-	-		-	-		-	-	-	2	-	-	-	-	-	-	-	-		-	-	
		13	-	-	-	▼	-	-	-	-	-	▼	-	-	▼	-	-	-	13	-	-	-	-	-	-	-	-	▼	-	-	▼
Output																														
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	13	2	-	-	-	-	-	-	14	-	-	7,9
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	2	13	-	-	-	-	-	-	14	-	-	7,9
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	2	13	-	-	-	-	-	-	14	-	-	7,9
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	13	2	-	-	-	-	-	-	14	-	-	7,9
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2,6,7
		8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	7,8,13
Power Requirements (Total Device)																														
Maximum Power Current	I_{max}	14	-	-	-	42	-	-	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13

OPERATING CHARACTERISTICS

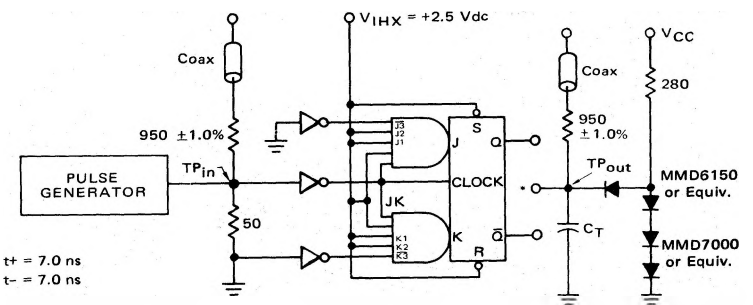
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the $\overline{SET}$ input sets Q high and low level on the $\overline{RESET}$ input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering – When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused $\overline{J}$ and $\overline{K}$ inputs must be tied to ground. The unused $\overline{SET}$ and $\overline{RESET}$ inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

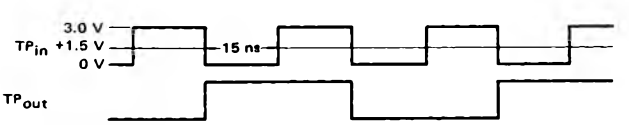
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

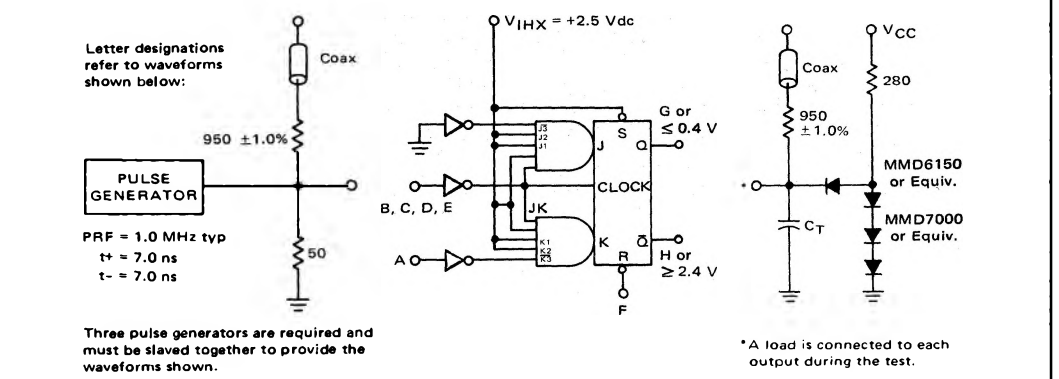
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

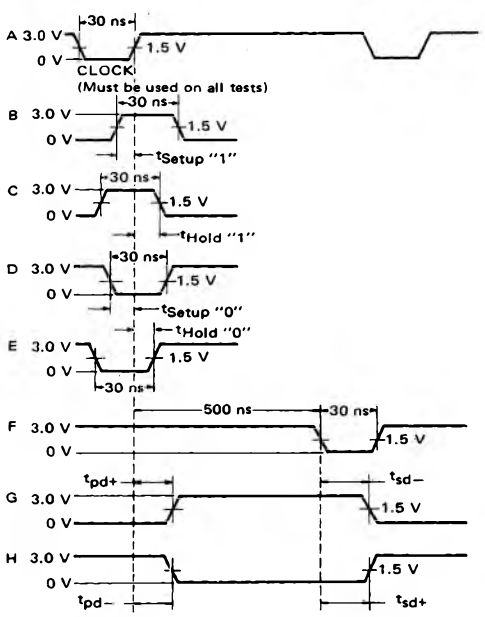
(For J inputs and $\overline{\text{RESET}}$ input; to test other inputs, refer to Test Procedures Chart)



The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J*	INPUT J̄*	INPUT SET*	INPUT RESET*	INPUT K*	INPUT K̄*	Q*	Q̄*	LIMITS (ns) Min	LIMITS (ns) Max
$t_{Setup\ "1"}$ J	C	Gnd	2.4 V	F	Gnd	Gnd	G	H	–	15
$t_{Hold\ "0"}$ J	B	Gnd	2.4 V	F	Gnd	Gnd	≤0.4 V	≥2.4 V	–	–3.0
$t_{Setup\ "1"}$ K	Gnd	Gnd	F	2.4 V	C	Gnd	H	G	–	15
$t_{Hold\ "0"}$ K	Gnd	Gnd	F	2.4 V	B	Gnd	≥2.4 V	≤0.4 V	–	–3.0
$t_{Setup\ "1"}$ J̄	2.4V	E	2.4 V	F	2.4 V	Gnd	G	H	–	15
$t_{Hold\ "0"}$ J̄	2.4 V	D	2.4 V	F	2.4 V	Gnd	≤0.4 V	≥2.4 V	–	–3.0
$t_{Setup\ "1"}$ R̄	2.4 V	Gnd	F	2.4 V	2.4 V	E	H	G	–	15
$t_{Hold\ "0"}$ R̄	2.4V	Gnd	F	2.4 V	2.4 V	D	≥2.4 V	≤0.4 V	–	–3.0
t_{pd+}	Delay from clock to Q during $t_{Setup\ "1"}$ J test. Delay from clock to Q̄ during $t_{Setup\ "1"}$ K test.								8	20
t_{pd-}	Delay from clock to Q̄ during $t_{Setup\ "1"}$ J test. Delay from clock to Q during $t_{Setup\ "1"}$ K test.								14	28
t_{sd+}	Delay from SET to Q during $t_{Setup\ "1"}$ K test. Delay from RESET to Q̄ during $t_{Setup\ "1"}$ J test.								–	18
t_{sd-}	Delay from SET to Q̄ during $t_{Setup\ "1"}$ K test. Delay from RESET to Q during $t_{Setup\ "1"}$ J test.								–	25

*Letters shown in these columns refer to waveforms.