Technical Data

TANGO3
MC33493/D
Rev. 1.6, 6/2002

PLL tuned UHF Transmitter for Data Transfer Applications

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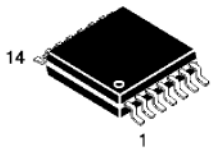
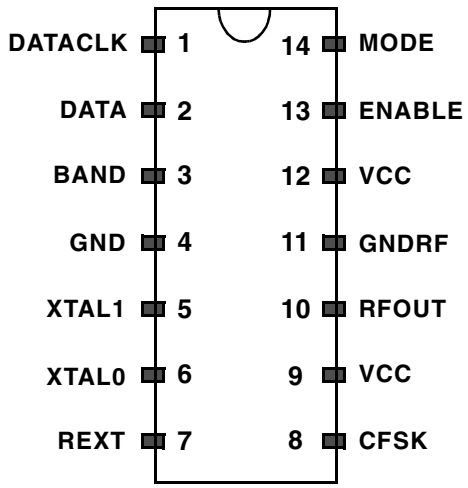


TSSOP–14
DTB SUFFIX
CASE 948G

FEATURES

- Selectable frequency bands: 315-434MHz and 868-928MHz
- OOK and FSK modulation
- Adjustable output power range
- Fully integrated VCO
- Supply voltage range: 1.9-3.6V
- Very low standby current: 0.1nA @ T_A=25°C
- Low supply voltage shutdown
- Data clock output for microcontroller
- Extended temperature range: -40°C to 125°C
- Low external component count
- Typical application compliant with ETSI standard

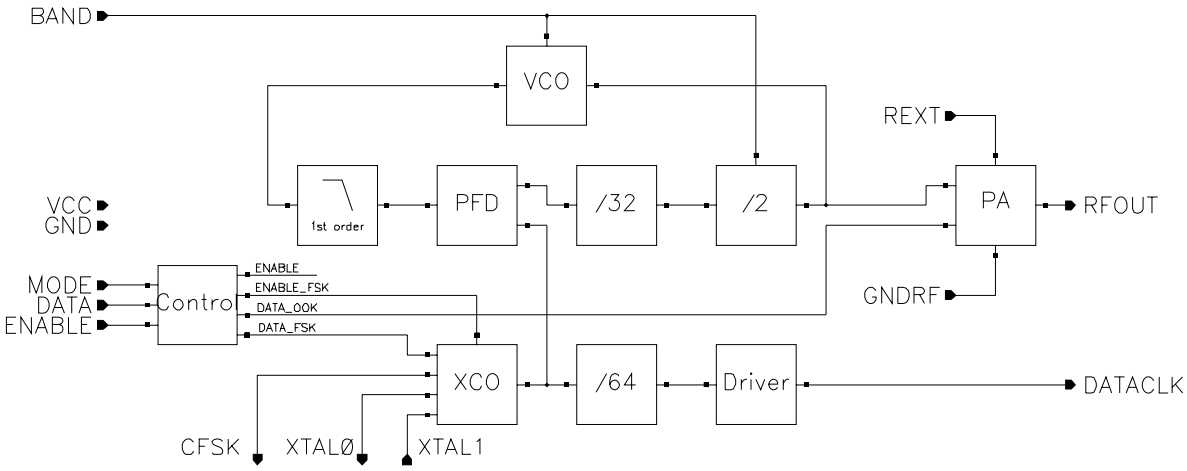
PIN CONNECTIONS



Ordering Information

Device	Ambiant Temperature Range	Package
MC33493 DTB	-40°C to 125°C	TSSOP14

Figure 1: Simplified block diagram



PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DATACLK	Clock output to the microcontroller
2	DATA	Data input
3	BAND	Frequency band selection
4	GND	Ground
5	XTAL1	Reference oscillator input
6	XTAL0	Reference oscillator output
7	REXT	Power amplifier output current setting input
8	CFSK	FSK switch output
9	VCC	Power supply
10	RFOUT	Power amplifier output
11	GNDRF	Power amplifier ground
12	VCC	Power supply
13	ENABLE	Enable input
14	MODE	Modulation type selection input

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	V_{GND} - 0.3 to 3.7	V
Voltage Allowed on Each Pin		V_{GND} - 0.3 to V_{CC} + 0.3	V
ESD HBM Voltage Capability on Each Pin (note 1)		±2000	V
ESD MM Voltage Capability on Each Pin (note 2)		±150	V
Storage Temperature	Ts	-65 to +150	°C
Junction Temperature	Tj	+150	°C

Notes:
1 Human Body model, AEC-Q100-002 Rev. C.
2 Machine Model, AEC-Q100-003 Rev. E.

TRANSMITTER FUNCTIONAL DESCRIPTION

MC33493 is a PLL tuned low power UHF transmitter. The different modes of operation are controlled by the microcontroller through several digital input pins. The power supply voltage ranges from 1.9V to 3.6V allowing operation with a single lithium cell.

PHASE LOCKED LOOP AND LOCAL OSCILLATOR

The VCO is a completely integrated relaxation oscillator. The Phase Frequency Detector (PFD) and the loop filter are fully integrated. The exact output frequency is equal to: $f_{RFOUT} = f_{XTAL}$ x [PLL Divider Ratio]. The frequency band of operation is selected through the BAND pin.

Table 1 provides details for each frequency band selection.

Table 1: Band selection and associated divider ratios

BAND Input Level	Frequency Band (MHz)	PLL Divider Ratio	Crystal Oscillator Frequency (MHz)
High	315	32	9.84
	434		13.56
Low	868	64	

An out-of-lock function is performed by monitoring the PFD output voltage. When it exceeds defined limits, the RF output stage is disabled.

RF OUTPUT STAGE

The output stage is a single ended square wave switched current source. Harmonics are present in the output current drive. Their radiated absolute level depends on the antenna characteristics and output power. Typical application demonstrates compliance to ETSI standard.

A resistor R_{ext} connected to the REXT pin controls the output power allowing a trade-off between radiated power and current consumption.

The output voltage is internally clamped to $V_{cc} \pm 2V_{be}$ (typ. $V_{cc} \pm 1.5V$ @ $T_A=25°C$).

MODULATION

A low logic level has to be applied on pin MODE to select the On Off Keying (OOK) modulation. This modulation is performed by switching on/off the RF output stage. The logic level applied on pin DATA controls the output stage state:

DATA=0 $\rightarrow$ output stage off,

DATA=1 $\rightarrow$ output stage on.

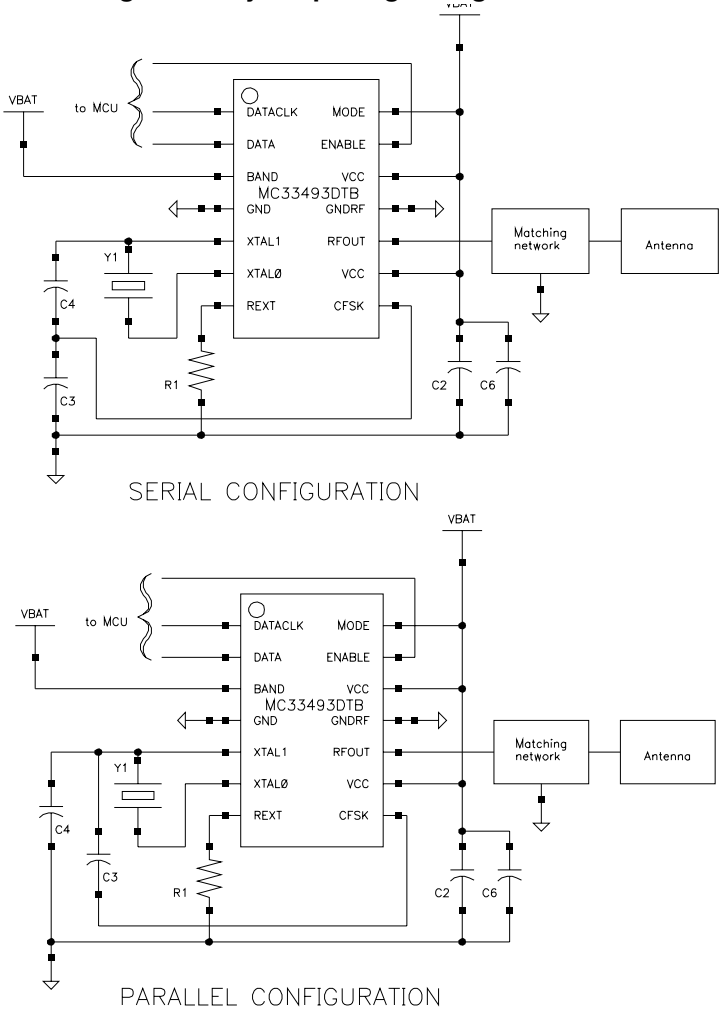
If a high logic level is applied on pin MODE, then Frequency Shift Keying (FSK) modulation is selected. This modulation is achieved by crystal pulling. An internal switch connected to CFSK pin enables to switch the external crystal load capacitors. Figure 2 shows the possible configurations: serial and parallel.
The logic level applied on pin DATA controls the state of this internal switch:

DATA=0 $\rightarrow$ switch off,

DATA=1 $\rightarrow$ switch on.

DATA input is internally re-synchronized by the crystal reference signal. The corresponding jitter on the data duty cycle cannot exceed ± 1 reference period (± 75ns for a 13.56MHz crystal).
This crystal pulling solution implies that the RF output frequency deviation equals the crystal frequency deviation multiplied by the PLL Divider Ratio (see table 1).

Figure 2: Crystal pulling configurations



MICROCONTROLLER INTERFACE

Four digital input pins (ENABLE, DATA, BAND and MODE) enable the circuit to be controlled by a microcontroller. It is recommended to configure the band frequency and the modulation type before enabling the circuit.

One digital output (DATACLK) provides to the microcontroller a reference frequency for data clocking. This frequency is equal to the crystal oscillator frequency divided by 64 (see table 2).

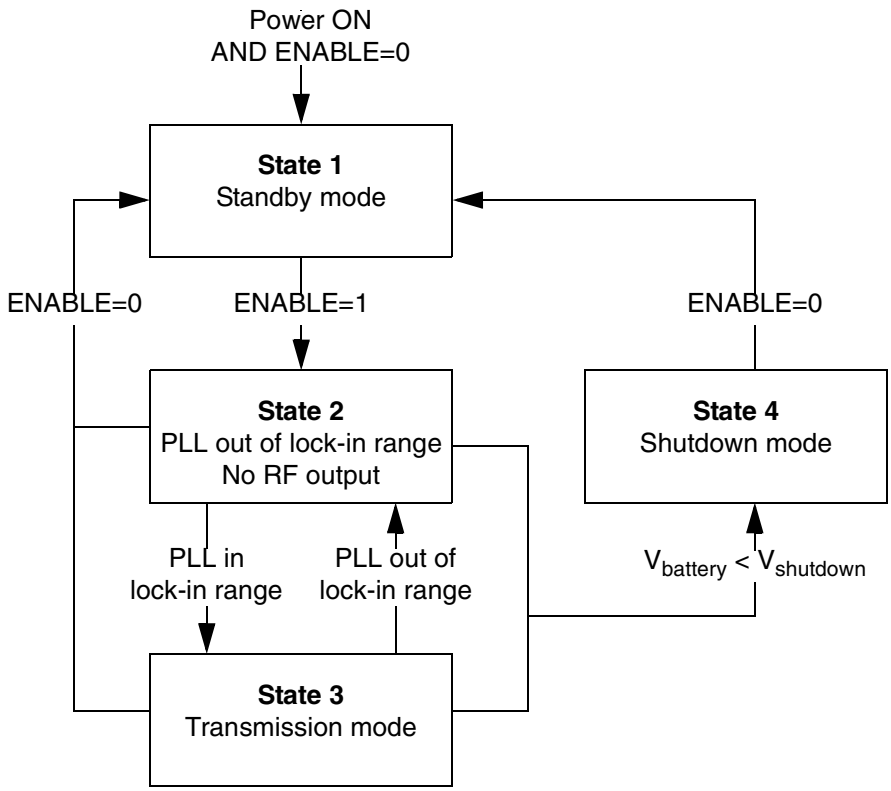
Table 2: DATACLK frequency vs crystal oscillator frequency

Crystal Oscillator Frequency (MHz)	DATACLK Frequency (kHz)
9.84	154
13.56	212

STATE MACHINE

Figure 3 details the state machine.

Figure 3: State machine



State 1:
The circuit is in standby mode and draws only a leakage current from the power supply.

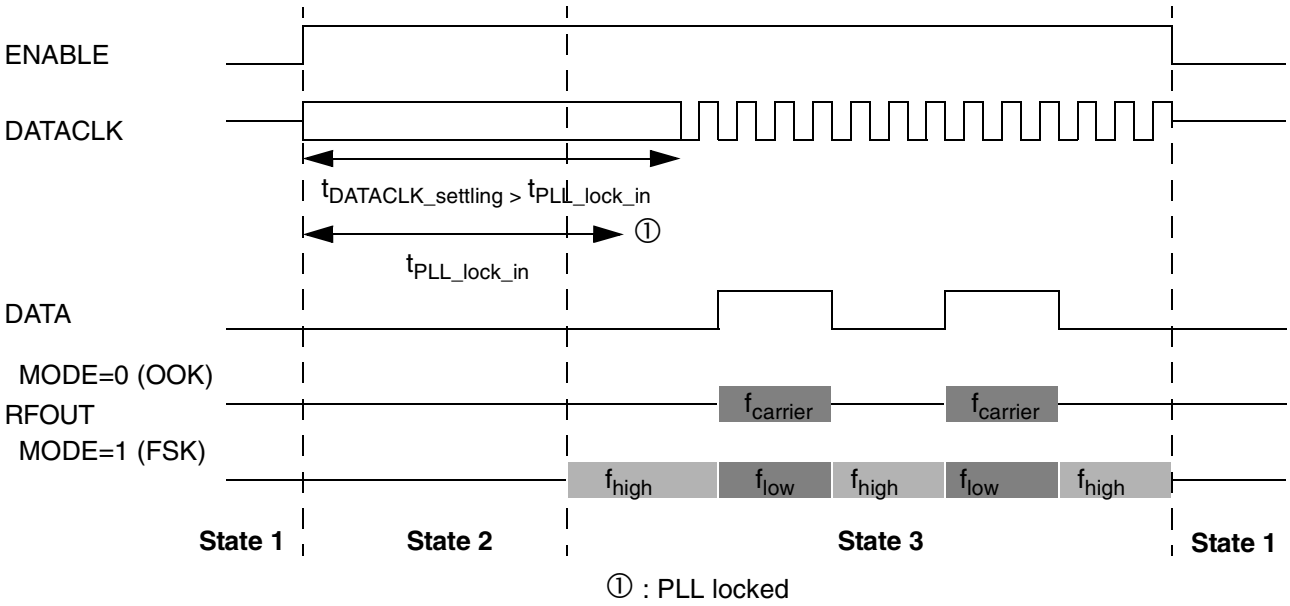
State 2:
In this state, the PLL is out of the lock-in range. Therefore the RF output stage is switched off preventing RF transmission. Data clock is available on pin DATACLK. Each time the device is enabled, the state machine passes through this state.

State 3:
In this state, the PLL is within the lock-in range. If $t<t_{PLL\_lock\_in}$ then the PLL can still be in acquisition mode. If $t \geq t_{PLL\_lock\_in}$, then the PLL is locked.
Data entered on pin DATA are output on pin RFOUT according to the modulation selected by the level applied on pin MODE.

State 4:
When the supply voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off. Applying a low level on pin ENABLE is the only condition to get out of this state.

Figure 4 shows the waveforms of the main signals for a typical application cycle.

Figure 4: Signals waveforms and timings definition



POWER MANAGEMENT

When the battery voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off. It has to be noted that after this shutdown, the circuit is latched until a low level is applied on pin ENABLE (see state 4 of the state machine).

DATA CLOCK

At start-up data clock timing is valid after the data clock settling time. As clock is switched off asynchronously, the last period duration cannot be guaranteed.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, voltage range V_{cc}=[$V_{shutdown}$;3.6V], temperature range T_A=[-40°C;+125°C], R_{ext}=12kΩ+/-5%, RF output frequency $f_{carrier}$=433.92MHz, reference frequency $f_{reference}$=13.560MHz, output load R_L=50Ω+/-1% (figure 9). Values refer to the circuit shown in the recommended application schematics: figure 12 (14) for OOK (FSK) modulation. Typical values reflect average measurement at V_{CC}=3V, T_A=25°C.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
1	**General Parameters**					
1.1	Supply Current in Standby Mode	T_A≤25°C	-	0.1	5	nA
1.2		T_A=60°C	-	7	30	nA
1.3		T_A=85°C	-	40	100	nA
1.4		T_A=125°C	-	800	1700	nA
1.7	Supply Current in Transmission Mode	315 & 434 bands, OOK and FSK modulation, continuous wave, T_A=25°C	-	11.6	13.5	mA
1.5		315 & 434 bands, DATA=0, -40°C≤T_A≤125°C	-	4.4	6.0	mA
1.6		868MHz band, DATA=0, -40°C≤T_A≤125°C	-	4.6	6.2	mA
1.8		315 & 434 bands, OOK and FSK modulation, continuous wave, -40°C≤T_A≤125°C	-	11.6	14.9	mA
1.9		868MHz band, OOK and FSK modulation, continuous wave, -40°C≤T_A≤125°C	-	11.8	15.1	mA
1.10	Supply Voltage		-	3	3.6	V
1.11	Shutdown Voltage Threshold	T_A=-40°C	-	2.04	2.11	V
1.12		T_A=-20°C	-	1.99	2.06	V
1.13		T_A=25°C	-	1.86	1.95	V
1.14		T_A=60°C	-	1.76	1.84	V
1.15		T_A=85°C	-	1.68	1.78	V
1.16		T_A=125°C	-	1.56	1.67	V

ELECTRICAL CHARACTERISTICS

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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2	**RF Parameters**					
2.1	R_{ext} value		12	-	21	kΩ
2.2	Output Power	315 & 434MHz bands, with 50Ω matching network	-	5	-	dBm
2.3		868MHz band, with 50Ω matching network	-	1	-	dBm
2.4		315 & 434MHz bands, -40°C≤T_A≤125°C	-3	0	3	dBm
2.8		868MHz band, -40°C≤T_A≤125°C	-7	-3	0	dBm
2.12	Current & Output Power Variation vs. R_{ext} value	315 & 434MHz bands, with 50Ω matching network	-	-0.35 -0.25	-	dB/kΩ mA/ kΩ
2.13	Harmonic 2 Level	315 & 434MHz bands, with 50Ω matching network	-	-34	-	dBc
2.14		868MHz band, with 50Ω matching network	-	-49	-	dBc
2.15		315 & 434MHz bands	-	-23	-17	dBc
2.16		868MHz band	-	-38	-27	dBc
2.17	Harmonic 3 Level	315 & 434MHz bands, with 50Ω matching network	-	-32	-	dBc
2.18		868MHz band, with 50Ω matching network	-	-57	-	dBc
2.19		315 & 434MHz bands	-	-21	-15	dBc
2.20		868MHz band	-	-48	-39	dBc
2.21	Spurious Level @ $f_{carrier} \pm f_{DATACLK}$	315 & 434MHz bands	-	-36	-24	dBc
2.22		868MHz band	-	-29	-17	dBc
2.23	Spurious Level @ $f_{carrier} \pm f_{reference}$	315 MHz band	-	-37	-30	dBc
2.24		434MHz band	-	-44	-34	dBc
2.25		868MHz band	-	-37	-27	dBc
2.41	Spurious Level @ $f_{carrier}/2$	315MHz band	-	-62	-53	dBc
2.26		434MHz band	-	-80	-60	dBc
2.27		868MHz band	-	-45	-39	dBc

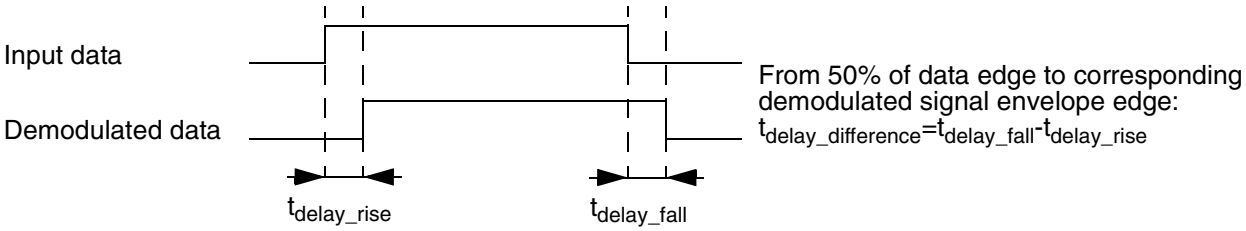
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, voltage range V_{cc}=[$V_{shutdown}$;3.6V], temperature range T_A=[-40°C;+125°C], R_{ext}=12kΩ+/-5%, RF output frequency $f_{carrier}$=433.92MHz, reference frequency $f_{reference}$=13.560MHz, output load R_L=50Ω+/-1% (figure 9). Values refer to the circuit shown in the recommended application schematics: figure 12 (14) for OOK (FSK) modulation. Typical values reflect average measurement at V_{CC}=3V, T_A=25°C.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2.30	Phase Noise	315 & 434MHz bands, ±175kHz from $f_{carrier}$	-	-75	-68	dBc/Hz
2.31		868MHz band, ±175kHz from $f_{carrier}$	-	-73	-66	dBc/Hz
2.32	PLL Lock-in Time, $t_{PLL\_lock\_in}$	$f_{carrier}$ within 30kHz from the final value, crystal series resistor=150Ω	-	400	1600	µs
2.33	XTAL1 Input Capacitance		-	1	-	pF
2.34	Crystal Resistance	OOK modulation	-	20	200	Ω
2.44		FSK modulation		20	50	
2.35	OOK Modulation Depth		75	90	-	dBc
2.36	FSK Modulation Carrier Frequency Total Deviation	315 & 434MHz bands, see note 1	-	-	100	kHz
2.37		868MHz band, see note 1	-	-	200	kHz
2.38	CFSK Output Resistance	MODE=0, DATA=x MODE=1, DATA=0	50	70	-	kΩ
2.39		MODE=1, DATA=1	-	90	300	Ω
2.43	CFSK Output Capacitance		-	1	-	pF
2.40	Data Rate	Manchester coding	-	-	10	kBit/s
2.41	Data to RF delay difference between falling and rising edges, $t_{delay\_difference}$	MODE=0, see note 2	3.5	5.25	7.5	µs
2.42		MODE=1, see note 2	-200	-	200	ns

Note 1: This parameter is depending on crystal characteristics, load capacitor values (see Table 6) and PCB track capacitance.

Note 2: Delay difference definition



ELECTRICAL CHARACTERISTICS

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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
3	**Microcontroller Interfaces**					
3.1	Input Low Voltage	Pins BAND, MODE, ENABLE, DATA	0	-	0.3 x V_{CC}	V
3.2	Input High Voltage		0.7 x V_{CC}	-	V_{CC}	V
3.3	Input Hysteresis Voltage		-	-	120	mV
3.4	Input Current	Pins BAND, MODE, DATA = 1	-	-	100	nA
3.5	ENABLE Pull Down Resistor		-	180	-	kΩ
3.6	DATACLK Output Low Voltage	C_{load} = 2pF	0	-	0.25 x V_{CC}	V
3.7	DATACLK Output High Voltage		0.75 x V_{CC}	-	V_{CC}	V
3.8	DATACLK Rising Time	C_{load} = 2pF, measured from 20% to 80% of the voltage swing	-	250	500	ns
3.9	DATACLK Falling Time		-	150	400	ns
3.10	DATACLK Settling Time, $t_{DATACLK\_settling}$	45% < Duty Cycle $f_{DATACLK}$ < 55%	-	800	2000	µs

RF OUTPUT SPECTRUM

Following are spectrums of transmitter carrier, measured in conduction mode. Three different spans have been used. The 5MHz span spectrum (figure) shows phase noise response close to the RF carrier, and the noise suppression within the PLL loop bandwidth. The 50MHz span spectrum (figure 6) shows both phase noise and reference spurious. Finally figure 7 shows second and third harmonics of carrier. All these spectrums are measured in OOK modulation, at DATA=1.

Figure 8 shows spectrum in case of FSK modulation, with 45kHz deviation, at 4kbit/s data rate.

Figure 5: RF spectrum at 434MHz frequency band displayed with a 5MHz span

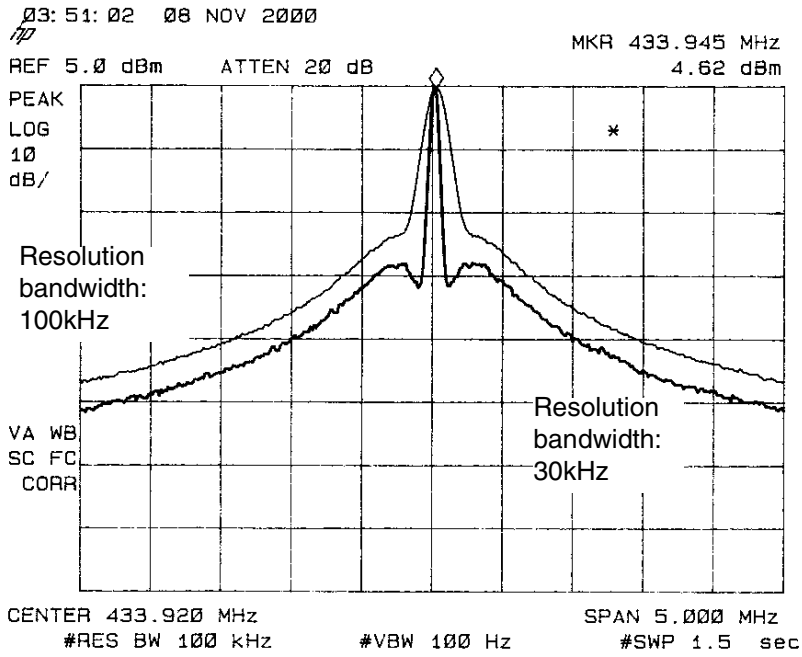


Figure 6: RF spectrum at 434MHz frequency band displayed with a 50MHz span

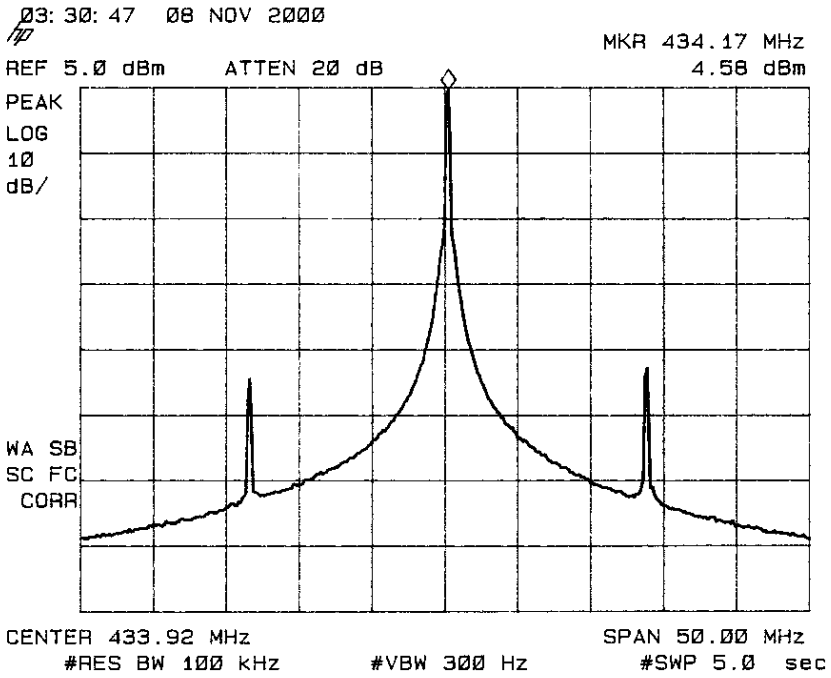


Figure 7: RF spectrum at 434MHz frequency band displayed with a 1.5GHz span

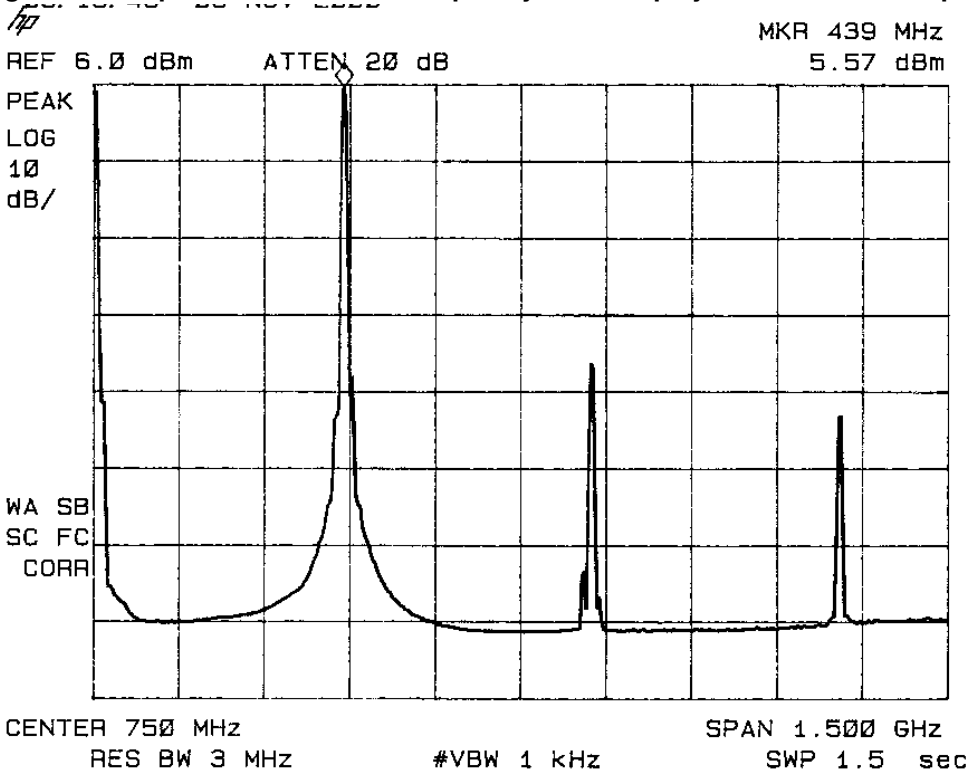
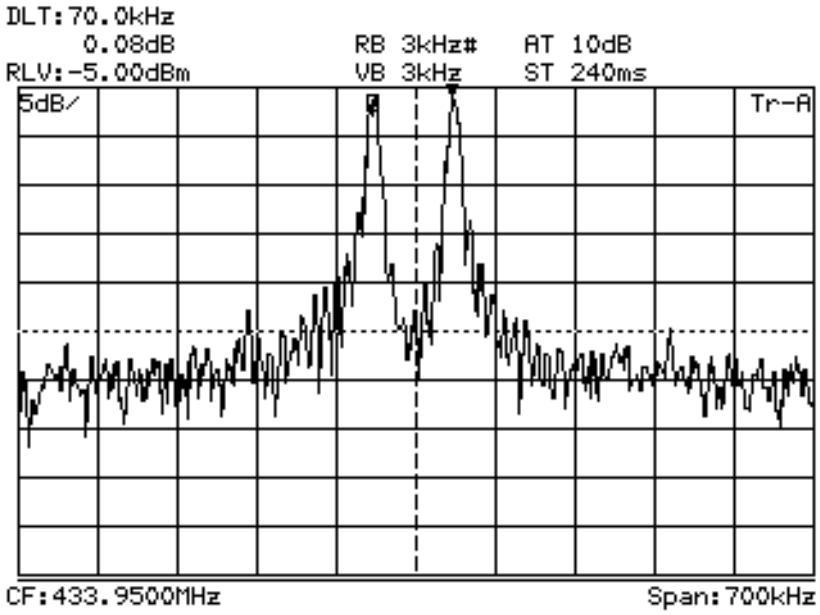


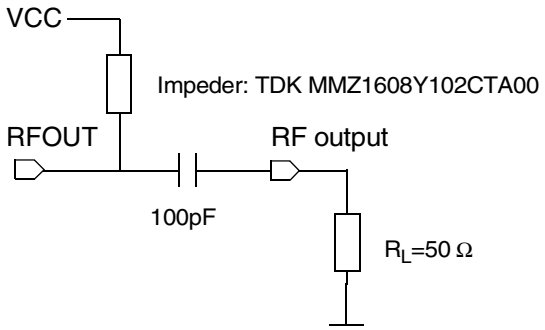
Figure 8: RF spectrum at 434MHz band for a 70kHz FSK deviation at 4.8kbit/s



OUTPUT POWER MEASUREMENT

The RF output levels given in the electrical characteristics section are measured with a 50Ω load directly connected to the pin RFOUT as shown below in figure 9. This wideband coupling method gives results independent of the application.

Figure 9: Output power measurement configurations



The configuration shown in figure 10-a provides a better efficiency in terms of output power and harmonics rejection. Schematic on figure 10-b gives the equivalent circuit of the pin RFOUT and the DC bias impeder as well as the matching network components for 434MHz frequency band.

Figure 10: Output model and matching network for 434MHz band

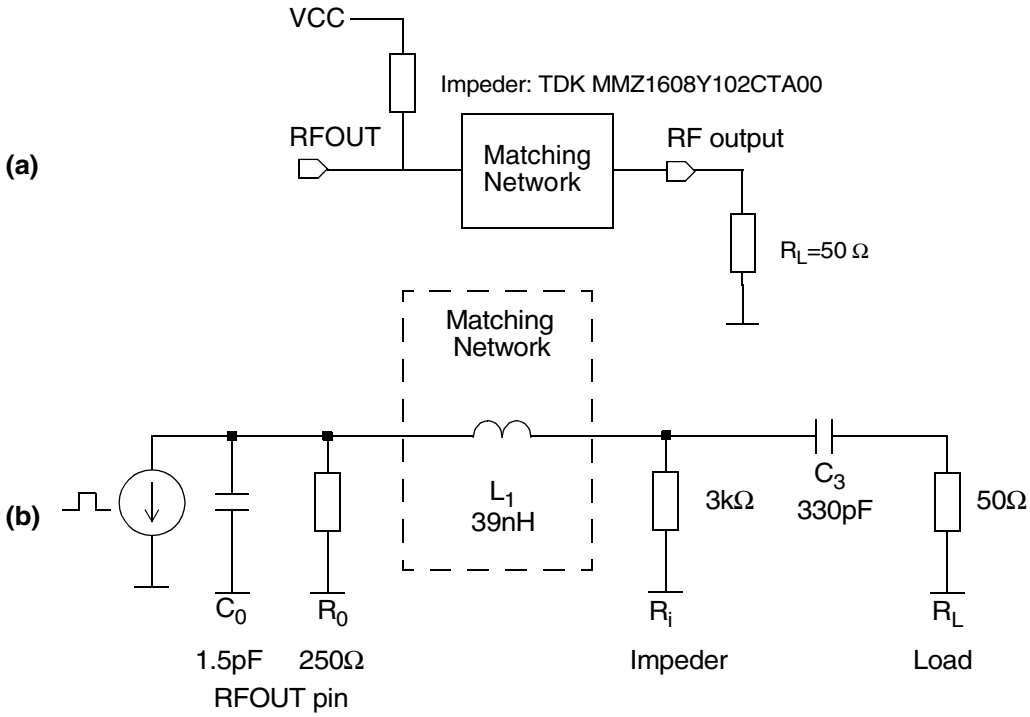
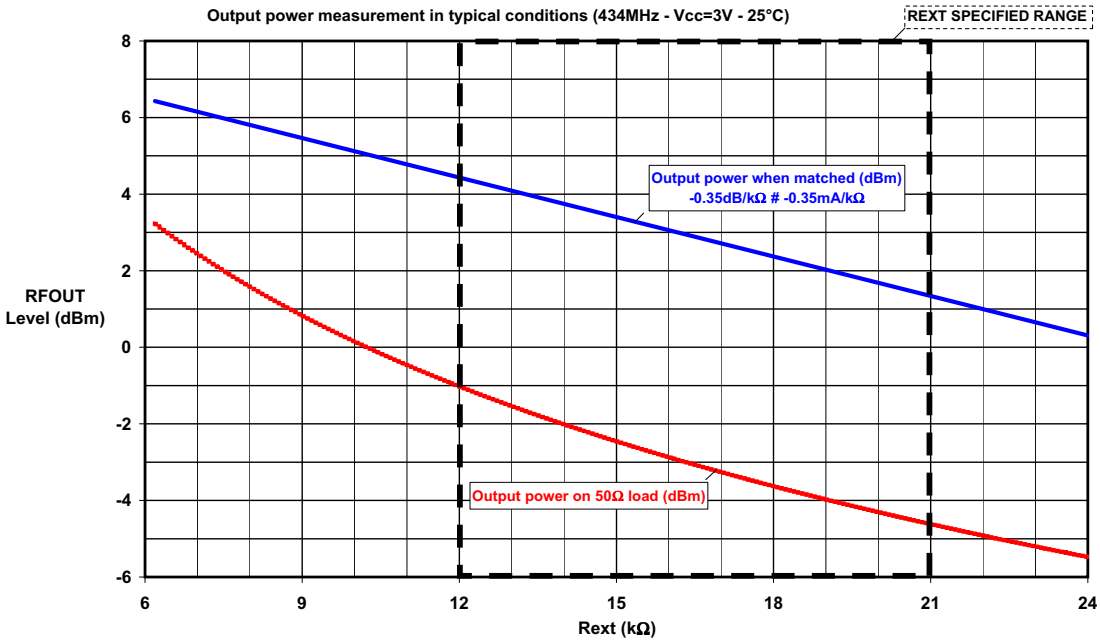


Figure 11 gives the output power versus the R_{ext} resistor value with 50Ω load and with matching network.

Figure 11: Output power at 434MHz band vs R_{ext} value

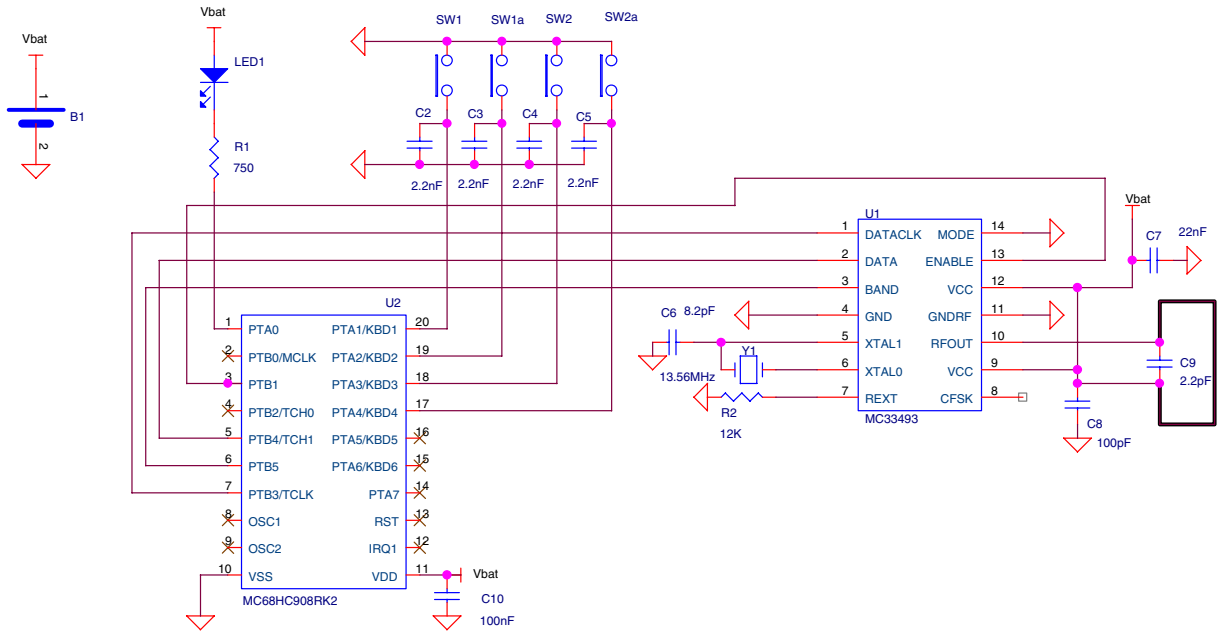


The 50Ω matching network used for the 868MHz band is similar to the 434MHz, except components values: in figure 10b, L1 is changed to 8.2nH and C3 to 470pF. The typical gain of this 868MHz matching network is 4dB compared to unmatched configuration.

COMPLETE APPLICATION SCHEMATIC AND PCB FOR OOK MODULATION

Figure 12 gives a complete application schematic using a Motorola MC68HC908RK2 microcontroller. OOK modulation is selected, $f_{carrier}$= 433.92MHz. C_2 to C_5 capacitors can be removed if switches debounce is done by software.

Figure 12: Application schematic for OOK modulation, 434MHz frequency band



Note that for 868MHz band application, the input pin BAND must be wired to ground. See component description

on following tables 3 and 4.

Table 3: External components description for OOK

Component	Function	Value	Unit
Y1	Crystal, see table 4	315MHz band: 9.84	MHz
		434MHz band: 13.56	MHz
		868MHz band: 13.56	MHz
R2	RF output level setting resistor (R_{ext})	12	kΩ
C6	Crystal load capacitor	8.2, see note 3	pF
C7	Power supply decoupling capacitors	22	nF
C8		100	pF

Note 3: C6 value equals recommended crystal load capacitance reduced by the PCB stray capacitances.
Examples of crystal reference are given below (see characteristics on table 4) for different application bands:

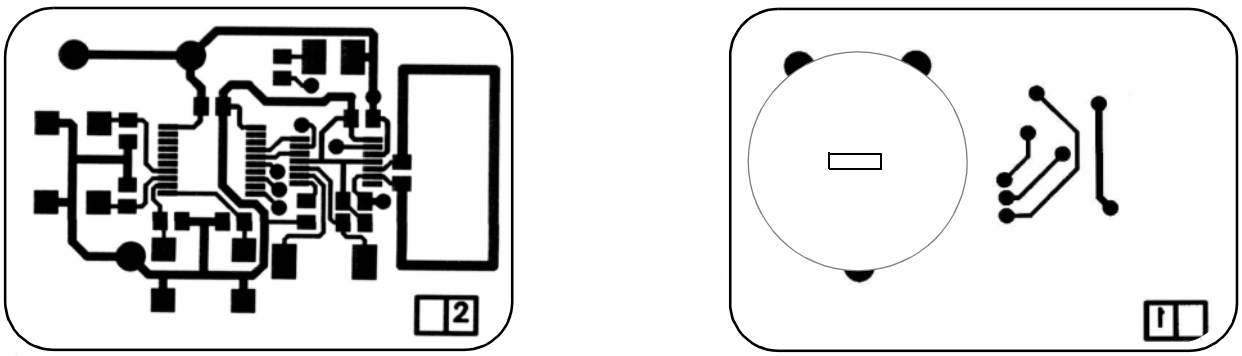
- at 315MHz band ($f_{reference}$= 9.84375MHz, -40°C < T_A < 85°C): NDK LN-G102-950,
- at 434/868MHz bands ($f_{reference}$= 13.56MHz, -40°C < T_A < 125°C):
  NDK NX8045GB/CSJ S1-40125-8050-12 and NDK NX1255GA.

Table 4: Typical crystal characteristics (SMD package)

Parameter	NDK LN-G102-950 (for 315MHz)	NDK NX8045GB/CSJ S1-40125-8050-12 (for 434MHz & 868MHz)	NDK NX1255GA (for 434MHz & 868MHz)	Unit
Load capacitance	12	12	12	pF
Motional capacitance	3.33	4.4	10.5	fF
Static capacitance	1.05	1.5	2.46	pF
Loss resistance	28	18.5	10	Ω

Figure 13 shows a two buttons keyfob board. Size is 30 x 45 millimeters.

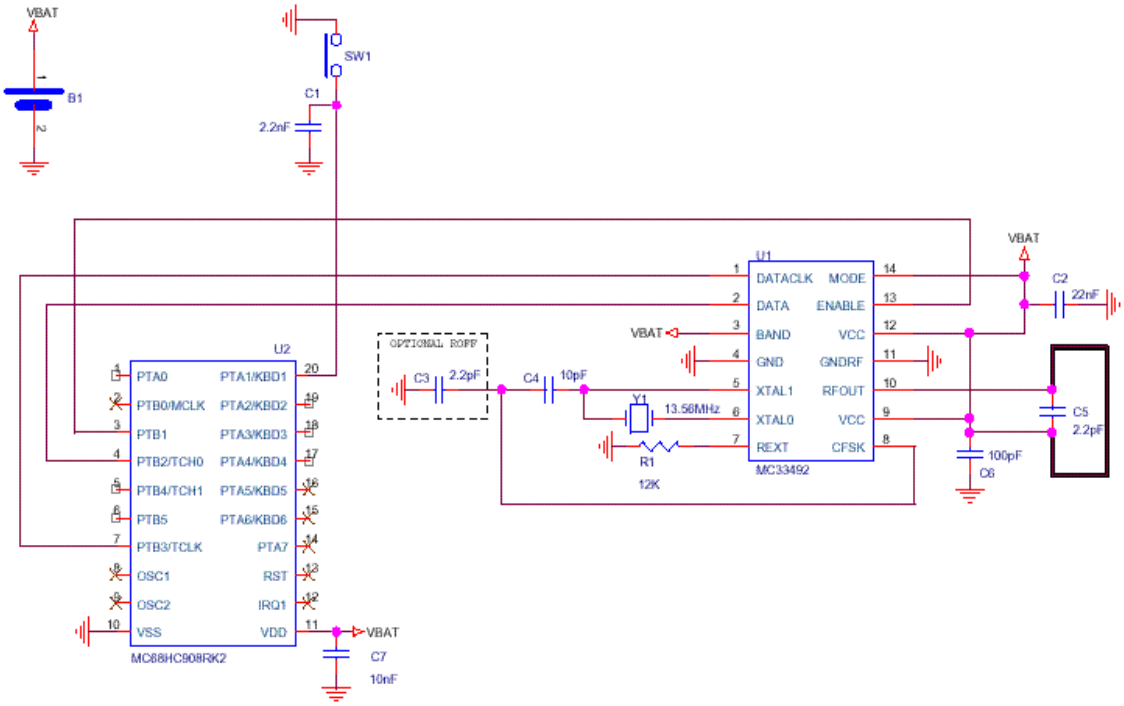
Figure 13: Two buttons keyfob board layout



COMPLETE APPLICATION SCHEMATIC AND PCB FOR FSK MODULATION

Figure 14 gives a complete application schematic using a Motorola MC68HC908RK2 microcontroller. FSK modulation is selected, $f_{carrier}$= 433.92MHz. C_1 capacitor can be removed if switch debounce is done by software.

Figure 14: .Application schematic for FSK modulation, serial configuration, 434MHz frequency band



Note that for 868MHz band application, the input pin BAND must be wired to ground. See component description on table 5.

Table 5: External components description for FSK

Component	Function	Value	Unit
Y1	Crystal	315MHz band: 9.84, see table 4	MHz
		434MHz band: 13.56, see table 4	MHz
		868MHz band: 13.56, see table 4	MHz
R1	RF output level setting resistor (R_{ext})	12	kΩ
C3	Crystal load capacitor	See table 6	pF
C4			pF
C2	Power supply decoupling capacitor	22	nF
C6		100	pF

Figure 15 gives the corresponding PCB layout.

Figure 15: Application PCB layout for FSK modulation, serial configuration, 434MHz frequency band

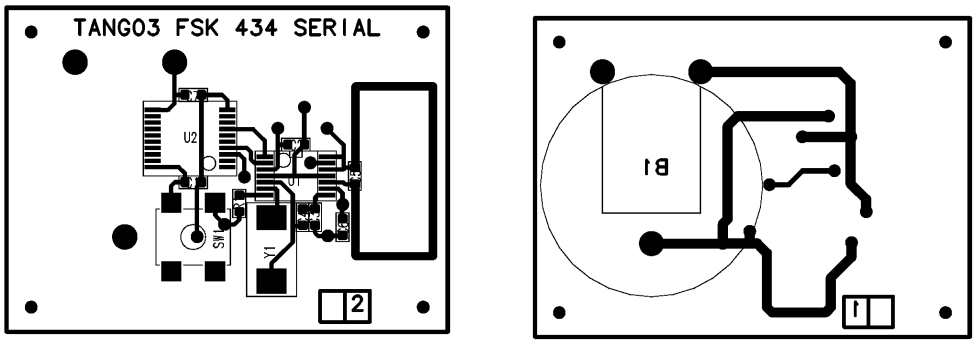


Table 6 gives the measured FSK deviations respective to C3 and C4 capacitor values for three deviations. Crystal reference is NDK NX8045GB/CSJ S1-40125-8050-12.

Table 6 : Crystal pulling capacitor values versus carrier frequency total deviation -1-

Carrier frequency (MHz)	Carrier frequency total deviation (kHz)	C3 capacitor (pF)	C4 capacitor (pF)	Recommended R_off value (kΩ)
434	45	4.7	6.8	10
	70	2.2	10	-
	100	1	15	22
868	90	4.7	6.8	10
	140	2.2	10	-
	200	1	15	22

Another crystal reference, NDK NX1255GA (see table 4), enables to reach higher deviation as mentioned on table 7. These results are due to the higher crystal motional capacitor.

Table 7 : Crystal pulling capacitor values versus carrier frequency total deviation -2-

Carrier frequency (MHz)	Carrier frequency total deviation (kHz)	C3 capacitor value (pF)	C4 capacitor value (pF)	Recommended R_off value (kΩ)
434	150	1	27	-
868	300	1	27	-

RECOMMENDATIONS FOR FSK MODULATION

FSK deviation is function of total load capacitance presented to the crystal. This load capacitance is constituted by various contributors:

- the crystal characteristic, especially its static capacitance,
- the external load capacitors (C3, C4 as defined in figure 14 and table 6),
- the device internal capacitance of pins XTAL0, XTAL1, CFSK,
- the PCB track capacitance.

The schematic given in figure 16 shows a typical FSK application using serial capacitor configuration, where device pads and PCB track capacitances are mentioned.

Device pad capacitance is defined by the package capacitance and by the internal circuitry. Typical capacitance values for these pads are given in table 8.

Some realistic assumptions and measurements have been made concerning track parasitic capacitances for a 0.8mm FR4 double side application PCB. They are given in table 8 and the corresponding PCB layout is shown in figure 15.

To achieve large deviations, this total load capacitance need to be lowered. For a given crystal, the PCB must be very carefully laid out in order to reduce as much as possible the capacitance of the tracks wired to XTAL0,

XTAL1, CFSK pins.

Recommendation: a R_off resistor can be added in parallel with the FSK switch to optimize the transient response of demodulated signal. Table 6 gives the optimized R_off values for two deviations. Note that there is no footprint for R_off resistor on the layout figure 15. When used, this component can be soldered on top of C3.

Figure 16: Schematic detailing the crystal load capacitance contributors

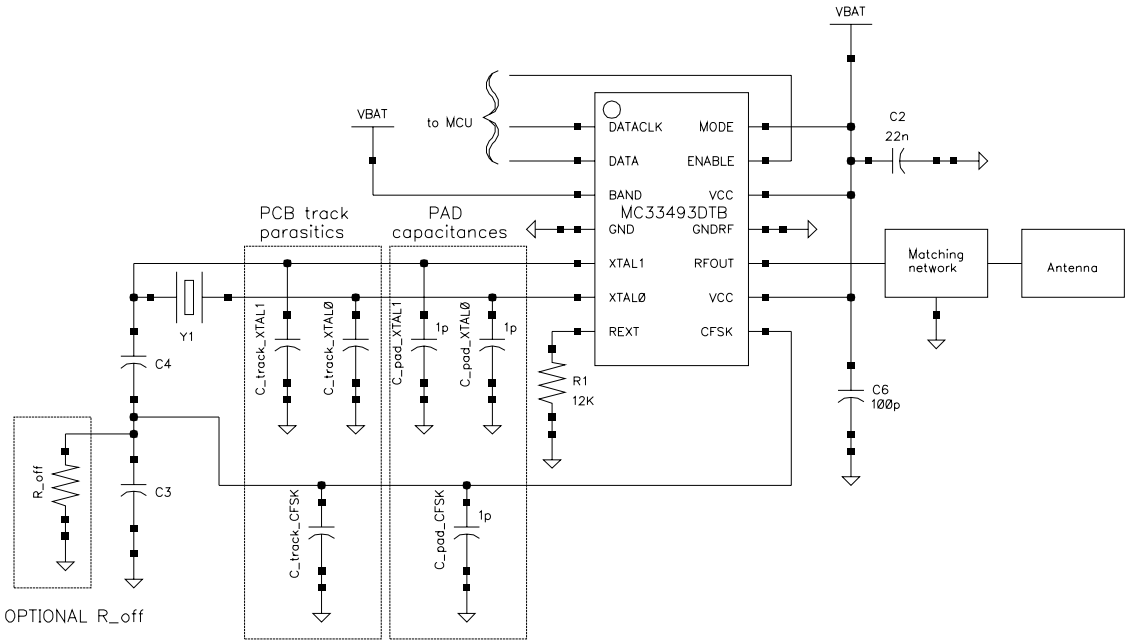
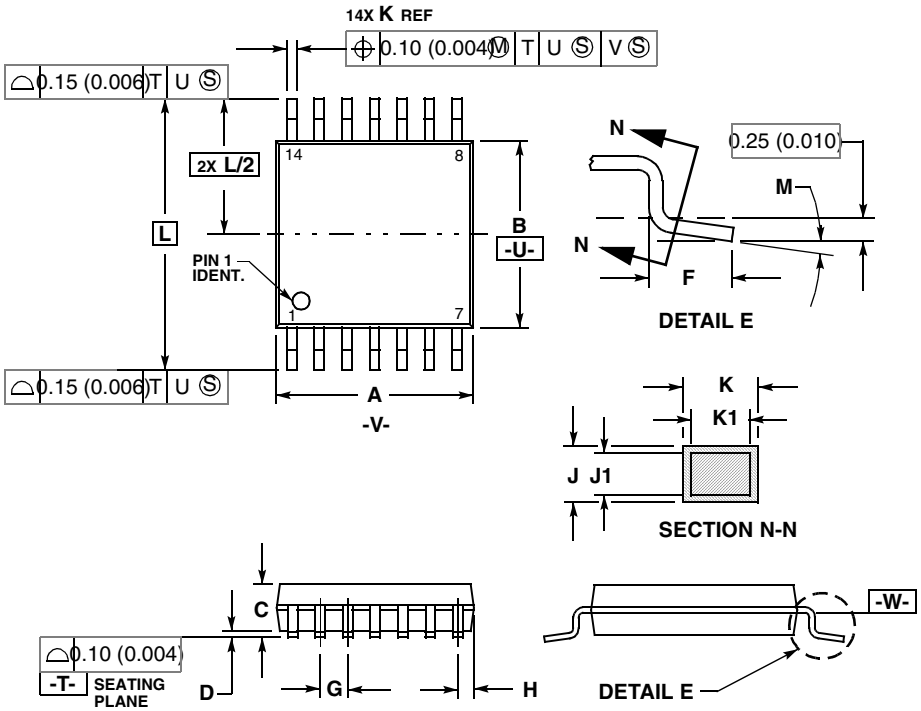


Table 8: Pads and tracks parasitic values

Capacitance	Value	Unit
C_pad_XTAL0	1	pF
C_pad_XTAL1	1	pF
C_pad_CFSK	1	pF
C_track_XTAL0	1.5	pF
C_track_XTAL1	1.5	pF
C_track_CFSK	1.5	pF

CASE OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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ISSUE O

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