Document order number: MC33886/D
Rev 2, 12/2002

**33886**

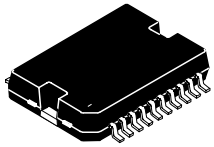
# 5.2 A H-Bridge

**5.2 A H-BRIDGE**

The 33886 is a monolithic H-Bridge ideal for fractional horsepower DC-motor and bi-directional thrust solenoid control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33886 is able to control continuous inductive DC load currents to 5.2 A. Output loads can be Pulse Width Modulation (PWM) controlled at frequencies to 10 kHz.

A Fault Status output reports undervoltage, overcurrent, and overtemperature conditions. Two independent inputs control the two half-bridge totem-pole outputs. Two disable inputs force the outputs to tristate (exhibit high impedance).

The 33886 is parametrically specified over a temperature range of -40°C ≤ $T_A$ ≤ 125°C, 5.0 V ≤ $V_{PWR}$ ≤ 28 V, and is available in an economical surface mount package.



**DH SUFFIX**
**PLASTIC PACKAGE**
**20-LEAD HSOP**
**CASE 979C**

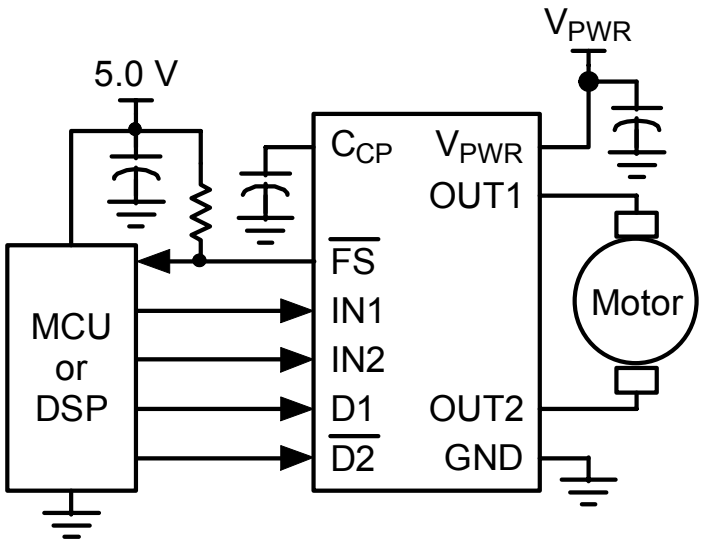
**Features**

- Direct Replacement for MC33186DH1 in the HSOP20 Package
- 5.0 V to 30 V Operation
- 120 mΩ $R_{DS(ON)}$ H-Bridge Switches
- TTL / CMOS Compatible Inputs
- PWM Frequencies to 10 kHz
- Automatic PWM Overcurrent Limiting
- Output Short Circuit Protection
- Overtemperature Output Current Reduction with Shutdown
- Undervoltage Shutdown
- Fault Status Reporting

**ORDERING INFORMATION**

| Device | Temperature Range ($T_A$) | Package |
|---|---|---|
| PC33886DH/R2 | -40 to 125°C | 20 HSOP |

**33886 Simplified Application Diagram**



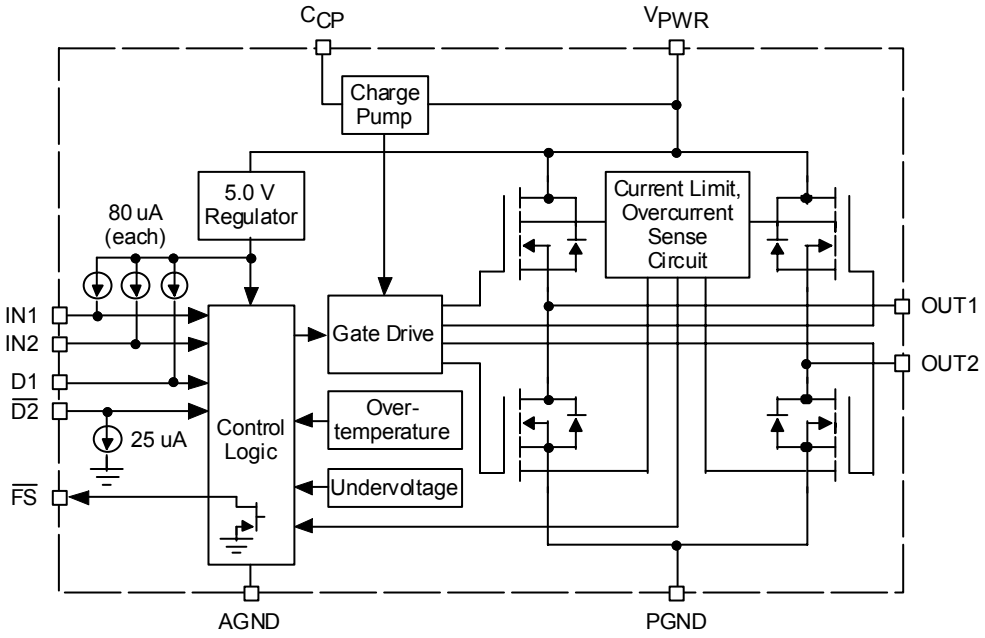
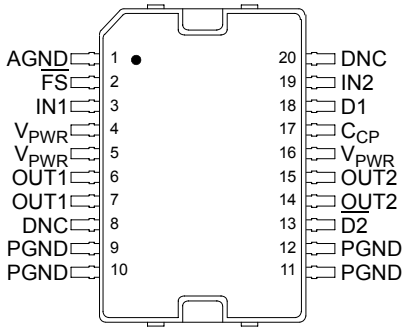



**Figure 1. 33886 Internal Block Diagram**




**PIN FUNCTION DESCRIPTION**

| Pin | Pin Name | Description |
|---|---|---|
| 1 | AGND | Low current Analog signal ground. |
| 2 | $\overline{FS}$ | Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V. |
| 3 | IN1 | True Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH). |
| 4, 5, 16 | $V_{PWR}$ | Positive power source connection. |
| 6, 7 | OUT1 | H-Bridge output 1. |
| 8, 20 | DNC | Connect these pins to ground in the application. They are test mode pins used in manufacturing only. |
| 9–12 | PGND | Device high current power ground. |
| 13 | $\overline{D2}$ | Active LOW input used to simultaneously tristate disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tristate. |
| 14, 15 | OUT2 | H-Bridge output 2. |
| 17 | $C_{CP}$ | External reservoir capacitor connection for internal Charge Pump. |
| 18 | D1 | Active HIGH input used to simultaneously tristate disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tristate. |
| 19 | IN2 | True Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH). |

**MAXIMUM RATINGS**

All voltages are with respect to ground unless otherwise noted.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage<br>Normal Operation (Steady-State)<br>Transient (Note 1) | <br>$V_{PWR(SS)}$<br>$V_{PWR(t)}$ | <br>30<br>30 to 40 | V |
| Input Voltage (Note 2) | $V_{IN}$ | 7.0 | V |
| $\overline{FS}$ Status Output (Note 3) | $V_{\overline{FS}}$ | 7.0 | V |
| Continuous Output Current (Note 4) | $I_{OUT(CONT)}$ | 5.2 | A |
| ESD Voltage<br>Human Body Model (Note 5)<br>Machine Model (Note 6) | <br>$V_{ESD1}$<br>$V_{ESD2}$ | <br>±2000 (Note 7)<br>±200 | V |
| Storage Temperature | $T_{STG}$ | -65 to 150 | °C |
| Ambient Temperature (Note 8) | $T_A$ | -40 to 125 | °C |
| Operating Junction Temperature | $T_J$ | -40 to 150 | °C |
| Lead Soldering Temperature (Note 9) | $T_{SOLDER}$ | 260 | °C |
| Approximate Junction-to-Board Thermal Resistance (Note 10) | $R_{\theta J-B}$ | ~5.0 | °C/W |

Notes

1. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
2. Exceeding the input voltage on IN1, IN2, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
3. Exceeding the pull-up resistor voltage on the open Drain $\overline{FS}$ pin may cause permanent damage to the device.
4. Continuous output current capability so long as junction temperature is $\leq$ 150°C.
5. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω).
7. All pins are capable of Human Body Model ESD voltages of ±2000 V with two exceptions: (1) $\overline{D2}$ to PGND is capable of ±1500 V and (2) OUT1 to AGND is capable of ±1000 V.
8. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
9. Lead soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. Exposed heat sink pad plus the power and ground terminals comprise the main heat conduction paths. The actual $R_{\theta J-B}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace.A

**STATIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V and -40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Supply** | | | | | |
| Operating Voltage Range | | | | | V |
| Steady-State (Note 11) | $V_{PWR(SS)}$ | 5.0 | – | 30 | |
| Transient (t < 500 ms) (Note 12) | $V_{PWR(t)}$ | – | – | 40 | |
| Standby Supply Current | $I_{PWR(standby)}$ | | | | mA |
| $V_{EN}$ = 5.0 V, $I_{LOAD}$ = 0 A | | – | – | 20 | |
| Threshold Supply Voltage | | | | | |
| Switch-OFF | $V_{PWR(thres-OFF)}$ | 4.15 | 4.4 | 4.65 | V |
| Switch-ON | $V_{PWR(thres-ON)}$ | 4.5 | 4.75 | 5.0 | V |
| Hysteresis | $V_{PWR(hys)}$ | 150 | – | – | mV |
| **Charge Pump** | | | | | |
| Charge Pump Voltage | $V_{CP}$ - $V_{PWR}$ | | | | V |
| $V_{PWR}$ = 4.15 V | | 3.35 | – | – | |
| $V_{PWR}$ < 40 V | | – | – | 20 | |
| **Control Inputs** | | | | | |
| Input Voltage (IN1, IN2, D1, $\overline{D2}$) | | | | | V |
| Threshold HIGH | $V_{IH}$ | 3.5 | – | – | |
| Threshold LOW | $V_{IL}$ | – | – | 1.4 | |
| Hysteresis | $V_{HYS}$ | 0.7 | 1.0 | – | |
| Input Current (IN1, IN2, D1) (Note 13) | $I_{IN}$ | | | | µA |
| $V_{IN}$ = 0 V | | -200 | -80 | – | |
| $\overline{D2}$ Input Current (Note 14) | $I_{\overline{D2}}$ | | | | µA |
| $V_{\overline{D2}}$ = 5.0 V | | – | 25 | 100 | |

Notes

11. Development specifications are characterised over the range of 5.0 V ≤ $V_{PWR}$ ≤ 28 V. However, the device is functional from 5.0 V to 30 V.
12. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
13. Inputs IN1, IN2, and D1 have independent internal pull-up current sources.
14. The $\overline{D2}$ input incorporates an active internal pull-down current sink.

**STATIC ELECTRICAL CHARACTERISTICS (continued)**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V and -40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Outputs (OUT1 and OUT2)** | | | | | |
| Output-ON Resistance (Note 15) | $R_{OUT}$ | | | | mΩ |
| 5.0 V < $V_{PWR}$ < 28 V, $T_J$ = 25°C | | – | 120 | – | |
| 8.0 V < $V_{PWR}$ < 28 V, $T_J$ = 150°C | | – | – | 225 | |
| 5.0 V < $V_{PWR}$ < 8.0 V, $T_J$ = 150°C | | – | – | 300 | |
| Output Latch-OFF Current (Note 16) | $I_{LATCH-OFF}$ | 5.2 | 6.5 | 7.8 | A |
| High-Side Overcurrent Detection | $I_{OCD(H)}$ | 11 | – | – | A |
| Low-Side Overcurrent Detection | $I_{OCD(L)}$ | 8.0 | – | – | A |
| Leakage Current (Note 17) | $I_{OUT(leak)}$ | | | | µA |
| $V_{OUT}$ = $V_{PWR}$ | | – | 100 | 200 | |
| $V_{OUT}$ = GND | | – | 30 | 60 | |
| Free-Wheeling Diode Forward Voltage Drop (Note 18) | $V_F$ | | | | V |
| $I_{OUT}$ = 3.0 A | | – | – | 2.0 | |
| Switch-OFF | | | | | °C |
| Thermal Shutdown | $T_{LIM}$ | 175 | – | – | |
| Hysteresis | $T_{HYS}$ | – | 15 | – | |
| **Fault Status** (Note 19) | | | | | |
| Fault Status Leakage Current (Note 20) | $I_{\overline{FS}(leak)}$ | | | | µA |
| $V_{\overline{FS}}$ = 5.0 V | | – | – | 10 | |
| Fault Status SET Voltage (Note 21) | $V_{\overline{FS}(LOW)}$ | | | | V |
| $I_{\overline{FS}}$ = 300 µA | | – | – | 1.0 | |

Notes

15. Output-ON resistance as measured from output to $V_{PWR}$ and GND.
16. Product with date codes of December 2002, week 51, will exhibit the values indicated in this table. Product with earlier date codes may exhibit a minimum of 6.0 A and a maximum of 8.5 A.
17. Outputs switched OFF with D1 or $\overline{D2}$.
18. Parameter is guaranteed by design but not production tested.
19. Fault Status output is an open Drain output requiring a pull-up resistor to 5.0 V.
20. Fault Status Leakage Current is measured with Fault Status HIGH and *not* SET.
21. Fault Status Set Voltage is measured with Fault Status LOW and SET with $I_{\overline{FS}}$ = 300 µA.

**DYNAMIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V and -40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Timing Characteristics** | | | | | |
| PWM Frequency (Note 22) | $f_{PWM}$ | – | – | 10 | kHz |
| Maximum Switching Frequency During Current Limit (Note 23) | $f_{MAX}$ | – | – | 20 | kHz |
| Output ON Delay (Note 24)<br>$V_{PWR}$ = 14 V | $t_{d(ON)}$ | – | – | 18 | µs |
| Output OFF Delay (Note 24)<br>$V_{PWR}$ = 14 V | $t_{d(OFF)}$ | – | – | 18 | µs |
| Output Rise and Fall Time (Note 25)<br>$V_{PWR}$ = 14 V, $I_{out}$ = 3.0 A | $t_f$, $t_r$ | 2.0 | 5.0 | 8.0 | µs |
| Output Latch-OFF Time | $t_a$ | 15 | 20.5 | 26 | µs |
| Output Blanking Time | $t_b$ | 12 | 16.5 | 21 | µs |
| Free-Wheeling Diode Reverse Recovery Time (Note 26) | $t_{rr}$ | 100 | – | – | ns |
| Disable Delay Time (Note 27) | $t_{d(disable)}$ | – | – | 8.0 | µs |
| Over-Current/Temperature Turn-OFF Time (Note 28) | $t_{FAULT}$ | – | 4.0 | – | µs |
| Power-OFF Delay Time | $t_{pod}$ | – | 1.0 | 5.0 | ms |

Notes

22. The outputs can be PWM controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. Refer to Typical Switching Waveforms, Figure 8 through Figure 15.
23. The Maximum Switching Frequency during Current Limit is internally implemented. The internal control produces a constant OFF-time PWM of the output. The output load current effects the Maximum Switching Frequency.
24. Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 3.
25. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 4.
26. Parameter is guaranteed by design but not production tested.
27. Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tristate response. See Figure 3.
28. Increasing output currents will become limited at 6.5 A. Hard shorts will breach the 6.5 A limit, forcing the output into an immediate tristate latch-OFF. See Figure 6 and Figure 7. Output current limiting will cause junction temperatures to rise. A junction temperature above 160°C will cause the output current limit to progressively "fold-back" (or decrease) to 2.5 A typical at 175°C where thermal latch-OFF will occur. See Figure 5.

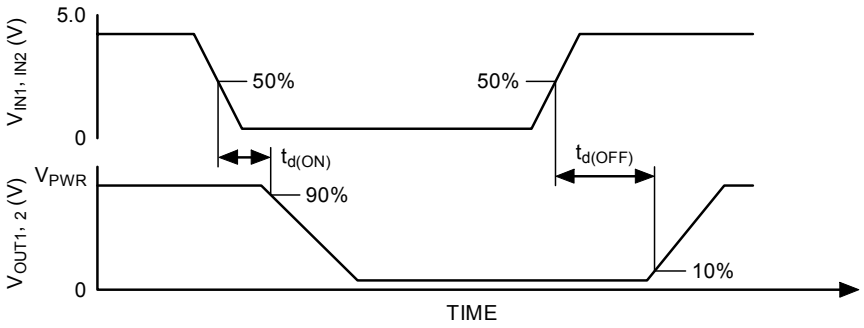



**Figure 2. Output Delay Time**

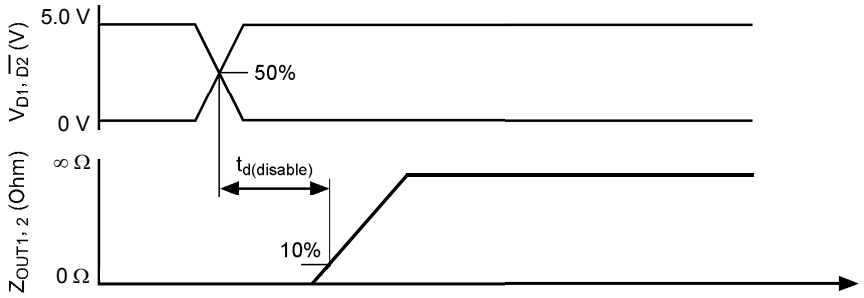



**Figure 3. Disable Delay Time**


**Figure 4. Output Switching Time**

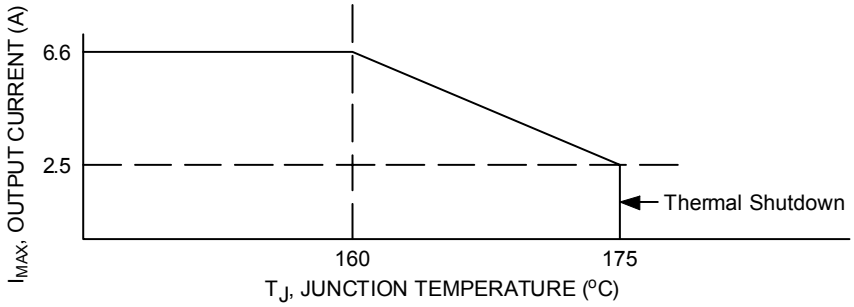



**Figure 5. Output Current Limiting Versus Temperature (Typical)**

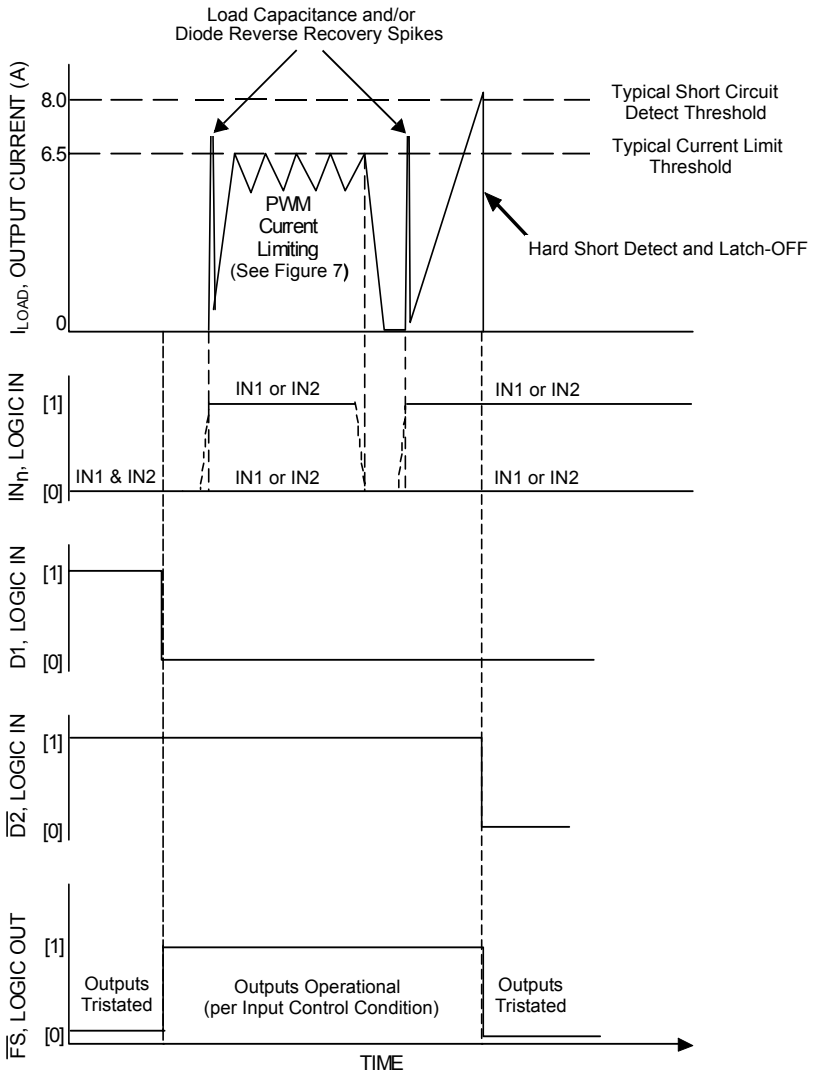



**Figure 6. Output Load Current Limiting Versus Time**

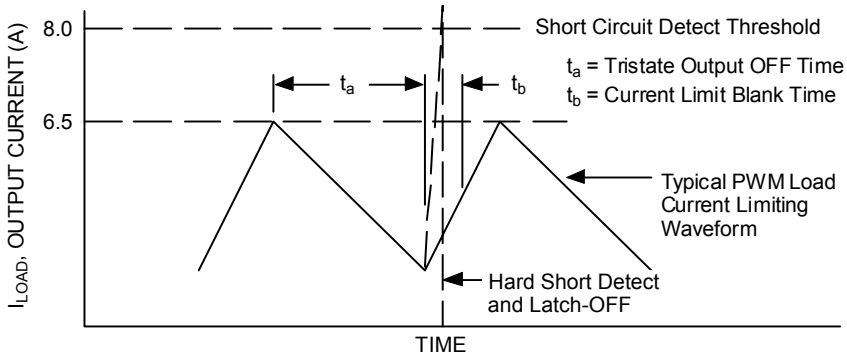



**Figure 7. PWM Current Limiting Detail**

## Typical Switching Waveforms

**Important** For all plots, the following applies:

- Ch2=2.0 A per division
- $L_{LOAD}$=533 µH @ 1.0 kHz
- $L_{LOAD}$=530 µH @ 10.0 kHz
- $R_{LOAD}$=4.0 Ω

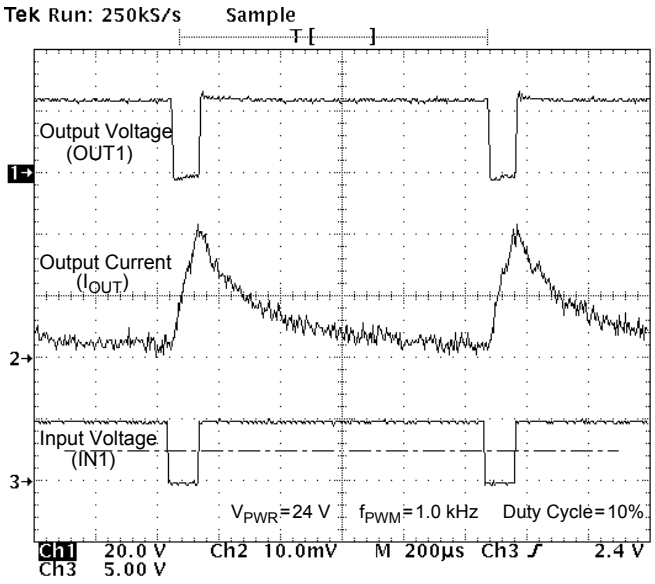



**Figure 8. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 10%**

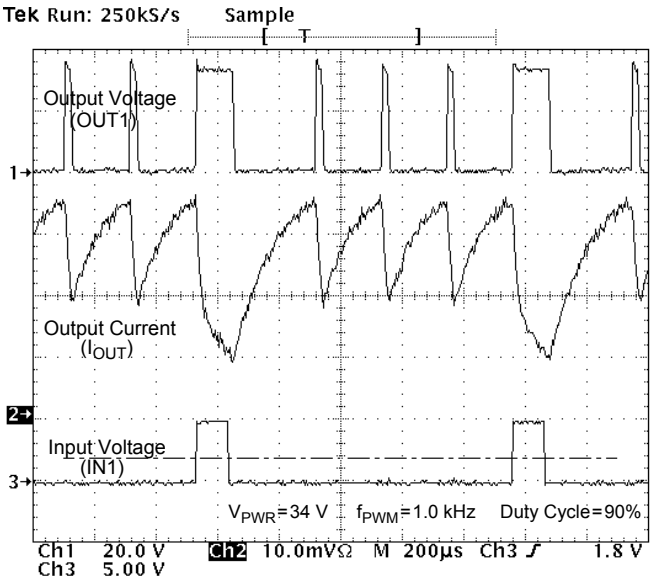



**Figure 10. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=34 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%, Showing Device in Current Limiting Mode**

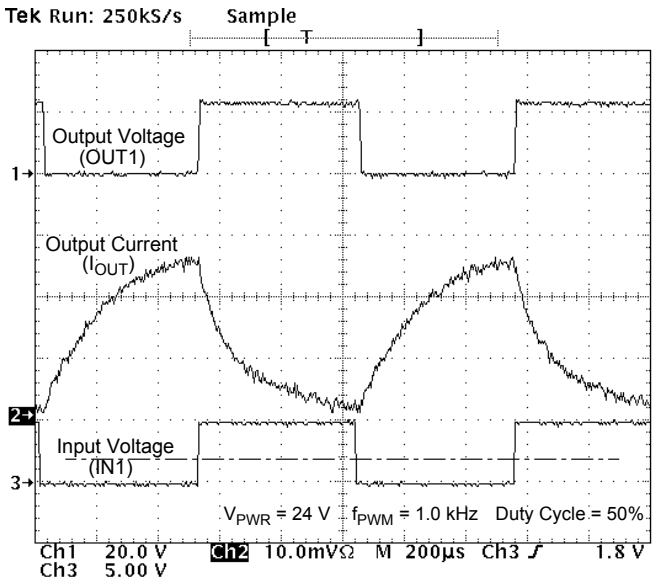



**Figure 9. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 50%**

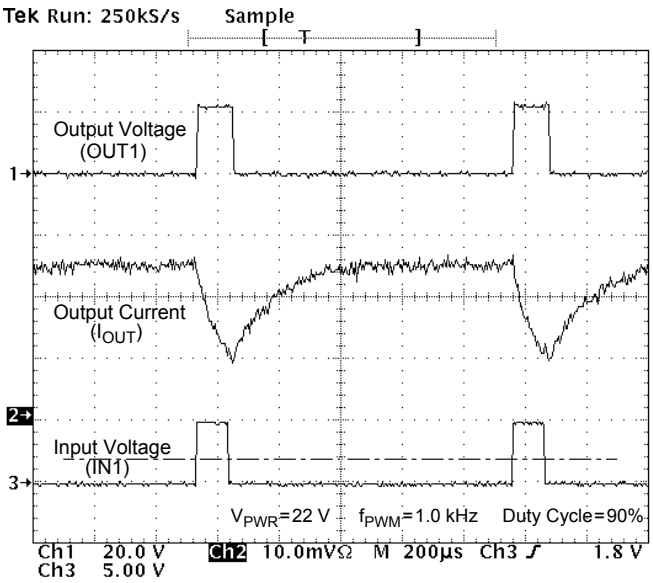



**Figure 11. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=22 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%**

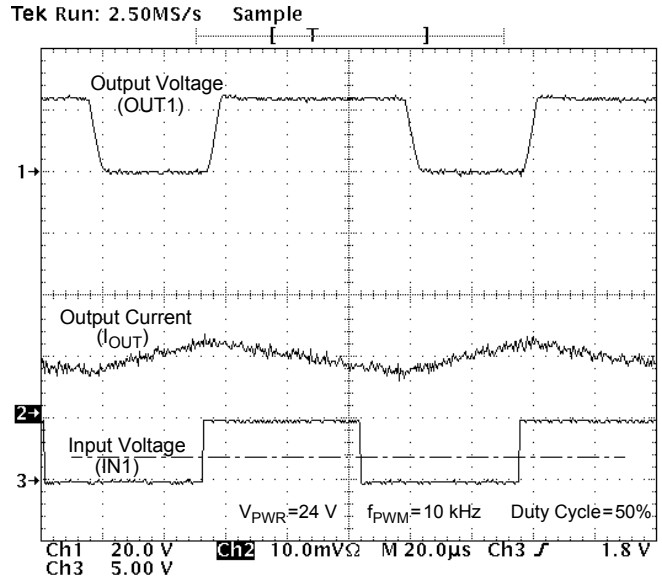



**Figure 12. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=24 V, PMW Frequency of 10 kHz, and Duty Cycle of 50%**

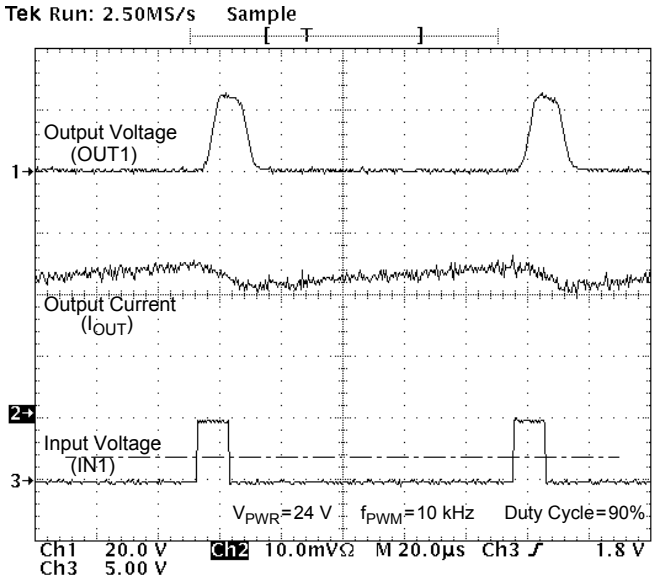



**Figure 13. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=24 V, PMW Frequency of 10 kHz, and Duty Cycle of 90%**

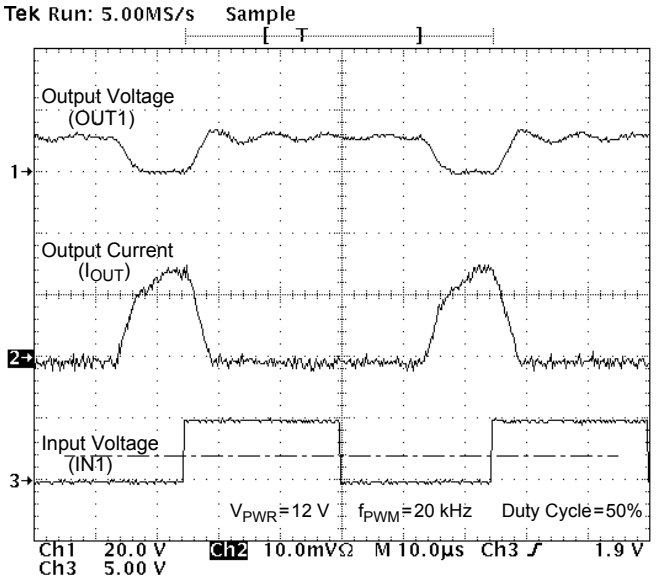



**Figure 14. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=12 V, PMW Frequency of 20 kHz, and Duty Cycle of 50% for a Purely Resistive Load**

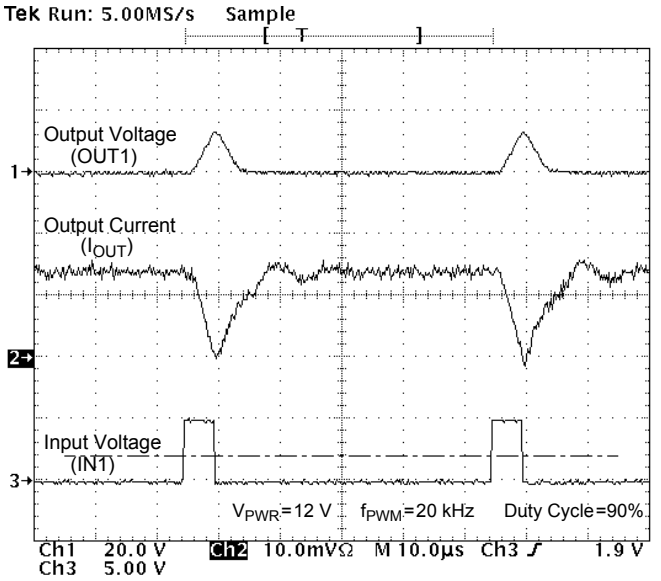



**Figure 15. Output Voltage and Output Current vs. Input Voltage at $V_{PWR}$=12 V, PMW Frequency of 20 kHz, and Duty Cycle of 90% for a Purely Resistive Load**

**Table 1. Truth Table**

The tristate conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = Low, H = High, X = High or Low, and Z = High impedance (all output power transistors are switched off).

| Device State | Input Conditions | | | | Status | Outputs | |
|---|---|---|---|---|---|---|---|
| | D1 | $\overline{D2}$ | IN1 | IN2 | $\overline{FS}$ | OUT1 | OUT2 |
| Forward | L | H | H | L | H | H | L |
| Reverse | L | H | L | H | H | L | H |
| Free Wheeling Low | L | H | L | L | H | L | L |
| Free Wheeling High | L | H | H | H | H | H | H |
| Disable 1 (D1) | H | X | X | X | L | Z | Z |
| Disable 2 ($\overline{D2}$) | X | L | X | X | L | Z | Z |
| IN1 Disconnected | L | H | Z | X | H | H | X |
| IN2 Disconnected | L | H | X | Z | H | X | H |
| D1 Disconnected | Z | X | X | X | L | Z | Z |
| $\overline{D2}$ Disconnected | X | Z | X | X | L | Z | Z |
| Undervoltage (Note 29) | X | X | X | X | L | Z | Z |
| Overtemperature (Note 30) | X | X | X | X | L | Z | Z |
| Overcurrent (Note 30) | X | X | X | X | L | Z | Z |

Notes

29. In the case of an undervoltage condition, the outputs tristate and the fault status is SET logic LOW. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
30. When an overcurrent or overtemperature condition is detected, the power outputs are tristate latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

# SYSTEM / APPLICATION INFORMATION

## INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic breaking, and PWM control), in addition to the 5.2 A output current capability, make the 33886 a very attractive, cost-effective solution for controlling a broad range of fractional horsepower DC-motors. A pair of 33886 devices can be used to control bipolar stepper motors in both directions. In addition, the 33886 can be used to control permanent magnet solenoids in a push-pull variable force fashion using PWM control. The 33886 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, Internal Block Diagram, the 33886 is a fully protected monolithic H-Bridge with Fault Status reporting. For a DC-motor to run the input conditions need be as follows: D1 input logic LOW, $\overline{D2}$ input logic HIGH, $\overline{FS}$ flag cleared (logic HIGH), with one IN logic LOW and the other IN logic HIGH to define output polarity. The 33886 can execute Dynamic Breaking by simultaneously turning-ON either the two High-Side or the two Low-Side H-Bridge switches; e.g., IN1 and IN2 logic HIGH or IN1 and IN2 logic LOW.

The 33886 outputs are capable of providing a continuous DC load current of 5.2 A from a 36 V $V_{PWR}$ source. An internal charge pump supports PWM frequencies up to 10 kHz. An external pull-up resistor is required for the open drain $\overline{FS}$ pin for fault status reporting.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) are for forcing the H-Bridge outputs to a high impedance state (all H-Bridge switches OFF).

The 33886 has Undervoltage Shutdown with automatic recovery, Output Current Limiting, Output Short-Circuit Latch-OFF, and Overtemperature Latch-OFF. An Undervoltage Shutdown, Output Short-Circuit Latch-OFF, or Overtemperature Latch-OFF fault condition will cause the outputs to turn-OFF (tristate) and the fault output flag to be set LOW. Either of the D inputs or $V_{PWR}$ must be “toggled” to clear the fault flag. The Overcurrent/Overtemperature Shutdown scheme is unique and best described as using a junction temperature dependent output current “fold back” protection scheme. When an overcurrent condition is experienced, the current limited output is “ramped down” as the junction temperature increases above 160°C, until at 175°C the output current has decreased to about 2.5 A. Above 175°C, Overtemperature Shutdown (Latch-OFF) occurs. This feature allows the device to remain in operation for a longer time with unexpected loads, but with regressive output performance at junction temperatures above 160°C.

## FUNCTIONAL PIN DESCRIPTION

### PGND and AGND

Power and analog ground pins. The power and analog ground pins should be connected together with a very low impedance connection.

### $V_{PWR}$

$V_{PWR}$ pins are the power supply inputs to the device. All $V_{PWR}$ pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

$V_{PWR}$ pins have an undervoltage threshold. If the supply voltage drops below a $V_{PWR}$ undervoltage threshold, the output power stage switches to a tristate condition and the fault status flag is SET and the Fault Status pin voltage switched to a logic LOW. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic HIGH.

### Fault Status ($\overline{FS}$)

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to 5.0 V. Refer to Table 1, Truth Table.

### IN1, IN2, D1, and $\overline{D2}$

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complimentary inputs used to tristate disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tristate disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(standby)}$ current is reduced to a few milliamperes. See Table 1, Truth Table**,** and STATIC ELECTRICAL CHARACTERISTICS table.

### OUT1 and OUT2

These pins are the outputs of the H-Bridge with integrated free-wheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have Pulse Width Modulated (PWM) current limiting above 6.5 A. The outputs also have thermal shutdown (tristate latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time $t_b$) incorporated to detect currents that are higher than current limit is activated at each output activation to facilitate detecting hard output short conditions. See Figure 7.

**$C_{CP}$**

Charge pump output pin. A filter capacitor (up to 33 nF) can be connected from the $C_{CP}$ pin and PGND. The device can operate without the external capacitor, although the $C_{CP}$ capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

## PERFORMANCE FEATURES

### Short Circuit or Overcurrent Protection

If an output overcurrent condition is detected, the power outputs tristate latched-OFF independent of the input signal states and the fault status output flag is SET logic LOW. If the D1 voltage changes from logic HIGH to logic LOW or from logic LOW to logic HIGH on $\overline{D2}$, the output switches ON again and the fault status flag is reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature.

### PWM Current Limiting

The maximum current flow under normal operating conditions is limited to $I_{MAX}$ (5.2 to 7.8 A). When the maximum current value is reached, the output stages are tristated for a fixed time ($t_a$) of 20 µs typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tristate duration until the next output ON cycle occurs. See Figure 7 and Figure 10.

The PWM current limitation value is dependent upon the device junction temperature. When -40°C < $T_J$ < 160°C, $I_{MAX}$ is between 5.2 and 7.8 A. When $T_J$ exceeds 160°C, the $I_{MAX}$ current decreases linearly down to 2.5 A typical at 175°C typical (or where the device reaches $T_{LIM}$) and overtemperature shutdown occurs. See Figure 5. This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

### Overtemperature Shutdown and Hysteresis

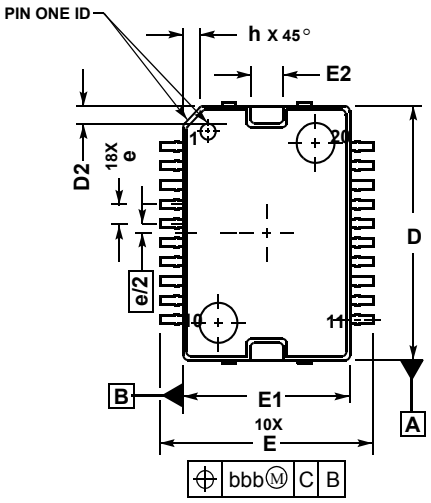
If an overtemperature condition occurs, the power outputs are tristate latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

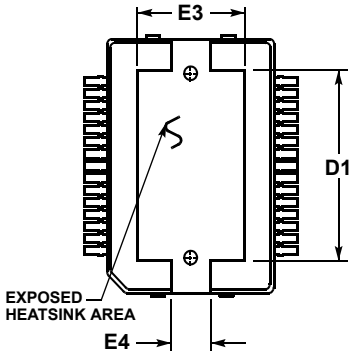
To reset from this condition, D1 must change from logic HIGH to logic LOW, or $\overline{D2}$ must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

**Note** Resetting from the fault condition will clear the fault status flag.

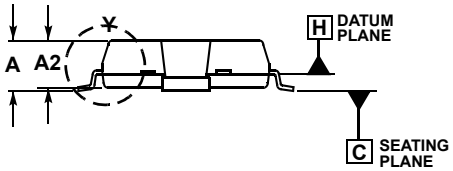
## PACKAGE DIMENSIONS

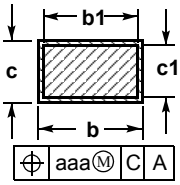
**DH SUFFIX**
(20-LEAD HSOP)
PLASTIC PACKAGE
CASE 979C-02
ISSUE A



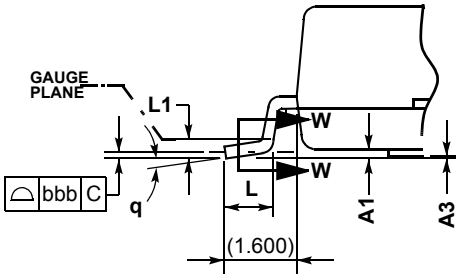




**BOTTOM VIEW**




**SECTION W-W**




**DETAIL Y**

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 3.000 | 3.400 |
| A1 | 0.100 | 0.300 |
| A2 | 2.900 | 3.100 |
| A3 | 0.00 | 0.100 |
| D | 15.800 | 16.000 |
| D1 | 11.700 | 12.600 |
| D2 | 0.900 | 1.100 |
| E | 13.950 | 14.450 |
| E1 | 10.900 | 11.100 |
| E2 | 2.500 | 2.700 |
| E3 | 6.400 | 7.200 |
| E4 | 2.700 | 2.900 |
| L | 0.840 | 1.100 |
| L1 | 0.350 BSC | |
| b | 0.400 | 0.520 |
| b1 | 0.400 | 0.482 |
| c | 0.230 | 0.320 |
| c1 | 0.230 | 0.280 |
| e | 1.270 BSC | |
| h | --- | 1.100 |
| q | 0 × | 8 × |
| aaa | 0.200 | |
| bbb | 0.100 | |

**HOW TO REACH US:**
**USA/EUROPE/LOCATIONS NOT LISTED:** Motorola Literature Distribution: P.O. Box 5405, Denver, Colorado 80217.
1-303-675-2140 or 1-800-441-2447
**JAPAN:** Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1 Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan.
81-3-3440-3569
**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T.,
Hong Kong. 852-26668334
**TECHNICAL INFORMATION CENTER:** 1-800-521-6274