Document Order Number MC33993/D
Rev 1, 12/2002

Advanced Information

Multiple Switch Detection Interface

33993

MULTIPLE SWITCH DETECTION INTERFACE

The 33993 Multiple Switch Detection Interface is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor through an SPI interface. The device also features a 22 to 1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output pin for the MCU to read.

The 33993 device has two modes of operation, Sleep and Normal. The Sleep mode provides low quiescent current and enables the wake up features of the device. Normal mode allows programming of the device and supplies switch contacts with pull-up or pull down current as it monitors switch change of state.

The 33993 is packaged in the 32-pin Wide Body SOIC, reducing circuit board area. Low quiescent current makes the 33993 ideal for automotive and industrial products requiring low sleep state currents. The internal block diagram of the 33993 is illustrated in Figure 1.

32-Lead SOIC
0.65 mm Pitch
CASE 1324-02
Issue A

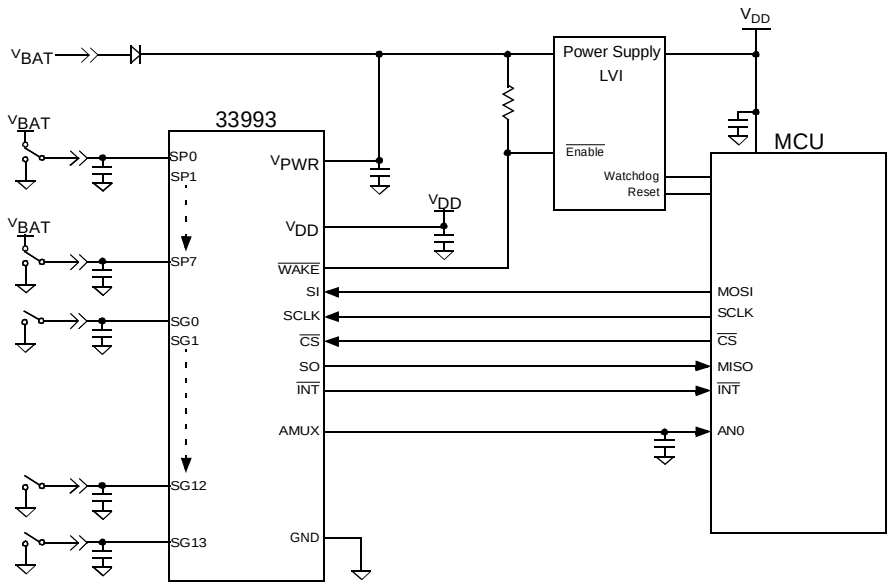
Features:

- Designed to Operate 5.5 V ≤ V_{PWR} ≤ 26 V
- Switch Input Voltage Range –14 V to VPWR, 40 V MAX
- Interfaces Directly to Microprocessor using 3.3/5.0 V SPI Protocol
- Selectable wake up on Change of State
- Selectable Wetting Current (16 mA or 2 mA)
- 8-Programmable Input (Switches to Battery or Ground)
- 14-Switch to Ground Inputs
- V_{PWR} Standby Current < 100 µA, V_{DD} Standby Current < 15 µA
- Active Interrupt ($\overline{INT}$) on Change of Switch State

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33993DWB	-40°C to 125°C	32 Ld SOIC

33993 Simplified Application Schematic



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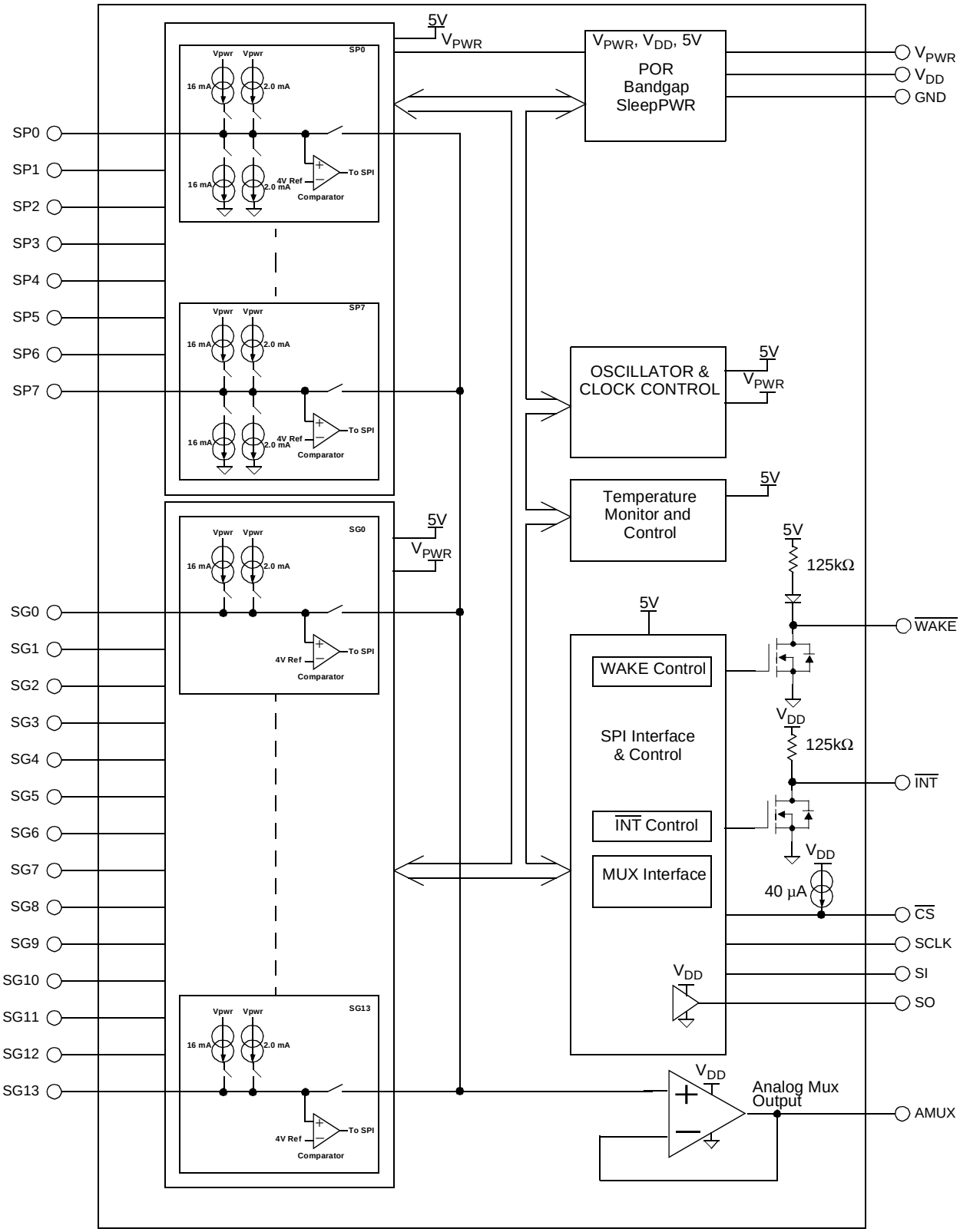


Figure 1. 33993 Block Diagram

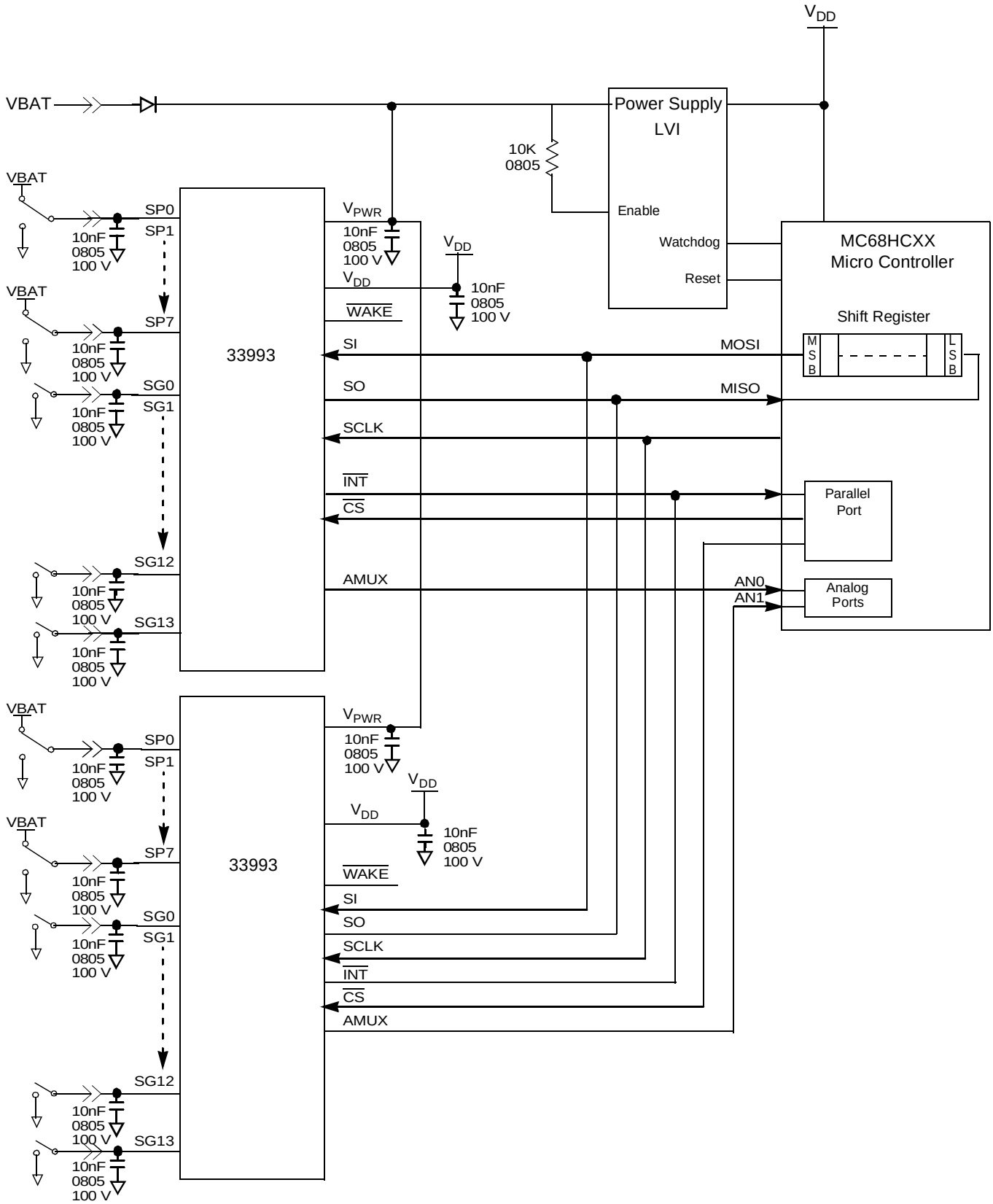


Figure 2. Power Supply Always Active

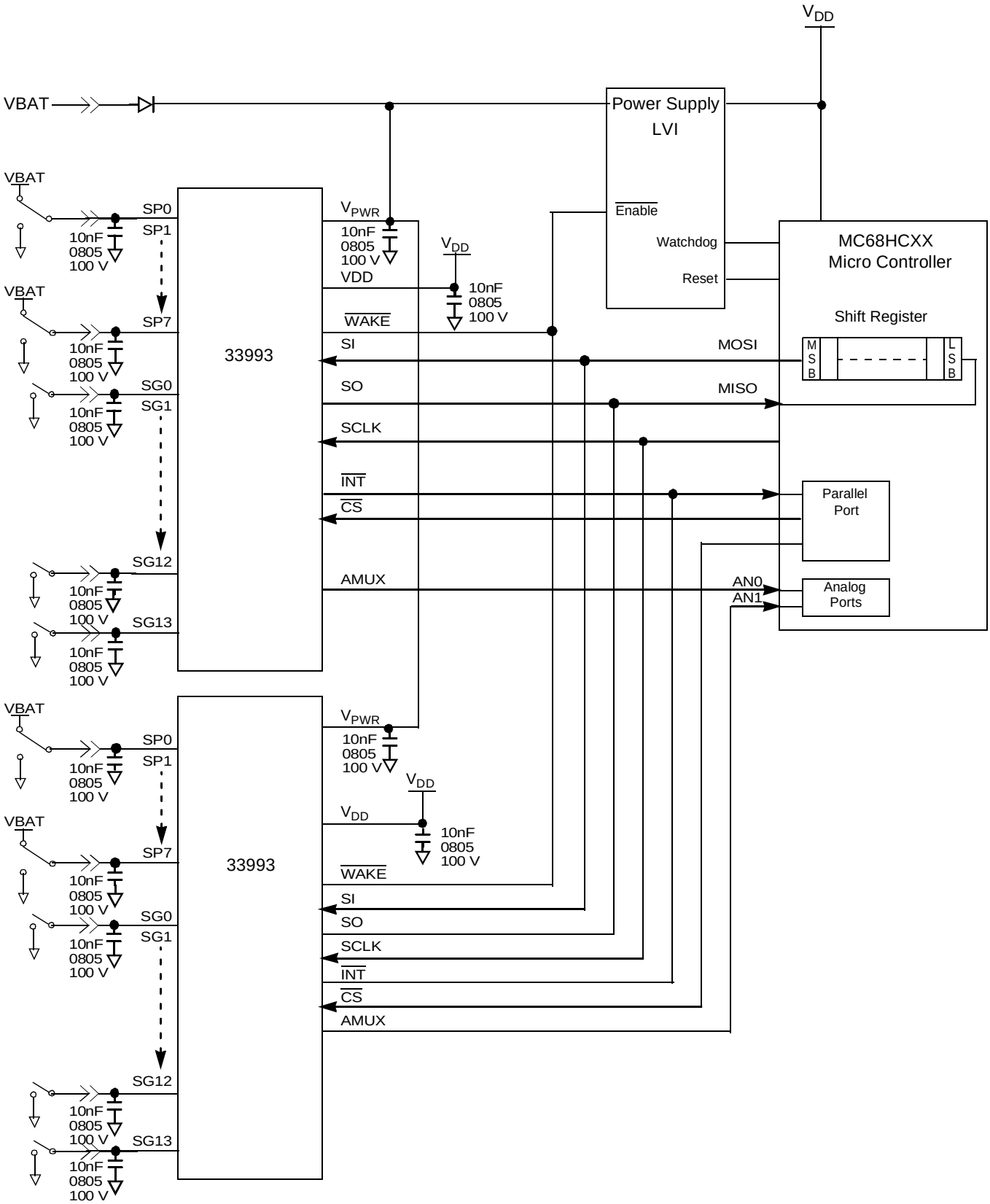
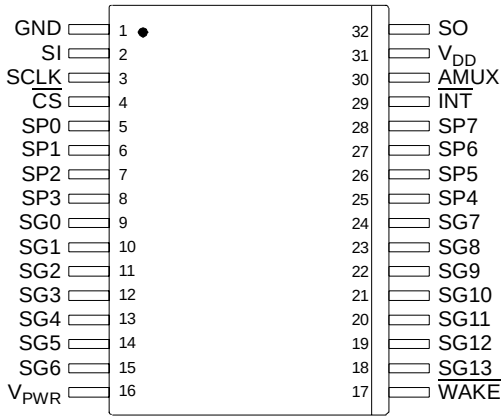


Figure 3. Power Supply Shutdown



PIN FUNCTIONAL DESCRIPTION (32 WB SOIC)

Pin No.	Name	Description
1	GND	Ground for logic, analog and switch to battery inputs.
2	SI	SPI control data input pin from MCU to 33993.
3	SCLK	SPI control clock input pin.
4	$\overline{CS}$	SPI control chip select input pin from MCU to 33993. Logic 0 allows data to be transferred in.
5	SP0	Programmable switch to battery or switch to ground input pin.
6	SP1	Programmable switch to battery or switch to ground input pin.
7	SP2	Programmable switch to battery or switch to ground input pin.
8	SP3	Programmable switch to battery or switch to ground input pin.
9	SG0	Switch to ground input pin.
10	SG1	Switch to ground input pin.
11	SG2	Switch to ground input pin.
12	SG3	Switch to ground input pin.
13	SG4	Switch to ground input pin.
14	SG5	Switch to ground input pin.
15	SG6	Switch to ground input pin.
16	V_{PWR}	Conditioned battery supply input pin. Pin requires external reverse battery protection.
17	$\overline{WAKE}$	Wake up power supply enable output - open drain output
18	SG13	Switch to ground input pin.
19	SG12	Switch to ground input pin.
20	SG11	Switch to ground input pin.
21	SG10	Switch to ground input pin.

PIN FUNCTIONAL DESCRIPTION (32 WB SOIC)

Pin No.	Name	Description
22	SG9	Switch to ground input pin.
23	SG8	Switch to ground input pin.
24	SG7	Switch to ground input pin.
25	SP4	Programmable switch to battery or switch to ground input pin.
26	SP5	Programmable switch to battery or switch to ground input pin.
27	SP6	Programmable switch to battery or switch to ground input pin.
28	SP7	Programmable switch to battery or switch to ground input pin.
29	$\overline{INT}$	Interrupt - Open drain output to MCU, used to indicate input switch change of state.
30	AMUX	Analog multiplex output
31	V_{DD}	5.0/3.3 V supply. Sets SPI communication level for SO driver.
32	SO	SPI Serial output data pin. SO provides digital data from 33993 to MCU.

MAXIMUM RATINGS

(All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
V_{DD} Supply Voltage	—	-0.3 to 7.0	VDC
$\overline{CS}$, SI, SO, SCLK, $\overline{INT}$, AMUX (Note 1)	—	-0.3 to 7.0	VDC
$\overline{WAKE}$ (Note 1)	—	-0.3 to 40	VDC
V_{PWR} Supply Voltage (Note 1)	—	-0.3 to 50	VDC
Switch Input Voltage Range	—	-14 to 40	VDC
Frequency of SPI Operation (V_{DD} = 5.0 V)	—	6	MHz
ESD Voltage (Note 2) Human Body Model (Note 3) (Note 4) Machine Model (Note 5)	 V_{ESD1} V_{ESD2}	 4000 200	V
Storage Temperature	T_{stg}	- 55 to +150	°C
Operating Case Temperature	T_C	- 40 to +125	°C
Operating Junction Temperature	T_J	- 40 to +150	°C
Power Dissipation (T_A = 25°C) (Note 6)	P_D	1.7	W
Maximum Junction Temperature	—	-40 to + 150	°C
Thermal Resistance, Junction-to-Ambient Plastic Package 32 SOIC fine pitch, Case 1324	$R_{\theta JA}$ $R_{\theta JL}$	74 25	°C/W

Notes:

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
4. All pins when tested individually.
5. ESD2 testing is performed in accordance with the Machine Model (C_{Zap} = 200 pF, R_{Zap} = 0 Ω).
6. Maximum power dissipation at T_J =150° C junction temperature with no heat sink used.

STATIC ELECTRICAL CHARACTERISTICS

(Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Units
Power Input					
Supply Voltage Range Quasi-Functional (Note 7) Fully Operational	 $V_{PWR(QF)}$ $V_{PWR(QF)}$ $V_{PWR(FO)}$	 5.5 26 8.0	 — — —	 8.0 40 26	V
Supply Current (All Switches Open, Normal Mode, Tri-state Disabled)	$I_{PWR(ON)}$	—	2	4	mA
Sleep State Supply Current (Scan Timer = 64 mS, Switches Open)	$I_{PWR(SS)}$	40	70	100	µA
Logic Supply Voltage	V_{DD}	3.1	—	5.25	V
Logic Supply Current (All Switches Open, Normal Mode)	I_{DD}	—	0.25	0.5	mA
Sleep State Logic Supply Current (Scan Timer = 64 mS, Switches Open)	$I_{DD(SS)}$	—	10	20	µA
Switch Input					
Pulse Wetting Current Switch to Battery (current sink)	I_{PULSE}	12	15	18	mA
Pulse Wetting Current Switch to Ground (current source)	I_{PULSE}	12	16	18	mA
Sustain Current Switch to Battery Input (current sink)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Switch to Ground Input (current source)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Matching Between Channels Switch to Ground Inputs $\frac{(MaxIsustain - MinIsustain)}{MinIsustain} \times 100$	I_{MATCH}	—	2.0	4	%
Input Offset Current when Selected as Analog	I_{OFFSET}	-2	1.4	2	µA
Input Offset Voltage when Selected as Analog ($V_{(SP\&SG\ inputs)}$ to AMUX output)	V_{OFFSET}	-10	2.5	10	mV
Analog Operational Amplifier Output Voltage (sink 250 µA)	V_{OL}	—	10	30	mV
Analog Operational Amplifier Output Voltage (source 250 µA)	V_{OH}	V_{DD} - 0.1	—	—	V
Switch Detection Threshold	V_{TH}	3.70	4.0	4.3	V
Switch Input Voltage Range	V_{IN}	-14	—	40	V
Global Over Temperature Monitor (Note 8) (Note 9)	T_{LIM}	155	—	185	°C
Over Temperature Shutdown Hysteresis (Note 9)	$T_{LIM(HYS)}$	5	10	15	°C

Notes:

7. Device operational; Table parameters may be out of specification. Junction temperature for V_{PWR} greater than 26 must be considered.
8. Thermal shutdown of 16 mA pull-up and pull down current source only, 2 mA current source/sink and all other functions remain active.
9. This parameter is guaranteed by design, but not production tested.

STATIC ELECTRICAL CHARACTERISTICS

(Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Units
DIGITAL INTERFACE					
Input Logic Voltage Thresholds (Note 10)	$V_{INLOGIC}$	0.8	—	2.2	V
SCLK, SI, Tri-state SO Input Current (0 V to V_{DD})	$I_{SCK,SI,TriSO}$	-10	—	10	µA
$\overline{CS}$ Input Current ($\overline{CS}$ = V_{DD})	I_{ICS}	-10	—	10	µA
$\overline{CS}$ Pull-Up Current ($\overline{CS}$ = 0 V)	I_{ICS}	30	—	100	µA
SO High State Output Voltage ($I_{SO-high}$ = -200 ∝A)	$V_{SO(HIGH)}$	V_{DD} – 0.8	—	V_{DD}	V
SO Low State Output Voltage ($I_{SO-high}$ = 1.6 mA)	$V_{SO(LOW)}$	—	—	0.4	V
Input Capacitance on SCLK, SI, Tri-state SO (Note 11)	C_{IN}	—	—	20	pF
$\overline{INT}$ Internal Pull-Up Current	—	20	40	100	µA
$\overline{INT}$ Voltage ($\overline{INT}$ = Open Circuit)	$V_{\overline{INT}(HIGH)}$	V_{DD} – 0.2	—	V_{DD}	V
$\overline{INT}$ Voltage (I_{INT_B} = 1 mA)	$V_{\overline{INT}(LOW)}$	—	0.2	0.4	V
$\overline{WAKE}$ Internal Pull-Up Current	—	20	40	100	µA
$\overline{WAKE}$ Voltage ($\overline{WAKE}$ = Open Circuit)	$V_{\overline{WAKE}(HIGH)}$	4.0	4.3	5.2	V
$\overline{WAKE}$ Voltage ($I_{\overline{WAKE}}$ = 1mA)	$V_{\overline{WAKE}(LOW)}$	—	0.2	0.4	V
$\overline{WAKE}$ Voltage (External Pull-Up)	—	—	—	40	V

Notes:

10. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, and SCLK.
11. This parameter is guaranteed by design, but it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

(Characteristics noted under conditions of 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Units
SWITCH INPUT					
Pulse Wetting Current Time	$t_{PULSE(ON)}$	15	16	20	ms
Interrupt Delay Time (Normal Mode)	$t_{INT-DLY}$	—	5.0	16	µs
Sleep Mode Switch Read Time	t_{READ}	100	200	300	µs
Programmable Scan Timer (Sleep mode)	$t_{SCAN\ TIMER}$	0	—	64	ms
Programmable Interrupt Timer (Sleep mode)	$t_{INT\ TIMER}$	0.032	—	4	s
DIGITAL INTERFACE TIMING (Note 12)					
Required Low State Duration on V_{PWR} for Reset (V_{PWR} ≤ 0.2 V) (Note 12)	t_{RESET}	—	—	10	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	t_{LEAD}	100	—	—	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)	t_{LAG}	50	—	—	ns
SI to Falling Edge of SCLK (Required Setup Time)	$t_{SI(SU)}$	16	—	—	ns
Falling Edge of SCLK to SI (Required Hold Time)	$t_{SI(HOLD)}$	20	—	—	ns
SI, $\overline{CS}$, SCLK Signal Rise Time (Note 13)	$t_{r(SI)}$	—	5	—	ns
SI, $\overline{CS}$, SCLK Signal Fall Time (Note 13)	$t_{f(SI)}$	—	5	—	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 14)	$t_{SO(EN)}$	—	—	55	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 15)	$t_{SO(DIS)}$	—	—	55	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 16)	t_{VALID}	—	25	55	ns

12. This parameter is guaranteed by design. Production test equipment uses 4.16 MHz, 5.0V SPI interface.
13. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
14. Time required for valid output status data to be available on SO pin.
15. Time required for output states data to be terminated at SO pin.
16. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

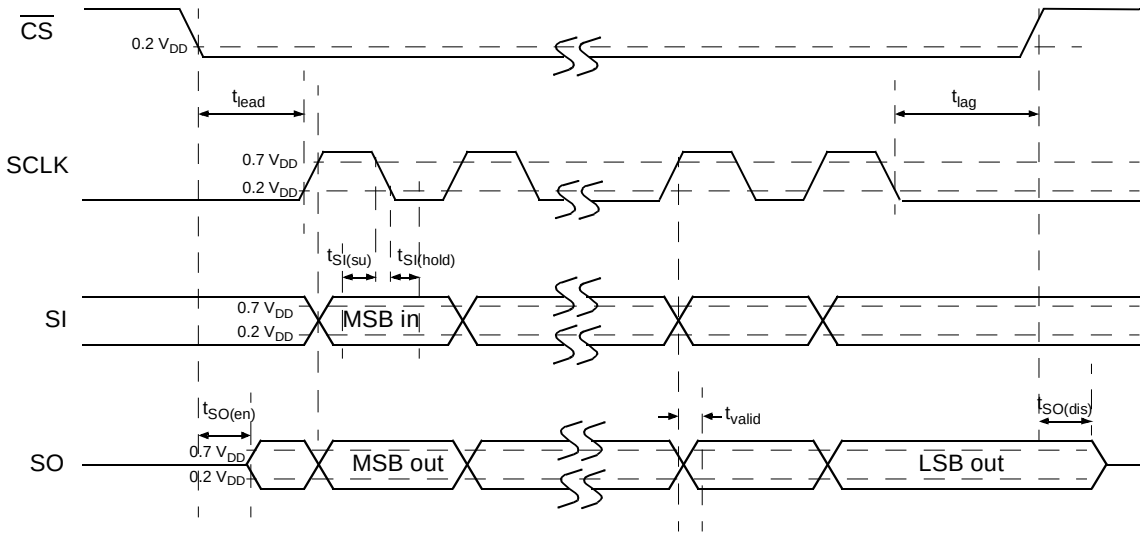


Figure 4. Input Timing Switching Characteristics

PIN FUNCTIONAL DESCRIPTION

$\overline{CS}$ Pin

The system MCU selects the 33993 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ in a logic low state, command words may be sent to the 33993 via SI pin and switch status information can be received by the MCU via SO. The falling edge of $\overline{CS}$ enables the SO output, latches the state of the $\overline{INT}$ pin, and the state of the external switch inputs.

Rising edge of $\overline{CS}$ initiates the following operation:

1. Disables the SO driver (high impedance)
2. $\overline{INT}$ pin is reset to logic [1], except when additional switch changes occur during $\overline{CS}$ low. See Figure 11
3. Activates the received command word, allowing the 33993 to act upon new data from switch inputs

To avoid any spurious data, it is essential the high-to-low and low-to-high transition of the $\overline{CS}$ signal occur only when SCLK is in a logic low state. Internal to the 33993 device is an active pull-up to V_{DD} on $\overline{CS}$.

In Sleep mode the negative edge of $\overline{CS}$ (V_{DD} applied) will wake up the 33993 device. Data received from the device during $\overline{CS}$ wake up may not be accurate.

SCLK Pin

The system clock pin (SCLK) clocks the internal shift register of the 33993. The serial input (SI) data is latched into the input shift register on the falling edge of SCLK signal. The serial output (SO) pin shifts the switch status bits out on the rising edge of SCLK. The SO data is available for the MCU to read on the falling edge of SCLK. False clocking of the shift register must be avoided to guarantee validity of data. It is essential the SCLK pin be in a logic low state whenever chip select pin $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin is commanded to a low logic state as long as the device is not accessed and $\overline{CS}$ is in a logic high state. When the $\overline{CS}$ is in a logic high state, any signal on the SCLK and SI pin will be ignored and the SO pin is tri-stated, that is, in high impedance.

SI Pin

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of SCLK. A logic high state present on SI will program a *one* in the command word on the rising edge of the $\overline{CS}$ signal. To program a complete word, 24 bits of information must be entered into the device.

SO Pin

The serial output (SO) pin is the output from the shift register. The SO pin remains tri-stated until the $\overline{CS}$ pin transitions to a logic low state. All *open switches* are reported as *zero*, all *closed switches* are reported as *one*. The negative transition of $\overline{CS}$ enables the SO driver.

The first positive transition of SCLK will make the status data bit 24 available on the SO pin. Each successive positive clock will make the next status data bit available for the MCU to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in-first-out protocol with both input and output words transferring the most significant bit (MSB) first.

$\overline{INT}$ Pin

The $\overline{INT}$ pin is an interrupt output from the 33993 device. The $\overline{INT}$ pin is an open drain output with an internal pull-up to V_{DD}. In the Normal mode, a switch state change will trigger the $\overline{INT}$ pin (when enabled). The $\overline{INT}$ pin and INT bit in the SPI register are latched on the falling edge of $\overline{CS}$. This permits the MCU to determine the origin of the interrupt. When two 33993 devices are used, only the device initiating the interrupt will have the $\overline{INT}$ bit set. The $\overline{INT}$ pin is cleared on the rising edge of $\overline{CS}$. The $\overline{INT}$ pin will not clear with rising edge of $\overline{CS}$ if a switch contact change has occurred while $\overline{CS}$ was low.

In a multiple 33993 device system with $\overline{WAKE}$ high and V_{DD} on (Sleep mode), the falling edge of $\overline{INT}$ will place all 33993s in the Normal mode.

$\overline{WAKE}$ Pin

The $\overline{WAKE}$ pin is an open drain output designed to control a power supply enable pin. In the Normal mode, the $\overline{WAKE}$ pin shall be low. In the Sleep mode, the $\overline{WAKE}$ pin shall be high. The $\overline{WAKE}$ pin has a pull-up to the internal +5.0 V supply.

In Sleep mode $\overline{WAKE}$ will be high. The falling edge of $\overline{WAKE}$ will place the 33993 in Normal mode. In Sleep mode, if V_{DD} is applied , $\overline{INT}$ must be high for negative edge of $\overline{WAKE}$ to wake up the device. If V_{DD} is not applied to the device in Sleep mode, $\overline{INT}$ does not affect $\overline{WAKE}$ operation.

V_{PWR} Pin

V_{PWR} pin is battery input and power-on reset to the 33993 IC. The V_{PWR} pin requires external reverse battery and transient protection. Maximum input voltage on V_{PWR} is 50 Vs. All wetting, sustain, and internal logic current is provided from V_{PWR} pin.

V_{DD} Pin

The V_{DD} input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from V_{DD} is used to drive SO output and the pull-up current for $\overline{CS}$ and $\overline{INT}$ pins.V_{DD} must be applied for wake up from negative edge of CS or INT.

GND Pin

The GND pin provides ground for the IC as well as ground for inputs programmed as switch to battery inputs.

SP0 – SP7 Pins

The 33993 device has 8-switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. Transient battery voltages greater than 40 Vs must be clamped by an external device. Surface mount 0805 MOV and transient voltage suppressors (TVS) devices are available in SOT23 packages. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 Vs are considered closed. Voltages less than 4.0 Vs are considered open. The opposite holds true when inputs are programmed as switch-to-ground. Programming features are defined in Table 13. Programming methods are provided in the following section.

SG0 – SG13 Pins

The SGx pins are switch-to-ground inputs only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 Vs are considered closed. Programming features are defined in Table 13. Programming methods are provided in the following section.

SYSTEM APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

Introduction

The 33993 device is an integrated circuit designed to provide systems with ultra low quiescent sleep/wake up modes and a robust interface between switch contacts and a microprocessor. The 33993 replaces many of the discrete components required when interfacing to microprocessors based systems while providing switch ground offset protection, contact wetting current and system wake up.

The 33993 features eight-programmable switch-to-ground or switch-to-battery inputs and 14-switch-to-ground inputs. All switch inputs may be read as analog inputs through the analog multiplexer. Other features include a programmable wake up timer, programmable interrupt timer, programmable wake up/ interrupt bits, and programmable wetting current settings.

This device is designed primarily for automotive but may be used in a variety of other applications in computer, telecommunications, and industrial controls.

The following sections describe the microprocessor interface, programming modes and features of the 33993.

Microprocessor Interface

The 33993 device directly interfaces to 3.3 or 5.0 V micro controller unit (MCU). SPI serial clock frequencies up to 6 MHz may be used for programming and reading switch input status (production tested at 4.16 MHz). Figure 5 illustrates the configuration between an MCU and one 33993.

Serial Peripheral Interface (SPI) data is sent to the 33993 device through the SI input pin. As data is being clocked into the SI pin, status information is being clocked out of the device by the SO output pin. The response to a SPI command will always return the switch status, interrupt flag and thermal flag. Input switch states are latched into the SO register on the falling edge of chip select. To complete a transfer of information between the 33993 and MCU, 24 bits are required.

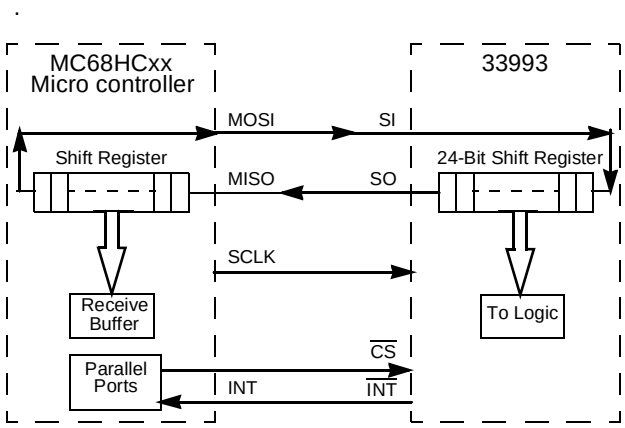


Figure 5. SPI Interface with Microprocessor

Two or more 33993 devices may be used in a module system. Multiple IC's may be SPI configured in parallel or serial. Figures 6 and 7 show the configurations. When using the serial configuration, 48-clock cycles are required to transfer data in/ out of the IC's.

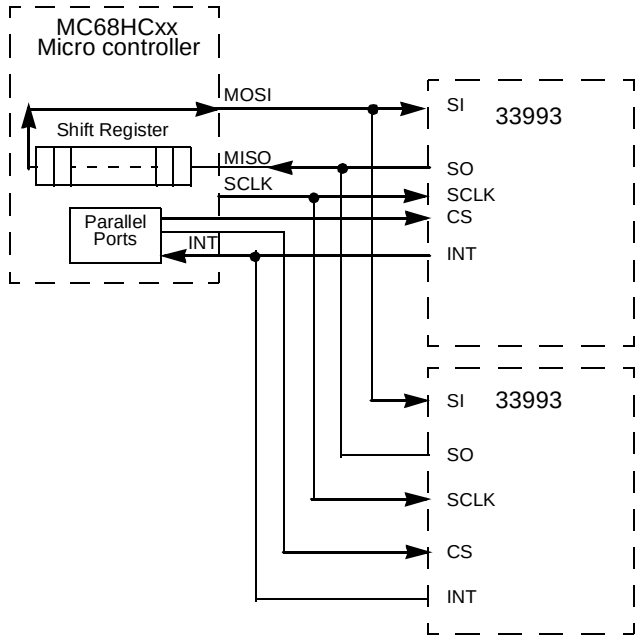


Figure 6. SPI Parallel Interface with Microprocessor

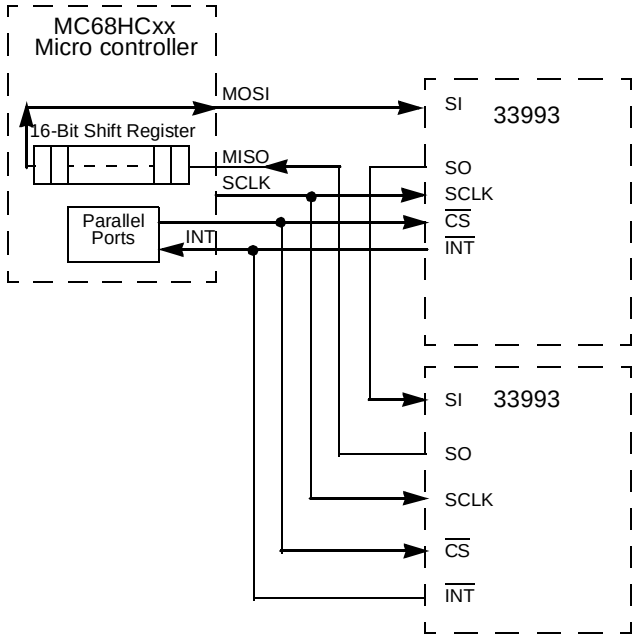


Figure 7. SPI Serial Interface with Microprocessor

FUNCTIONAL DESCRIPTION

Power Supply

The 33993 is designed to operate from 5.5 to 40 Vs on the V_{PWR} pin. Characteristics are provided from 8.0 to 16 Vs for the device. Switch contact currents and the internal logic supply are generated from the V_{PWR} pin. The V_{DD} supply pin is used to set the SPI communication voltage levels, current source for the SO driver and pull up current on $\overline{INT}$ and $\overline{CS}$.

V_{DD} supply may be removed from the device to reduce quiescent current. If V_{DD} is removed while device is in NORMAL mode, the device will remain in NORMAL mode. If V_{DD} is removed in SLEEP mode the device will remain in SLEEP mode until wake up input is received ($\overline{WAKE}$ high to low, switch input or interrupt timer expires).

Removing V_{DD} from the device disables SPI communication and will not allow the device to wake up from $\overline{INT}$ and $\overline{CS}$ pins.

Power On Reset (POR)

Applying V_{PWR} to the device will cause a Power On Reset and place the device in NORMAL mode.

Default settings from power on reset via V_{PWR} or Reset Command are:

- Programmable Switch – Set to Switch to Battery
- All Inputs Set as Wake Up
- Wetting Current - Set to 16 mA
- Wetting Current Timer On (20 ms)
- All Inputs Tri-state
- Analog Select *00000* (no input channel selected)

Modes of Operation

The 33993 has two operating modes: NORMAL and SLEEP modes.

Normal Mode

Normal mode may be entered by the following events:

- Application of V_{PWR} to the IC
- Change of Switch State (when enabled)
- Falling Edge of $\overline{WAKE}$
- Falling Edge of $\overline{INT}$ (with V_{DD} = 5.0 & $\overline{WAKE}$ at logic [1])
- Falling Edge of $\overline{CS}$ (with V_{DD} = 5.0V)
- Interrupt Timer Expires

Only in Normal mode with V_{DD} applied can the registers of the 33993 be programmed through the SPI.

Registers capable of being programmed in Normal mode are:

- Programmable Switch Register (*settings command*).
- Wake up/Interrupt Register (*wake up/interrupt command*)
- Wetting Current Register (*metallic command*)
- Wetting Current Timer Register (*wetting current timer enable command*)
- Tri-state Register (*tri-state command*)
- Analog Select Register (*analog command*)
- Calibration of Timers (*calibration command*)
- Reset (*reset command*)

Figure 11 is a graphical description of the device operation in Normal mode. Switch states are latched into the input register on the falling edge of $\overline{CS}$. The $\overline{INT}$ to the MCU is cleared on the rising edge of $\overline{CS}$. However, $\overline{INT}$ will not clear on rising edge of $\overline{CS}$ if a switch has closed during SPI communication ($\overline{CS}$ low). This prevents switch states from being missed by the MCU.

Programmable Switch Register

Inputs SP0 to SP7 may be programmable for Switch to Battery or Switch to Ground. These inputs types are defined using the *settings command*. To set an SPx input for switch to battery, a logic [1] for the appropriate bit must be set. To set an SPx input for switch to ground a logic [0] for the appropriate bit must be set. The MCU may change or update the *settings register* via software at any time in Normal mode. Regardless of the setting, when the SPx input switch is closed a logic [1] will be placed in the SO output register.

Table 1. Settings Command

Settings Command								Not used								Batt/GND Select							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0

Wake up/Interrupt Register: The *Wake up/Interrupt register* defines the inputs allowed to wake the 33993 from Sleep mode or set the $\overline{INT}$ pin low in Normal mode. Programming the Wake up/Interrupt bit to logic [0] disables the specific input from generating an interrupt and will disable the specific input from waking the IC in Sleep mode. Programming the Wake up/Interrupt bit to logic [1] enables the specific input to generate an interrupt with switch change of state and will enable the specific input as wake up. The MCU may change or update the *wake up/Interrupt register* via software at any time in Normal mode.

Table 2. Wake up/Interrupt Command

Wake up/Interrupt Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Wetting Current Register

The 33993 has two levels of switch contact current, 16 mA and 2 mA. The *metallic command* is used to set the switch contact current level. Programming the metallic bit to logic [0] will set the switch wetting current to 2 mA. Programming the metallic bit to logic [1] will set the switch contact wetting current to 16 mA. The MCU may change or update the *metallic register* via software at any time in Normal mode Wetting current is designed to provide higher levels of current during switch closure. The higher level of current is designed to keep switch contacts from building up oxides that form on the switch contact surface.

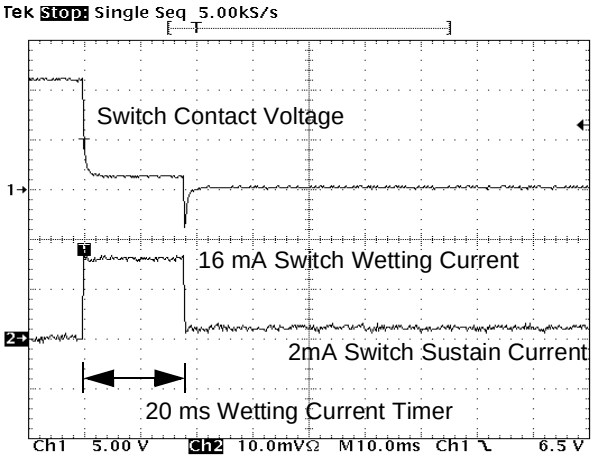


Figure 8. Contact Wetting and Sustain Current

Table 3. Metallic Command

Metallic Command								Command Bits													
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Wetting Current Timer Register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparatorthreshold (4.0 V). When the 20 ms timer expires the contact current is reduced from 16 mA to 2 mA. The wetting current timer may be disabled for a specific input. When the timer is disabled, 16 mA of current will continue to flow through the closed switch contact. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the *wetting current timer register* via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the wetting current timer bit to logic [0] will disable the wetting current timer. Programming the wetting current timer bit to logic [1] will enable the wetting current timer.

Table 4. Wetting Current Timer Command

Wetting Current Timer Commands								Command Bits													
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	0	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Tri-state Register

The *tri-state command* is use to set the SPx or SGx input node as high impedance. By setting the *tri-state register* bit to logic [1] the input will be high impedance regardless of the metallic command setting. The comparator on each input remains active. This command allows the use of each input as a comparator with a 4.0 volt threshold. The MCU may change or update the *tri-state register* via software at any time in Normal mode.

Table 5. Tri-State Command

Tri-State Commands								Command Bits													
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	1	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

Analog Select Register

The analog voltage ON switch inputs may be read by the MCU using the *analog command*. Internal to the IC is a 22 to 1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. When selecting a channel to be read as analog, the desired current (16 mA, 2 mA or high impedance) must also be set. Setting bit 5 and bit 6 to [0,0] selects the input as high impedence. Setting bit 5 and bit 6 to [0,1] selects the input as 2mA. Setting the bits to [1,0] selects the input as 16 mA. Setting bit 5 and bit 6 to logic [1,1] in the *analog select register* is not allowed and will set the input as an analog input with high impedance. Analog currents set by the *analog command* are pull up currents for all SGx and SPx inputs. The *analog command* does not allow pull down currents on the SPx inputs. Setting the current to 16 mA or 2 mA may be useful for reading sensor inputs. Further information is provided in the Application Notes in this Data Sheet.The MCU may change or update the *analog select register* via software at any time in Normal mode.

Table 6. Analog Command

Analog Command								Not used								Current Select		Input Select				
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16 ma	2 ma	0	0	0	0	0

Table 7. Analog Channel Select

Bit 43210	Analog Channel Select
00000	No Input Selected
00001	SG0
00010	SG1
00011	SG2
00100	SG3
00101	SG4
00110	SG5
00111	SG6
01000	SG7
01001	SG8
01010	SG9
01011	SG10
01100	SG11
01101	SG12
01110	SG13
01111	SP0
10000	SP1
10001	SP2
10010	SP3
10011	SP4
10100	SP5
10101	SP6
10110	SP7

Calibration of Timers

In cases where an accurate time base is required to minimize quiescent current, the user may calibrate the internal timers using the *calibration command.* The device is calibrated by sending the *calibration command*. After the 33993 device receives the calibration command the device will wait for a 512 µs logic [0] pulse on the CS pin. The pulse is used to calibrate the internal clock. No other SPI pins should transition during this 512 µs calibration pulse. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. The *calibration command* may be used to update the device on a periodic basis.

Table 8. Calibration Command

Calibration Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Reset

The reset command resets all registers to Power On Reset (POR) state. See Table 4 for POR states or POR in this section of the Data Sheet.

Table 9. Reset Command

Reset Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Normal Mode Operation

The operation of the device in Normal mode is defined by the states of the previously discussed registers. A typical application may have the following settings:

- Programmable Switch – Set to Switch to Ground
- All Inputs Set as Wake Up
- Wetting Current - Set to 16 mA
- Wetting Current Timer On (20 ms)
- All inputs Tri-state-disabled (comparator is active)
- Analog select *00000* (no input channel selected)

With the device programmed as above an interrupt will be generated with each switch contact change of state (open to close or close to open) and 16 mA of contact wetting current will be source for 20 ms. The $\overline{INT}$ pin will remain low until switch status is acknowledged by the microprocessor. It is critical to understand $\overline{INT}$ will not be cleared on the rising edge of $\overline{CS}$ if a switch closure occurs while $\overline{CS}$ is low. The maximum duration a switch state change can exist without acknowledgement depends on the software response time to the interrupt. Figure 9 provides further information.

If desired the user may disable interrupts (*wake up/interrupt command*) from the 33993 device and read the switch states on a periodic basis. Switch activation and deactivation faster than the MCU read rate will not be acknowledged.

The 33993 device will exit the Normal mode and enter the Sleep mode only with a valid sleep command.

Sleep Mode Operation

Sleep mode is used to reduce system quiescent currents. Sleep mode may be entered only by sending the *sleep command.* All register settings programmed in Normal mode will be maintained in Sleep mode.

The 33993 will exit Sleep mode and enter Normal mode due to any of the following events:

- Input Switch Change of State (when enabled)
- Interrupt Timer Expire
- Falling Edge of $\overline{WAKE}$
- Falling Edge of $\overline{INT}$ (with V_{DD} = 5.0 & $\overline{WAKE}$ at logic [1])
- Falling Edge of $\overline{CS}$ (with V_{DD} = 5.0V)
- Power On Reset (POR)

The V_{DD} supply may be removed from the device during Sleep mode. However removing V_{DD} from the device in Sleep mode will disable a wake up from Falling Edge of $\overline{INT}$ and $\overline{CS}$.

Note: In cases where $\overline{CS}$ is used to wake the device, the first SO data message is not valid.

The sleep command contains settings for two programmable timers for Sleep mode (Interrupt timer, Scan timer).

Table 10. Sleep Command

Sleep Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer

The interrupt timer is used as a periodic wake up timer. When the timer expires an interrupt is generated and the device enters Normal mode. The interrupt timer is a fail-safe timer designed to guarantee module wake up.

The scan timer sets the polling period of switch inputs during Sleep mode. For example: In Sleep mode with scan timer set to 32 ms the 33993 will wake up every 32 ms for 125 µs and read switch status.

The table below illustrates the programmable settings of the Interrupt timer.

Table 11. Interrupt Timer

Bit 543	Interrupt Period
000	32 ms
001	64 ms
010	128 ms
011	256 ms
100	512 ms
101	1.024s
110	2.048s
111	4.096s

The table below illustrates the programmable settings of the Scan timer.

Table 12. Scan Timer

Bit 210	SCAN Period
000	No Scan
001	1 ms
010	2 ms
011	4 ms
100	8 ms
101	16 ms
110	32 ms
111	64 ms

The scan timer sets the polling period between input switch reads in Sleep mode. The period is set in the sleep command and may be set to 000 (no period) to 111 (64 ms). In Sleep mode when the scan timer expires, inputs will behave as programmed prior to sleep command. The 33993 will wake up for approximately 125 µs and read the switch inputs. At the end of the 125 µs the input switch states are compared with the switch state prior to sleep command. When switch state changes are detected an interrupt (when enabled - see *Wake Up/Interrupt Command*) is generated and the device enters Normal mode. Without switch state changes, the 33993 will reset the scan timer, inputs become tri-state, and the Sleep mode continues until scan timer expires again.

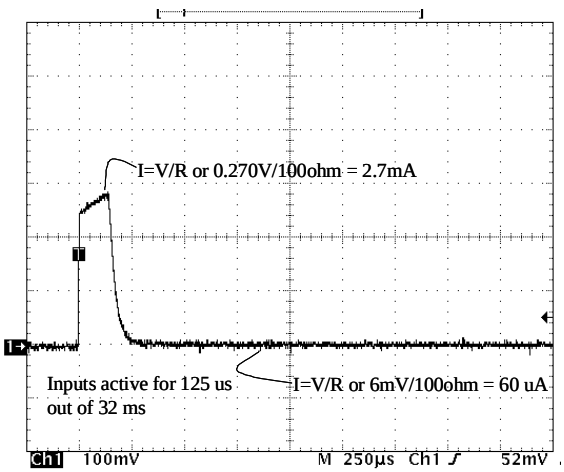


Figure 9. Sleep Current Waveform

It is critical to note the Interrupt and Scan timers are disabled in the Normal mode.

Figure 10 is a graphical description of how the 33993 device exits Sleep mode and enters Normal mode. Notice the device will exit Sleep mode when the interrupt timer expires or when a switch change of state occurs. The falling edge of $\overline{INT}$ triggers the MCU to wake from sleep state.

Over Temperature

With multiple switch inputs closed and the device programmed with the wetting current timer disabled, considerable power is dissipated by the IC. For this reason global temperature monitoring is implemented. Temperature monitor is active in the Normal mode only. When activated, Over Temperature monitor will:

- Force all 16 mA pull-up and pull down current sources to revert to 2mA current sources.
- Maintain the 2 mA current source and all other functionality
- Set the Over Temperature bit in the SPI output register

An interrupt will be generated when Over Temperature monitor has been detected. The Over Temperature bit in the SPI word will be cleared on rising edge of $\overline{CS}$ provided the die temperature has cooled below the specification limit. When die temperature has cooled below thermal limit the device will resume previously programmed settings.

Table 13 provides a comprehensive list of SPI commands recognize by the 33993 and the reset state of each register

Table 13. .SPI COMMAND REGISTER DEFAULT SETTINGS																									
	MSB Command Bits								Setting Bits																
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Status Command	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Settings command (SI) Bat=1,Gnd=0	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1
wake up/interrupt bit (default is wake up) wakeup=1, nonwakeup=0	0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1
wake up/interrupt bit (default is wake up) wakeup=1, nonwakeup=0	0	0	0	0	0	0	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Metallic command 1(SI) M = 1, N = 0	0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1
Metallic command 1(SI) M = 1, N = 0	0	0	0	0	0	1	0	1	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Analog command (SI)	0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16mA 0	2mA 0	0	0	0	0	0
Wetting Current Timer Enable Default = on on = 1, off = 0	0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1
Wetting Current Timer Enable Default = on on = 1, off = 0	0	0	0	0	1	0	0	0	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Tri-State Command Tri-State=1	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1
Tri-State Command Tri-State=1	0	0	0	0	1	0	1	0	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Calibration Command	0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Sleep command (SI)	0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer
Reset Command	0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Test Mode (SI)	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO response will always send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

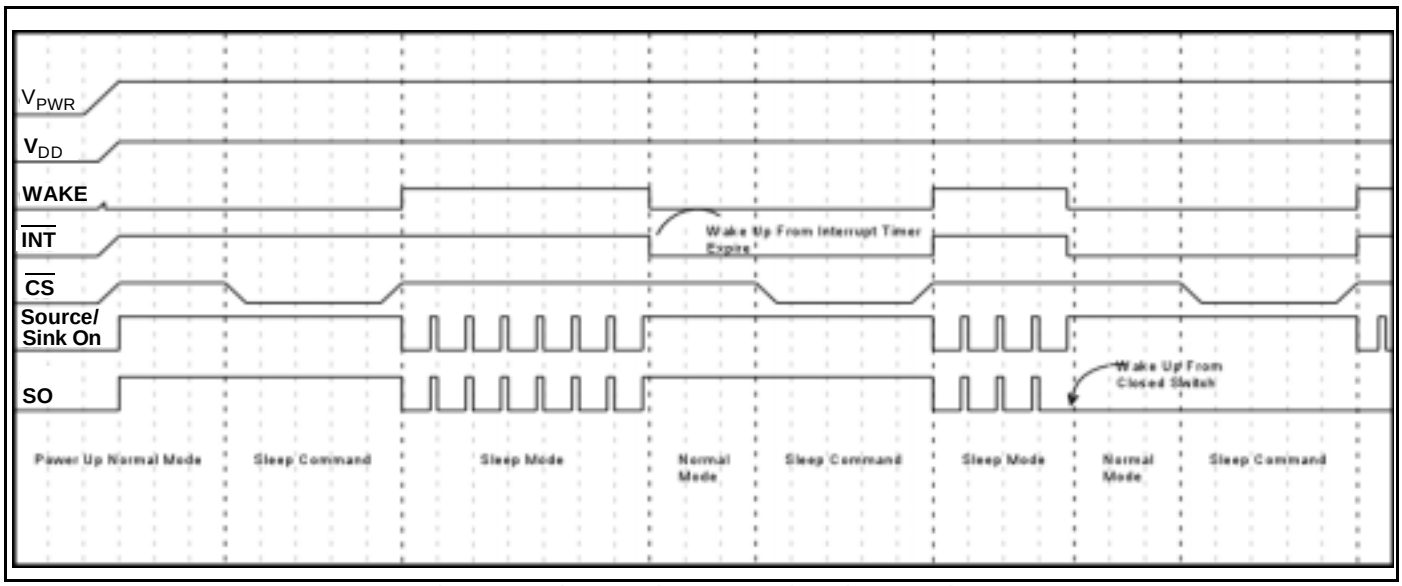


Figure 10. Sleep Mode to Normal Mode Operation

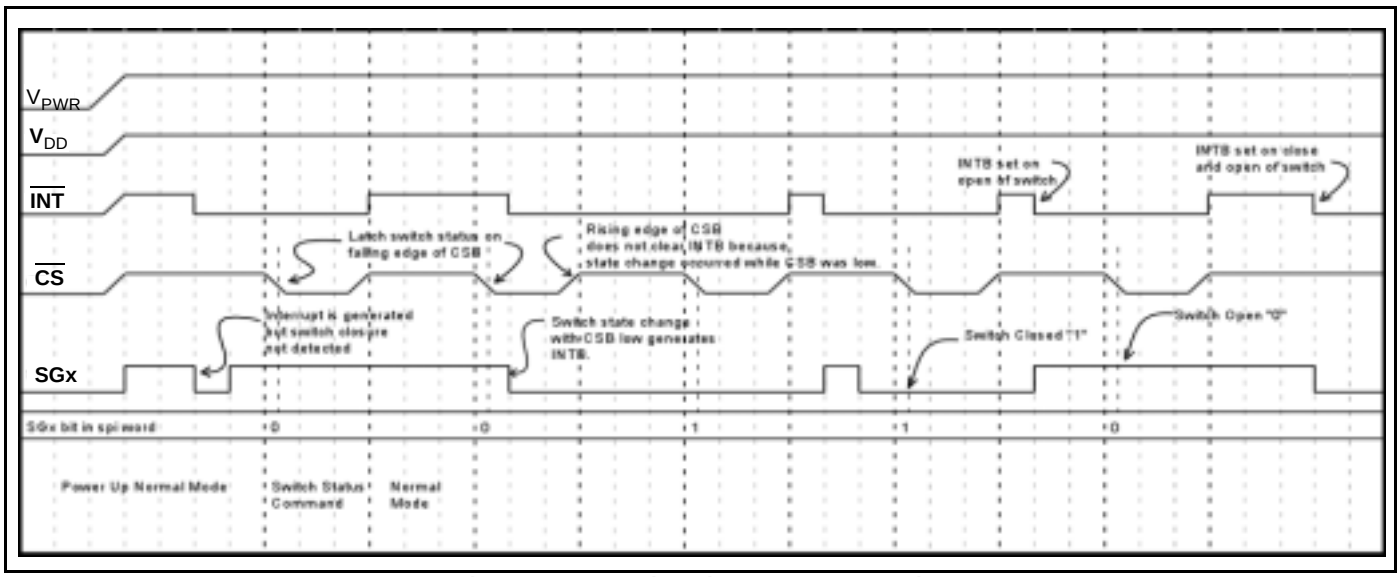


Figure 11. Normal Mode Interrupt Operation

APPLICATION NOTES

Introduction

The 33993 device primary function is the detection of open or closed switch contacts. However, there are many features allowing the device to be used in a variety of applications. The following list of applications should be considered for the IC:

- Sensor Power Supply
- Switch Monitor for Metallic or Elastomeric Switches
- Analog Sensor Inputs (ratio metric)
- Power Mosfet/LED Driver & Monitor
- Multiple 33993 Devices in Module System

Sensor Power Supply

Each input may be used to supply current to sensors external to a module. Many sensors such as hall effect, pressure sensors and temperature sensors require a supply voltage to power the sensor and provide an open collector or analog output. The diagram below shows how the 33993 may be used to supply power and interface to these types of sensors. In an application where the input makes continuous transitions, consider using the *wake up/interrupt command* to disable the interrupt for the particular input.

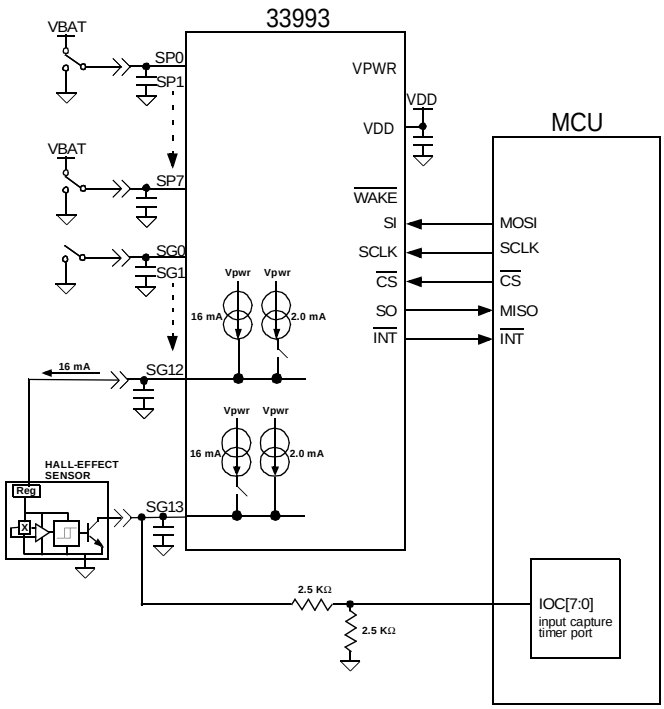


Figure 12. Sensor Power Supply

Metallic/Elastomeric Switch

Metallic switch contacts often develop higher contact resistance over time due to contact corrosion. The corrosion is induced by humidity, salt and other elements that exist in the environment. For this reason the 33993 provides two settings for contacts. When programmed for metallic switches the device provides higher wetting current to keep switch contacts free of oxides. The higher current occurs for the first 20 ms of closed switch. After the time period set by the MCU, the *wetting current timer command* may be sent again to enable the timer. The user must consider power dissipation on the device when disabling the timer (see Over Temperature Operation).

switch closure. Where longer duration of wetting current is desired, the user may send the *wetting current timer command* and disable the timer. Wetting current will be continuous to the To increase the amount of wetting current for a switch contact the user has two options. Higher wetting current to a switch may be achieved by paralleling SGx or SPx inputs. This will increase wetting current by 16 mA for each input added to the switch contact. The second option is to simply and an external resistor pull up to the V_{PWR} supply for switch to ground inputs or a resistor to ground for a switch to battery input. Adding an external resistor has no effect on the operation of the device.

Elastomeric switch contacts are made of carbon and have a high contact resistance. Resistance of 1K is common. Applications with elastomeric switches, the pull-up and pull down currents must be reduced to prevent excessive power dissipation at the contact. Programming for lower current settings is provided in the *Functional Description* section of this specification.

Analog Sensor Inputs

The 33993 features a 22 to 1 analog multiplexer. Setting the binary code for a specific input in the *analog command* allows the micro controller to perform analog to digital conversion on any of the 22 inputs. On rising edge of $\overline{CS}$ the multiplexer connects a requested input to the AMUX pin. The AMUX pin is clamped to max of V_{DD} Vs regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in next SO data stream will be logic [0].

The input pin, when selected as analog may be configured as analog with high impedance, analog with 2 mA pull up or analog with 16 mA pull up. The following diagram show how the 33993 may be used to provide a ratiometric reading of variable resistive input.

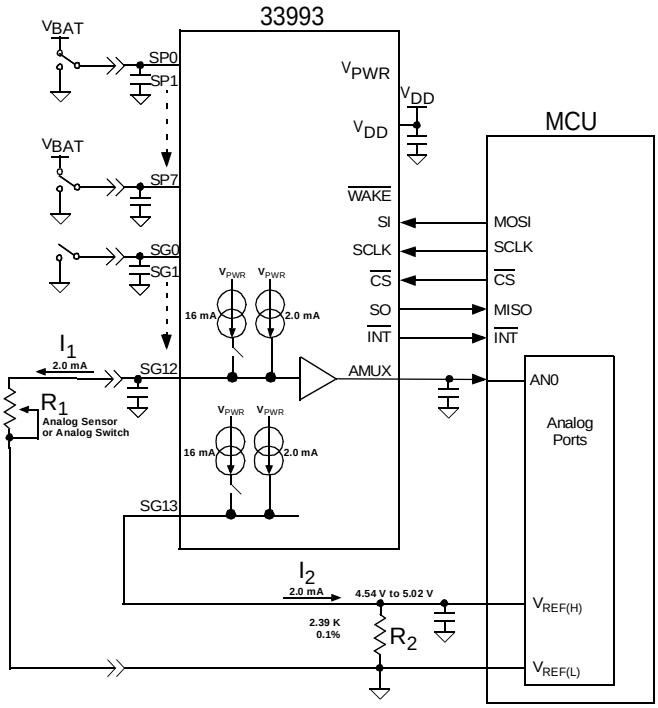


Figure 13. Analog Ratiometric Conversion

To read a potentiometer sensor, the wiper should be grounded and brought back to the module ground, illustrated in Figure 11. With the wiper changing the impedance of the sensor, the analog voltage on the input will represent the position of the sensor.

Using the Analog feature to provide 2 mA of pull-up current to an analog sensor may induce error due to the accuracy of the current source. For this reason, a ratiometric conversion must be considered. Using two current sources (one for the sensor and one to set the reference voltage to the A/D converter) will yield a maximum error (due to the 33993) of four percent.

Higher accuracy may be achieved through module level calibration. In this example we use the resistor values from Figure 11, and assume the current sources are four percent from each other. The user may use the module end of line tester to calculate the error in the A/D conversion. By placing a 2.0K, 0.1 percent resistor in the end of line test equipment and assuming a perfect 2.0 mA current source from the 33993 a calculated A/D conversion may be obtained. Using the equation yields

$$ADC = \frac{I1 \text{ Þ } R1}{I2 \text{ Þ } R2} \times 255$$

$$ADC = \frac{2mA \cdot 2K}{2mA \cdot 2.39K} \times 255$$

$$ADC = 213counts$$

The ADC value of 213 counts is the value with zero percent error (neglecting the resistor tolerance and AMUX input offset voltage). Now we can calculate the count value induced by the mismatch in current sources. From a sample device the maximum current source was measured at 2.05 mA and minimum current source was measured at 1.99 mA. This yields three percent error in A/D conversion. The A/D measurement will be as follows.

$$ADC = \frac{1.99mA \cdot 2K}{2.05mA \cdot 2.39K} \times 255$$

$$ADC = 207counts$$

This A/D conversion is three percent low in value. The error correction factor of 1.03 my be used to correct the value.

$$ADC = 207counts \cdot 1.03$$

$$ADC = 213counts$$

An error correction factor may then be stored in E^2 memory and used in the A/D calculation for the specific input. Each input used as analog measurement will have a dedicated calibrated error correction factor.

Power MOSFET/LED Driver & Monitor

Because of the flexible programming of the 33993 device, it may be used to drive small loads like LEDs or MOSFET gates. It was specifically designed to power up in the Normal mode with the inputs tri-state. This was done to insure the LEDs or MOSFETs connected to the 33993 power up in the off-state. The Switch Programmable (SP0-SP7) inputs have a source and sink capability, providing effective MOSFET gate control. To complete the circuit, a pull down resistor should be used to keep the gate from floating during the Sleep modes. An SGx input may be used to monitor the drain voltage for open load detection. An external resistor on the SGx input is used to adjust the comparator threshold in the mosfet ON state. The drain to source voltage may also be monitored using the *analog command* for the SGx input. See Figure 14 below.

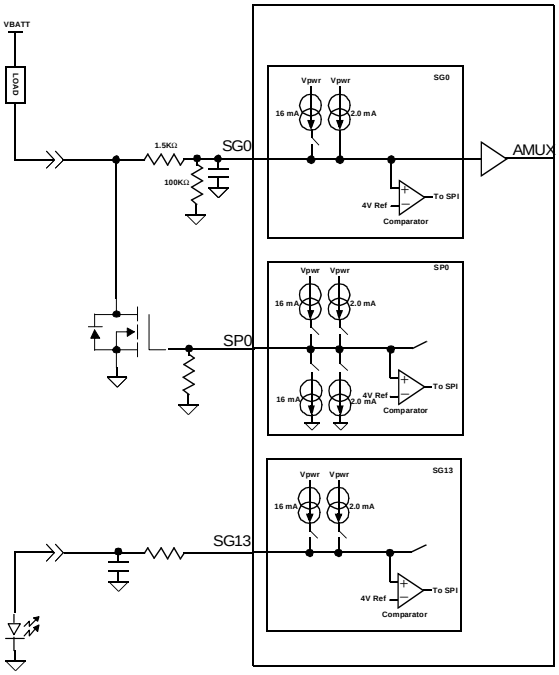


Figure 14. MOSFET or LED Driver Output

The sequence of commands (from Normal mode with inputs tri-state) required to set up the device to drive the gate are as follows:

- *Wetting current timer enable command* -disable SPx wetting current timer
- *Metallic command* -set SPx to 16 mA or 2 mA gate drive current
- *Settings command* - set SPx as switch to battery
- *Tri-state command* -disable tri-state for SPx

After the tri-state command is sent (tri-state disable) the MOSFET gate will be pulled to ground. From this point forward the MOSFET may be turned ON and OFF by sending the setting command.

- *Settings command* - SPx as switch to ground (MOSFET ON)
- *Settings command* - SPx as switch to battery (MOSFET OFF)

Monitoring of the MOSFET drain in the OFF state provides open load detection. This is done by using an SGx input comparator. With the SGx input in tri-state the load will pull-up the SGx input to battery. With open load the SGx pin is pulled down to ground through an external resistor. The open load is indicated by a logic [1] in the SO data bit.

The analog command may be used to monitor the drain voltage in the mosfet ON state. By sourcing 2 mA of current to the 1.5KΩ resistor the analog voltage on the SGx pin will be approximately

$$V\ sgx = Is\ (gx \bullet (1.5K + V\ ds))$$

As the voltage on the drain of the MOSFET increases, so does the voltage on the SGx pin. With the SGx pin selected as analog the MCU may perform the A/D conversion.

Using this method for controlling unclamped inductive loads is not recommended. Inductive flyback voltages greater than V_{PWR} may damage the IC.

The SP0 to SP7 pins of this device may also be used to send signals from one module to another. Operation is similar to the gate control of a MOSFET.

For LED applications a resistor in series with the LED is recommended but not required. The Switch to Ground inputs are recommended for LED application. To drive the LED use the following commands:

- *Wetting current timer enable command* -disable SGx wetting current timer
- *Metallic command* -set SGx to 16 mA

From this point forward the LED may be turned ON and OFF using the *tri-state command:*

- *Tri-state command* -disable tri-state for SGx (LED ON)
- *Tri-state command* -disable tri-state for SGx (LED OFF)

These parameters are easily programmed via SPI commands in Normal mode.

Multiple 33993 Devices in a Module System

Multiple 33993 devices may be used in a module system. SPI control may be achieved in parallel or serial. However, when Parallel mode is used each device is addressed independently. Therefore, when sending the *sleep command* one device will enter sleep before the other. For multiple devices in a system, it is recommended the devices are controlled in serial (S0 from first device is connected to SI of second device). With two devices, 48 clock pulses are required to shift data in. When the $\overline{\text{WAKE}}$ feature is used to enable the power supply, both $\overline{\text{WAKE}}$ pins should be connected to the enable pin on the power supply. The $\overline{\text{INT}}$ pins may be connected to one interrupt pin on the MCU or may have their own dedicated interrupt to the MCU.

The transition from Normal mode to Sleep mode is done by sending the *sleep command*. With the devices connected in serial and *sleep command* sent, both will enter Sleep mode on rising edge of CS. When Sleep mode is entered, the WAKE pin will be logic [1]. If either device wakes up the $\overline{\text{WAKE}}$ pin will transition low, waking the other device.

A condition exists where the MCU is sending the *sleep command* (CS logic [0]) and a switch input changes state. With this event the device detecting this input will not transition to Sleep mode while the second device will enter Sleep mode. In this case two *switch status commands* must be sent to receive accurate switch status data. The first *switch status command* will wake the device in Sleep mode. Switch status data may not be valid from the first *switch status command* because the time required for the input voltage to rise above the 4.0 V input comparator threshold. This time is dependant on the impedance of SG or SP node. The second *switch status command* will provide accurate switch status information. It is recommended for software to wait 10 to 20 ms between the two *switch status commands,* allowing time for switch input voltages to stabilize. With all switch states acknowledged by the MCU, the sleep sequence may be initiated. All parameters for Sleep mode should be updated prior to sending the *sleep command*.

The 33993 IC has an internal 5.0 V supply from V_{PWR} pin. A POR circuit monitors the internal 5.0 V supply. In the event of transients on the V_{PWR} pin an internal reset may occur. Upon reset the 33993 will enter Normal mode with the internal registers as defined in Table 13. Therefore, it is recommended the MCU periodically update all registers internal to the IC.

Using the $\overline{\text{WAKE}}$ Feature

The 33993 provides a $\overline{\text{WAKE}}$ output designed to control an enable pin on system power supply. While in the Normal mode, the $\overline{\text{WAKE}}$ output is low, enabling the power supply. In the Sleep mode, the $\overline{\text{WAKE}}$ pin is high, disabling the power supply. The $\overline{\text{WAKE}}$ pin has a passive pull-up to the internal 5.0 V supply.

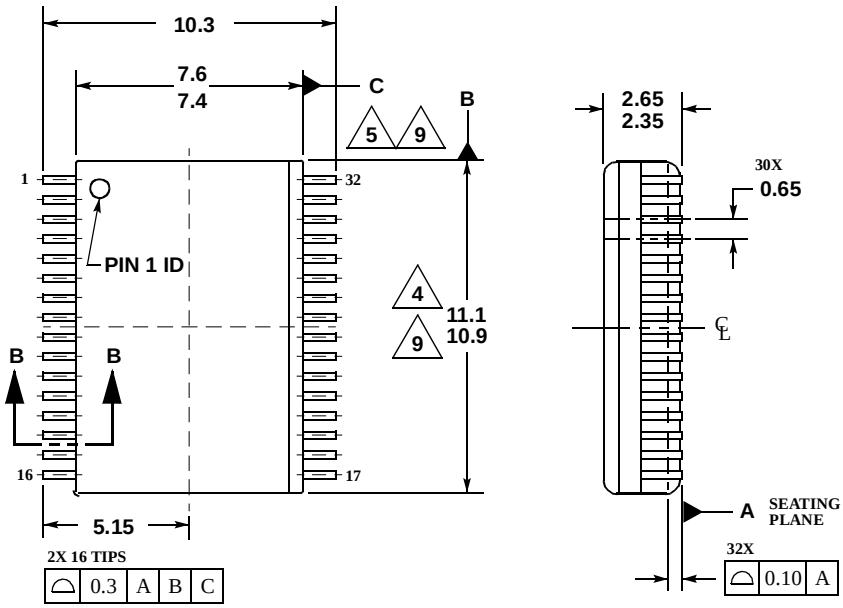
During the Sleep mode, a switch closure will set the $\overline{\text{WAKE}}$ pin low, causing the 33993 to enter the Normal mode. The power supply will then be activated, supplying power to the V_{DD} pin and the microprocessor and the 33993. The microprocessor can determine the source of the $\overline{\text{WAKE}}$ up by reading the interrupt flag.

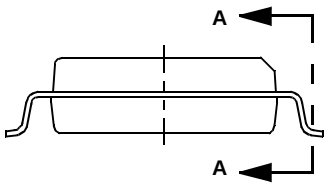
Cost and Flexibility

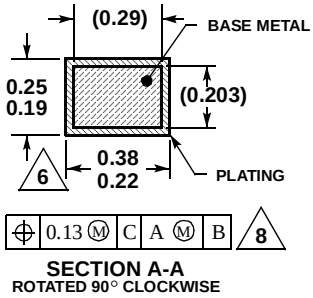
The bottom line relates to system cost. Systems requiring a significant number of switch interfaces have many discrete components. Discrete components on standard PWB consume board space and must be checked for solder joint integrity. An integrated approach reduces solder joints, consumes less board space, and offers wider operating voltage and greater flexibility. Another noteworthy advantage the 33993 device is it offers analog interface capability. High impedance analog circuits are susceptible to noise from other signals on the PWB. By implementing a short analog signal to the 33993 and allowing it to buffer the signal reduces the susceptibility. By implementing the analog method mentioned in the *Application* section, an accurate ratio metric conversion may be accomplished. The method also reduces system wiring and failure modes over conventional systems.

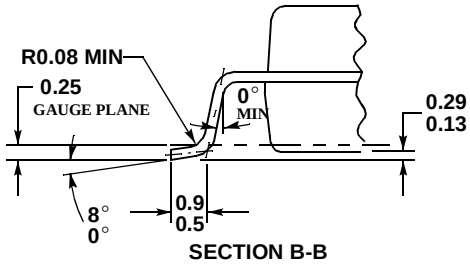
PACKAGE DIMENSIONS

32-Lead SOIC
0.65 mm Pitch
CASE 1324-02
Issue A









NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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