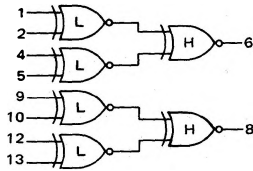


DUAL 4-BIT PARITY TREE

MC4300/MC4000 series

MC4010L, P *



VCC = PIN 14
GND = PIN 7

Positive Logic:

6 = 1 ⊕ 2 ⊕ 4 ⊕ 5

where $X \oplus Y = \bar{X} \cdot \bar{Y} + X \cdot Y$

Input Loading Factor = 2

Output Loading Factor = 10

Total Power Dissipation = 125 mW typ/pkg

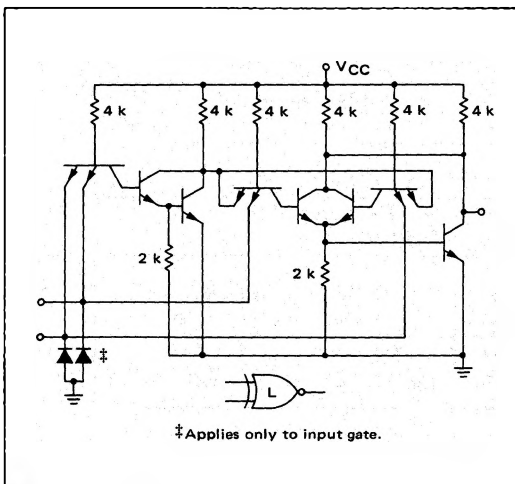
Propagation Delay Time = 9.5 to 22 ns typ

ADVANCE INFORMATION/NEW PRODUCT

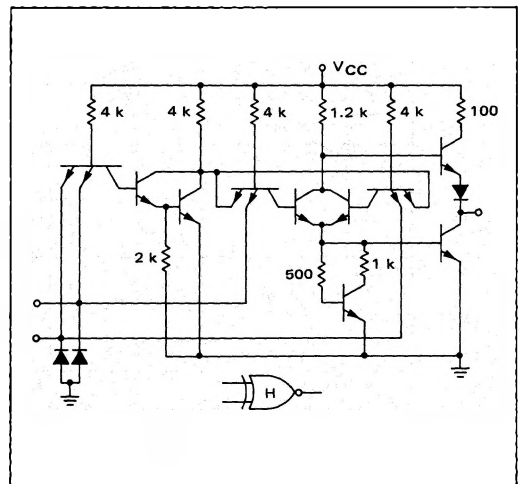
Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic "1" states on the inputs will result in a logic "1" output state. An odd parity checker can be made by connecting an inverter to the output of the device.

This function is constructed using low and high-level Exclusive NOR gates connected as shown in the logic diagram to maximize output drive capability and minimize power dissipation.

LOW-LEVEL GATE



HIGH-LEVEL GATE



* L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

MC4010L, P (continued)

INPUT and OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

($T_A = 0$ to 75°C)

Characteristic	Symbol	Value	Conditions
Input Forward Current	I_{F1}	-3.2 mA dc max	$V_{in} = 0.4$ Vdc, $V_{CC} = 5.25$ Vdc
	I_{F2}	-2.8 mA dc max	$V_{in} = 0.4$ Vdc, $V_{CC} = 4.75$ Vdc
Leakage Current	I_R	80 μ A dc max	$V_{in} = 2.5$ Vdc, $V_{CC} = 5.25$ Vdc
Breakdown Voltage	BV_{in}	5.5 Vdc max	$I_{in} = 1.0$ mA dc, $V_{CC} = 5.25$ Vdc, $T_A = 25^\circ\text{C}$
Clamp Voltage	V_D	-1.5 Vdc max	$I_D = -10$ mA dc, $V_{CC} = 4.75$ Vdc, $T_A = 25^\circ\text{C}$
Threshold Voltage	V_{th} "1"	2.0 Vdc 1.8 Vdc	$T_A = 0^\circ\text{C}$ $T_A = +25^\circ\text{C}$, or $T_A = +75^\circ\text{C}$
	V_{th} "0"	1.1 Vdc 0.9 Vdc	$T_A = 0^\circ\text{C}$, or $T_A = +25^\circ\text{C}$ $T_A = +75^\circ\text{C}$
Output Output Voltage	V_{OL}	0.4 Vdc max	$I_{OL} = 16$ mA dc, $V_{CC} = 4.75$ Vdc†
		0.4 Vdc max	$I_{OL} = 17.6$ mA dc, $V_{CC} = 5.25$ Vdc†
	V_{OH}	2.5 Vdc min	$I_{OH} = -1.6$ mA dc, $V_{CC} = 4.75$ Vdc†
Short-Circuit Current	I_{SC}	-20 to -65 mA dc	$V_{CC} = 5.0$ Vdc, output grounded†

† These tests are performed according to the logic equations with a true input equal to V_{th} "1" and a false input equal to V_{th} "0".