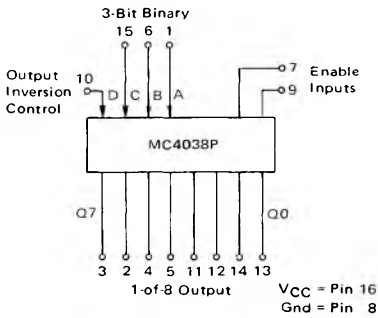


**INVERTING/NON-INVERTING
ONE-OF-EIGHT DECODER**

MC4300/MC4000 series

MC4038P*



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Total Power Dissipation = 240 mW typ/pkg

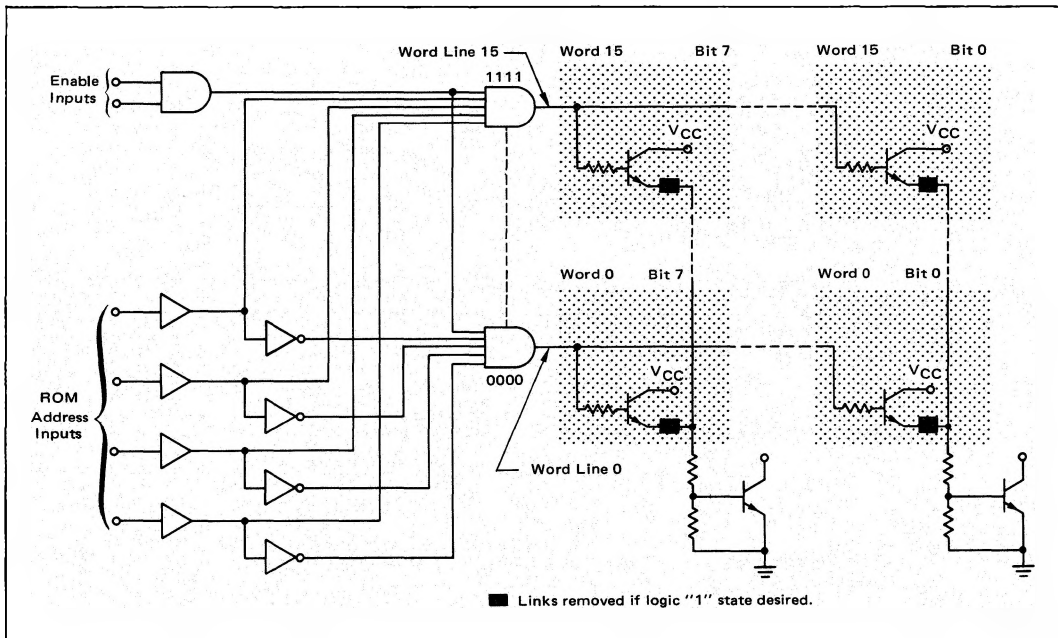
The MC4038P is derived from the XC170 128-Bit Read Only Memory. A 3-bit binary address selects the desired word for the 8-bit output. The inversion control, D, selects half of the memory chip with the bit pattern that defines a 1-of-8 decoder function. When D is a logic "0", the selected output is designated as a logic "0". A logic "1" on D produces a logic "1" on the selected output.

Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



*P suffix = 16-pin dual in-line plastic package (Case 612).

MC4038P (continued)

INPUT and OUTPUT LOADING FACTORS with respect to M TTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT LOADING FACTOR
MC4000	1.0	Open Collector $I_{OL} = 20 \text{ mA}$
MC400	1.0	
MC2000	0.67	
MC3000	0.7	
MC7400	1.0	
MC830	1.15**	

Note: Differences in MC4000 series loading factors result from differences in specifications for each family.

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Supply Operating Voltage Range	V_{CC}	4.5 to 5.5	Vdc
Input Voltage	V_{in}	-1.5 to +5.5	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS ($T_A = 0 \text{ to } +75^\circ\text{C}$)

Characteristic	Symbol	Min	Max	Unit
Address Input Forward Current ($V_A = 0, V_{CC} = 5.0 \text{ Vdc}$)	I_F	-	1.6	mAdc
Enable Input Forward Current ($V_E = 0, V_{CC} = 5.0 \text{ Vdc}$)	I_F	-	1.6	mAdc
Address Input Leakage Current ($V_A = 5.5 \text{ Vdc}, V_{CC} = 5.0 \text{ Vdc}$)	I_R	-	100	μAdc
Enable Input Leakage Current ($V_E = 5.5 \text{ Vdc}, V_{CC} = 5.0 \text{ Vdc}$)	I_R	-	100	μAdc
Logical "0" Output Voltage ($I_{OL} = 20 \text{ mAdc}, V_{IL} = 0.9 \text{ Vdc}, V_{IH} = 2.0 \text{ Vdc}, V_{CC} = 4.75 \text{ Vdc}$)	V_{OL}	-	0.45	Vdc
Logical "1" Output Leakage Current ($V_{IL} = 0.9 \text{ Vdc}, V_{IH} = 2.0 \text{ Vdc}, V_{CEX} = 7.0 \text{ Vdc}, V_{CC} = 5.25 \text{ Vdc}$)	I_{CEX}	-	100	μAdc
Power Supply Drain Current (Memory Enabled, $V_{CC} = 5.25 \text{ Vdc}$) (Memory Disabled, $V_{CC} = 5.25 \text{ Vdc}$)	$I_{PD \text{ max}}$ $I_{PD \text{ min}}$	-	73	mAdc

SWITCHING TIMES ($V_{CC} = 5.0 \text{ Vdc}$)

Positive Input Address to Positive Output	$I_{OL} = 10 \text{ mA}$ driving 30 pF	t++	-	45	ns
Negative Input Address to Negative Output		t--	-	45	ns
Positive Input Address or Enable to Negative Output		t+-	-	45	ns
Negative Input Address or Enable to Positive Output		t-+	-	45	ns