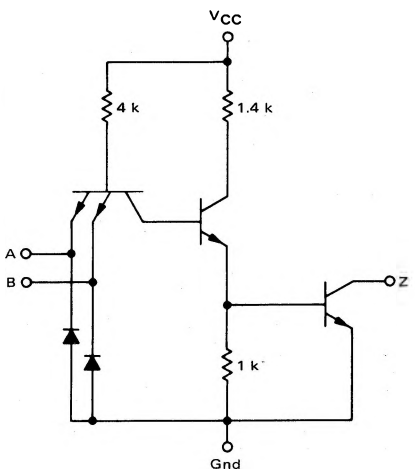
QUAD 2-INPUT "NAND" GATE
WITH OPEN COLLECTOR

MC5403 • MC7403

Add Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 607) MC7403 only.

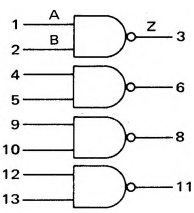
CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



V_{CC} = Pin 14
Gnd = Pin 7

Device available only in dual in-line package.

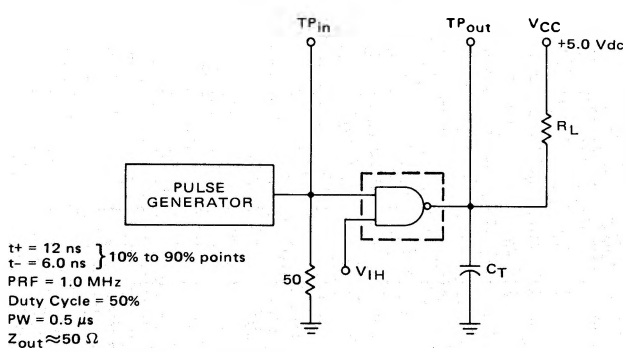
This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



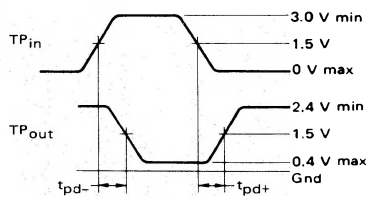
Positive Logic: $Z = \overline{A \bullet B}$
Negative Logic: $Z = \overline{A + B}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 35 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



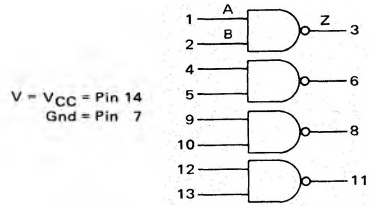
t+ = 12 ns
t- = 6.0 ns } 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$



R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

									TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
									mA	Volts											
									I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
								MC5403	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.50	5.50	
								MC7403	16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.75	5.25	Pin 7 is grounded for all tests in addition to the pins listed below:
			MC5403 Test Limits −55 to +125°C			MC7403 Test Limits 0 to +70°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Min	Max	Unit	I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	$V_{th\,1}$	$V_{th\,0}$	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	A	-	-	B	-	-	-	-	-	-	V	*
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc	-	-	A	-	-	-	-	-	-	-	-	V	B*
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	-	A	-	-	-	-	-	-	-	V	B*
Output Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	A,B	-	-	-	V	-	*
Output Leakage Current	I_{CEX}	Z	-	0.25	mAdc	-	0.25	mAdc	-	-	-	-	A	-	-	B	Z	-	V	-	*
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	V	-	22	mAdc	-	22	mAdc	-	-	-	-	-	All Inputs	-	-	-	-	-	V	-
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	V	A,B*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-
Turn-Off Delay	t_{pd+}	A,Z	-	45**	ns	-	45**	ns	A	Z	B	-	-	-	-	-	-	V	-	-	-

*Ground inputs to gates not under test.
**Tested only at 25°C.