MC68176

Advance Information

MC68176 2-BIT A/D CONVERTER IC

The MC68176 chip is part of a total solution available from Motorola for providing FLEX™ paging capabilities in a low-power, low-cost system. Working in conjunction with standard paging receivers, the MC68176 takes the 4-level baseband audio signals from the receiver and performs 2-bit A/D using 8-bit DACs for peak and valley detection, passing the 2-bit digital signal directly to the MC68175 FLEX chip or MC68181 Roaming FLEX chip for further decoding and FLEX protocol handling. Received messages are then passed to the host microcontroller or microprocessor via the Serial Peripheral Interface (SPI). The host processor (running FLEXstack™ software) interprets the data appropriately (as binary, alphanumeric or numeric message types), and handles all I/O and user interaction functions.

The FLEX paging protocol is the multi-speed, high-performance protocol adopted by leading service providers worldwide. FLEX protocol gives service providers the increased capacity, added reliability, and enhanced pager battery performance required today. It also provides an upward migration path to the service provider which is completely transparent to the end user.

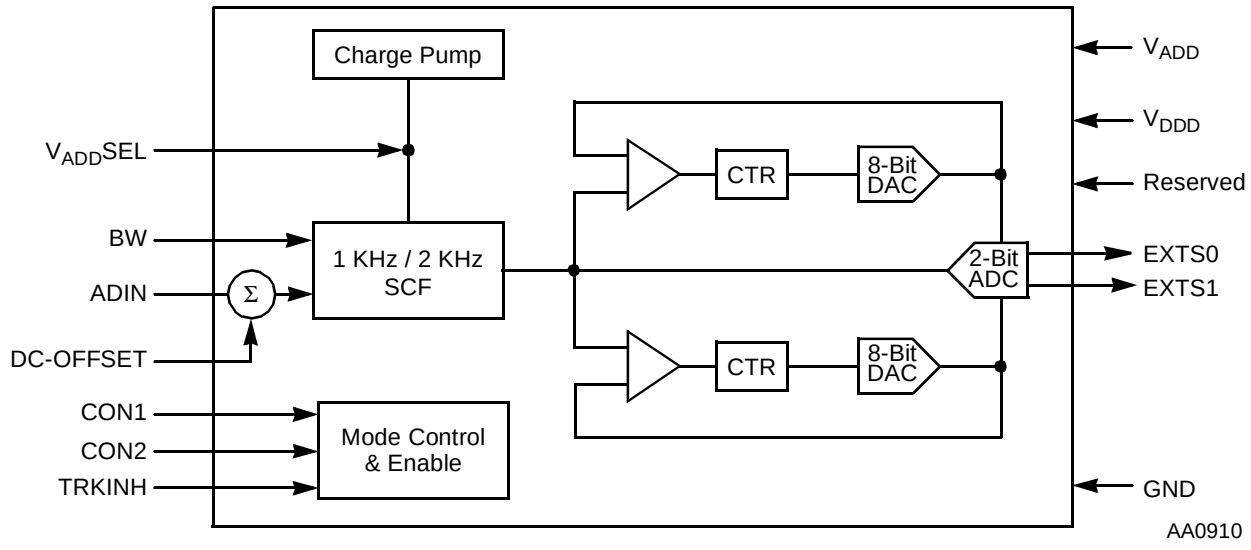

Figure 1 MC68176 Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

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Internet: http://www.motorola-dsp.com

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

- 2-bit A / D converter
- Supports FLEX Protocol with the MC68175 and MC68181 FLEX Decoder chips
- Peak and valley 8-bit DAC detectors compensate for signal strength variation
- Pin-selectable 2-Pole Butterworth Low Pass Filter
  - BW = 0: 1 Khz ± 5% (–3 dB) (for 1600 symbols / second)
  - BW = 1: 2 Khz ± 5% (–3 dB) (for 3200 symbols / second)
- 600 mV input voltage range @V_{ADD} = 2.7 V and 1.8 V
- 100 µA typical operating current @ V_{ADD} = 2.7 V
- Three Modes of Operation:
  - Fast Track mode
  - Slow Track mode
  - Hold Acquisition
- Standby mode for low power consumption
- –30 °C to 85 °C temperature range
- 2 V and 3 V operation ± 10% for both V_{DDD} and V_{ADD}
- Flexible supply mode (i.e., V_{ADD} can be at 2 V and V_{DDD} can be at 3 V or vice-versa)
- For V_{ADD} = 2 V, an internal charge pump is enabled to provide higher voltages for some analog circuits.
- 14-pin SOIC package

ADDITIONAL SUPPORT

FLEX System Software from Motorola is a family of software components for building world-class products incorporating messaging capabilities. FLEXstack™ Software is specifically designed to support the FLEX chip IC. FLEXstack Software runs on a product host processor and takes care of communicating with the FLEX chip IC and fully interpreting the codewords that are passed to the host from the FLEX chip IC.

DOCUMENTATION

This document is the primary document supporting the MC68176 FLEX 2-bit A / D. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the MC68176 are organized into six functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**.

Table 1-1 MC68176 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power and Reserved Signal	4	**Table 1-2**
Timing	1	**Table 1-3**
Analog Inputs	2	**Table 1-4**
Analog Controls	2	**Table 1-5**
Digital Outputs	2	**Table 1-6**
Digital Inputs	3	**Table 1-7**

Figure 1-1 on page 1-2 is a diagram of MC68176 signals by functional group.

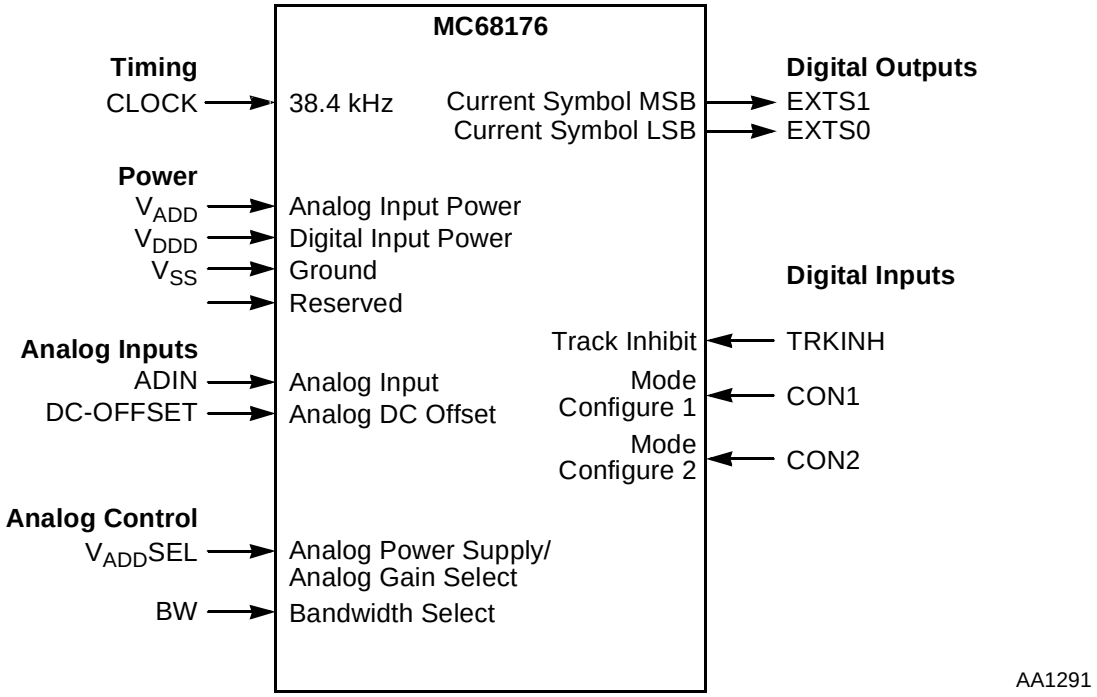


Figure 1-1 Signals Identified by Functional Group

POWER

Table 1-2 Power and Reserved Signal

Signal Name	Description
V_{ADD}	**Power**—V_{ADD} is the input power for the analog portion of the IC.
V_{DDD}	**Power**—V_{DDD} is the input power for the digital portion of the IC.
V_{SS}	**Ground**—V_{SS} is ground connection for the IC.
Reserved	**Reserved**—This pin must be connected to VSS to ensure proper operation

TIMING

Table 1-3 Timing Signal

Signal Name	Type	Signal Description
CLOCK	Input	**Clock Input**—This is a 38.4 kHz 50% duty cycle clock, typically provided by CLKOUT on the MC68175 FLEX chip or MC68181 Roaming FLEX chip.

ANALOG INPUTS

Table 1-4 Analog Input Signals

Signal Name	Type	Signal Description
ADIN	Input	**Analog Data In**—This is the 4-level baseband analog audio input signal to be digitized.
DC-OFFSET	Input	**DC Offse**t—This analog input signal is the dc content of the analog input signal ADIN. This pin needs a dc voltage (identical to the IF dc voltage content) applied to it, to prevent clipping of the ADIN input signal.

ANALOG CONTROL

Table 1-5 Analog Control Signals

Signal Name	Type	Signal Description
V_{ADD}SEL	Input	**V_{ADD} Select**—If V_{ADD} is nominal 3 V, set V_{ADD}SEL to 0. If V_{ADD} is nominal 2 V, set V_{ADD}SEL to 1. This signal has two functions—to enable a charge pump when V_{ADD} is 2 V, and to control the analog gain of the filter stage. If V_{ADD}SEL is 1, the charge pump is enabled, ensuring parts of the analog circuit have a higher supply. V_{ADD}SEL also controls the gain of the filter stage: V_{ADD}SEL = 0: gain = 3.656 V_{ADD}SEL = 1: gain = 2.437
BW	Input	**BandWidth Select**—This digital signal controls the cutoff frequency for the second-order low-pass Butterworth or Switched Capacitor filter: BW = 0: 1 kHz filter (for 1600 symbols / second) BW = 1: 2 kHz filter (for 3200 symbols / second)

DIGITAL OUTPUTS

Table 1-6 Digital Output Signals

Signal Name	Signal Type	Signal Description
EXTS0–1	Output	**Digitized Output bits**—These are the gray-scale encoded digitized representation of ADIN. The transition levels are relative to the measured peak and valley signal levels. EXTS0 = 1, EXTS1 = 0: 5/6 < ADIN < 1 EXTS0 = 1, EXTS1 = 1: 1/2 < ADIN < 5/6 EXTS0 = 0, EXTS1 = 1: 1/6 < ADIN < 1/2 EXTS0 = 0, EXTS1 = 0: 0 < ADIN < 1/6

DIGITAL INPUTS

Table 1-7 Digital Input Signals

Signal Name	Signal Type	Signal Description
CON0–1	Input	**Mode Configuration**—CON0 and CON1 specify the mode of operation for the MC68176. CON0 = 0, CON1 = 0: Lower Power Standby mode CON0 = 0, CON1 = 1: Fast Track mode CON0 = 1, CON1 = 0: Hold mode CON0 = 1, CON1 = 1: Slow Track mode
TRKINH	Input	**Track Inhibit**—This signal controls the operation of the peak and valley audio signal strength detectors. TRKINH is synchronized with the falling edge of CLOCK. TRKINH = 0: Enables peak and valley counters and enables decay. TRKINH = 1: Disables peak and valley counters and disables decay.

Note: All digital signals are latched on the falling edge of CLOCK except V_{ADD}SEL.

SECTION 2

SPECIFICATIONS

INTRODUCTION

The MC68176 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The MC68176 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., GND, V_{DDD} or V_{ADD}).

Table 2-1 Maximum Ratings

Spec.	Rating	Symbol	Value	Unit
M 1	Supply Voltage	V_{CC}	–0.3 to +3.3	V
M 2	All input voltages	V_{IN}	GND –0.5 to VCC +0.5	V
M 3	Current drain per pin excluding V_{DD} and V_{SS}	I	10	mA
M 4	Operating temperature range	T_A	–30 to +85	°C
M 5	Storage temperature	T_{STG}	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Table 2-2 Recommended Operating Conditions

Spec.	Characteristic	Symbol	Min	Typ	Max	Unit
1	Analog Supply Voltage (V_{ADD}SEL = 1)	V_{ADD}	1.8	2.0	2.2	V
2	Analog Supply Voltage (V_{ADD}SEL = 0)	V_{ADD}	2.7	3.0	3.3	V
3	Input Clock Frequency	CLOCK	—	38.4	—	kHz
4	Input Clock Duty Cycle	CLOCK	45	50	55	%
5	Operating Temperature	T_A	− 30	—	+ 85	°C

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Spec.	Characteristics	Symbol	Min	Typ	Max	Unit
6	Output high voltage (I_{OH} = – 0.3 mA, V_{DDD} = 3.0 V ± 10%)	V_{oh}	V_{DDD} − 0.13	—	—	V
7	Output high voltage (I_{OH} = – 0.3 mA, V_{DDD} = 2.0 V ± 10%)	V_{oh}	V_{DDD} − 0.3	—	—	V
8	Output low voltage (I_{OL} = 2 mA, V_{DDD} = 3.0 V ± 10%)	V_{oL}	—	—	0.13	V
8	Output low voltage (I_{OL} = 2 mA, V_{DDD} = 2.0 V ± 10%)	V_{oL}	—	—	0.3	V
10	Input high voltage	V_{ih}	$0.8 \times V_{DDD}$	—	V_{DDD}	V
11	Input low voltage	V_{il}	− 0.3	—	$0.2 \times V_{DDD}$	V
12	Digital Internal Supply Current (V_{DDD} = 3 V) ± 10%	IV_{DDD}	—	2.5	8.0	µA
13	Digital Internal Supply Current (V_{DDD} = 2 V ± 10%)	IV_{DDD}	—	1.6	5.3	µA
14	Analog Internal Supply Current (V_{ADD} = 3 V ± 10%, V_{ADD}SEL = 0)	I_{SBY}	—	110	220	µA
15	Analog Internal Supply Current (V_{ADD} = 2V ± 10%, V_{ADD}SEL = 1)	I_{SBY}	—	75	150	µA
16	Standby Supply Current	I_{SBY}	—	—	1	µA
17	Digital Input capacitance	C_{di}	—	—	10	pF
18	Analog Input capacitance	C_{ai}	—	—	10	pF
19	DC-OFFSET Range	V_{DCO}	0.0	—	V_{ADD}	V

PEAK AND VALLEY DAC

Table 2-4 Peak and Valley DAC

Spec.	Characteristic	Symbol	Min	Typ	Max	Unit
20	Specification Deleted					
21	DAC output voltage	—	IV_{AG} – 128 LSB	—	IV_{AG} + 128 LSB	V
22	Step Size (input referred)	LSB	$0.3367 \times V_{ADD} / 255 \pm 1\%$			V
23	Differential Linearity	—	—	—	1	LSB
24	Min / Max Full Scale Error	—	—	—	1	LSB
25	Zero Code Error	—	—	—	7	LSB
26	Voltage Output Drift, Hold mode	—	—	—	0.0	mV / mS
Note:	$IV_{AG} = (V_{ADD} / 2) \pm 1\%$					

SWITCH CAPACITOR FILTER

Table 2-5 Switch Capacitor Filter

Spec.	Characteristic	Symbol	Min	Typ	Max	Unit
27	Pass Band Gain (V_{ADD}SEL = 0)	—	11.16	11.26	11.36	dB
28	Pass Band Gain (V_{ADD}SEL = 1)	—	7.64	7.74	7.84	dB
29	Cutoff Frequency, – 3 dB, BW = 1	—	1.95	2.0	2.05	kHz
30	Cutoff Frequency, – 3 dB, BW = 0	—	0.95	1.0	1.05	kHz
31	Stabilization time, off mode to hold mode	—	—	—	5.0	mS
32	Analog Input Impedance (f_{IN} = 10 kHz)	Z_{IN}	1.0	—	—	MΩ
33	ADIN Voltage Range (See Note)	ADIN	0.0	—	V_{ADD}	V

Note: Although the voltage on ADIN may be any value in the range specified, the actual maximum permitted ac signal peak is given by:

$V_{ADIN\text{-}peak} = 0.410 \times V_{ADD} / SCFGAIN – V_{difoffset}$

where

$V_{difoffset} = |V_{ADoffset} – V_{DC\text{-}OFFSET}|$ (absolute value of error in signal DC-OFFSET)
$V_{ADoffset}$ = Actual dc offset of analog signal presented on ADIN
$V_{DC\text{-}OFFSET}$ = dc value present as signal DC-OFFSET

2-BIT A/D CONVERTER

Table 2-6 2-bit A/D Converter

Spec.	Characteristic	Min	Typ	Max	Unit
34	Lower Threshold	Valley + (Peak – Valley) × 1/6; ± 0.00625 @ Peak – Valley = 125 mV			V
35	Middle Threshold	Valley + (Peak – Valley) × 1/2; ± 0.00625 @ Peak – Valley = 125 mV			V
36	Upper Threshold	Valley + (Peak – Valley) × 5/6; ± 0.00625 @ Peak – Valley = 125 mV			V

Note: Maximum ac peak input voltage on ADIN
(V_{ADD}SEL = 1, SCFGAIN = 2.437 ± 1%) and (V_{ADD}SEL = 0, SCFGAIN = 3.656 ± 1%):

$V_{ADIN\text{-}peak}$ = $(0.410 \times V_{ADD} / SCFGAIN - V_{diffoffset})$

$V_{diffoffset}$ = $| V_{ADoffset} - V_{DC\text{-}OFFSET} |$

$V_{ADoffset}$ = dc value of the analog signal ADIN

$V_{DC\text{-}OFFSET}$ = Voltage of input offset signal DC-OFFSET.

($V_{diffoffset}$ is the absolute value of the difference between $V_{ADoffset}$ and $V_{DC\text{-}OFFSET,}$ that is the absolute value of the error in the input offset signal DC-OFFSET.)

TIMING DIAGRAMS

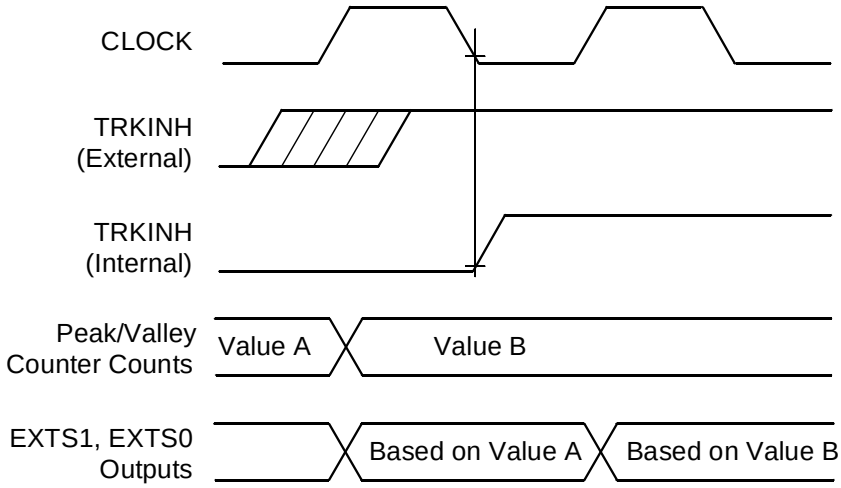


Figure 2-1 External Timings

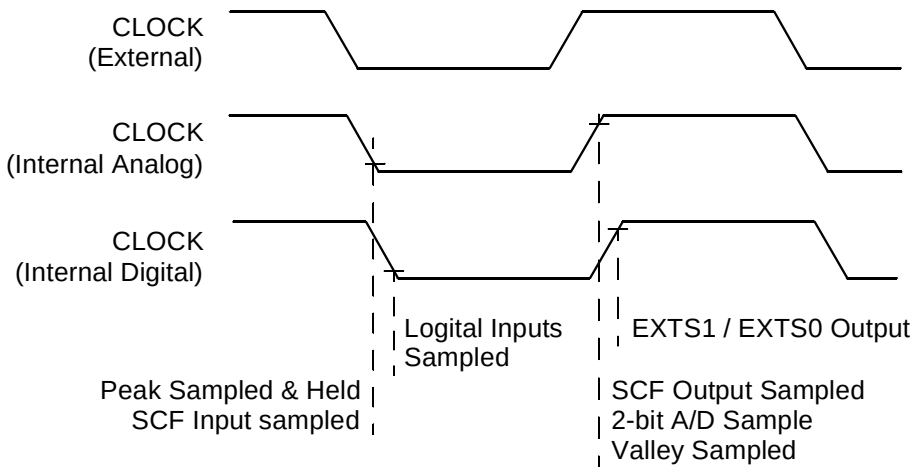


Figure 2-2 Internal Timings

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated. The MC68176 is available in a 14-pin Small Outline Integrated Circuit (SOIC) package.

TQFP Package Description

Top and bottom views of the SOIC package are shown in **Figure 3-1** and **Figure 3-2** with their pinouts.

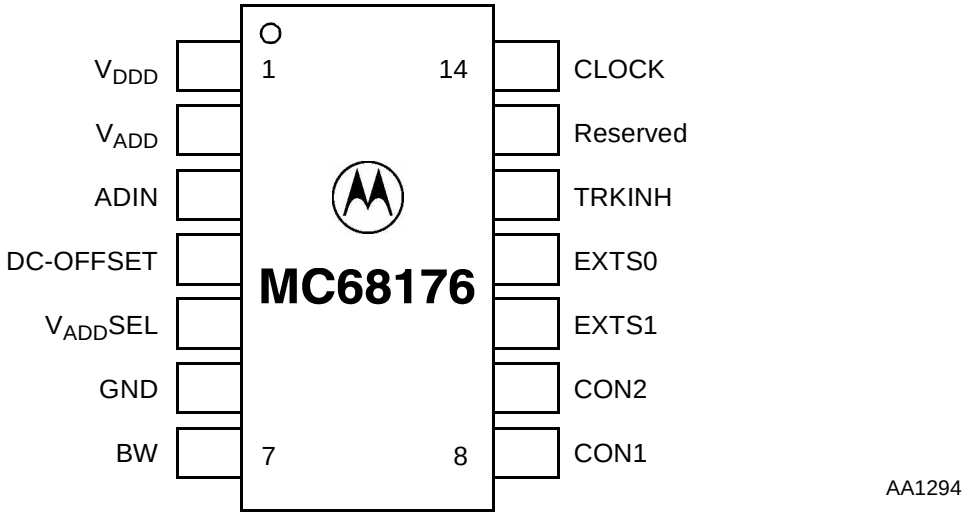


Figure 3-1 MC68176 Small Outline Integrated Circuit (SOIC), Top View

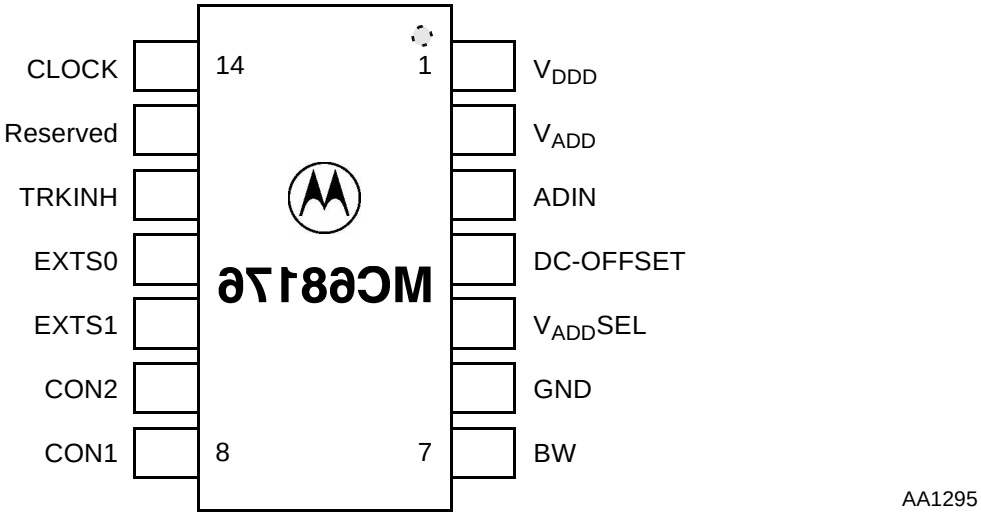


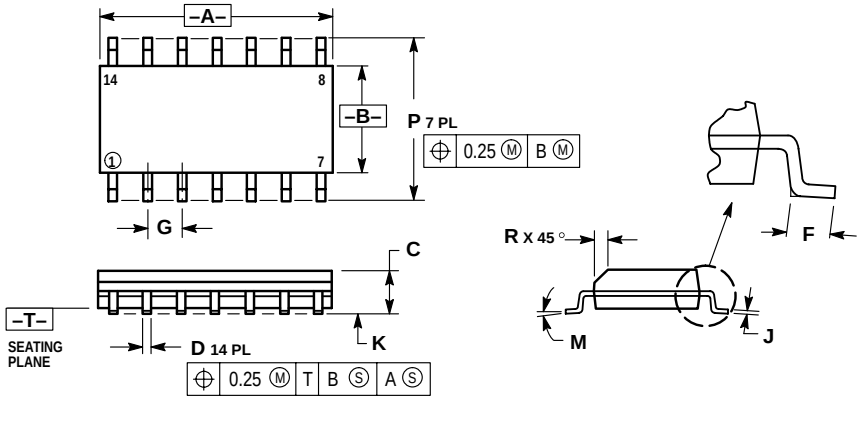
Figure 3-2 MC68176 Small Outline Integrated Circuit (SOIC), Bottom View

Table 3-1 Signal by Pin Number

Pin #	Signal Name	Pin #	Signal Name
1	V_{DDD}	8	CON1
2	V_{ADD}	9	CON2
3	ADIN	10	EXTS1
4	DC-OFFSET	11	EXTS0
5	V_{ADD}SEL	12	TRKINH
6	V_{SS}	13	Reserved
7	BW	14	CLOCK

Table 3-2 Signal by Name

Signal Name	Pin #	Signal Name	Pin #
ADIN	3	EXTS1	10
BW	7	Reserved	13
CLOCK	14	TRKINH	12
CON1	8	V_{ADD}	2
CON2	9	V_{ADD}SEL	5
DC-OFFSET	4	V_{DDD}	1
EXTS0	11	V_{SS}	6



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	8.55	8.75
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.19	0.25
K	0.10	0.25
M	0 °	7 °
P	5.80	6.20

Figure 3-3 14-pin Small Outline Integrated Circuit (SOIC) Mechanical Information

ORDERING DRAWINGS

Complete mechanical information regarding MC68176 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The MC68176 14-pin SOIC package mechanical drawing is referenced as 751-A.

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C / W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C / W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C / W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C / W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

APPLICATION DESIGN CONSIDERATIONS

The FLEX chip IC connects to a receiver capable of converting a four-level audio signal into a 2-bit digital signal with the MC68176 FLEX 2-bit D / A. The FLEX chip IC has eight receiver control lines used for warming up and shutting down a receiver in stages, dual bandwidth control signals for two post detection filter bandwidths for receiving the two symbol rates of the FLEX signal, and the ability to detect a low battery signal during the receiver control sequences. It interfaces to a host MCU through a standard SPI. It has a 38.4 kHz clock output capable of driving other devices, in particular the MC68176. It has a 1 minute timer that offers low power support for time of day function on the host. **Figure 4-1** shows a typical application block diagram.

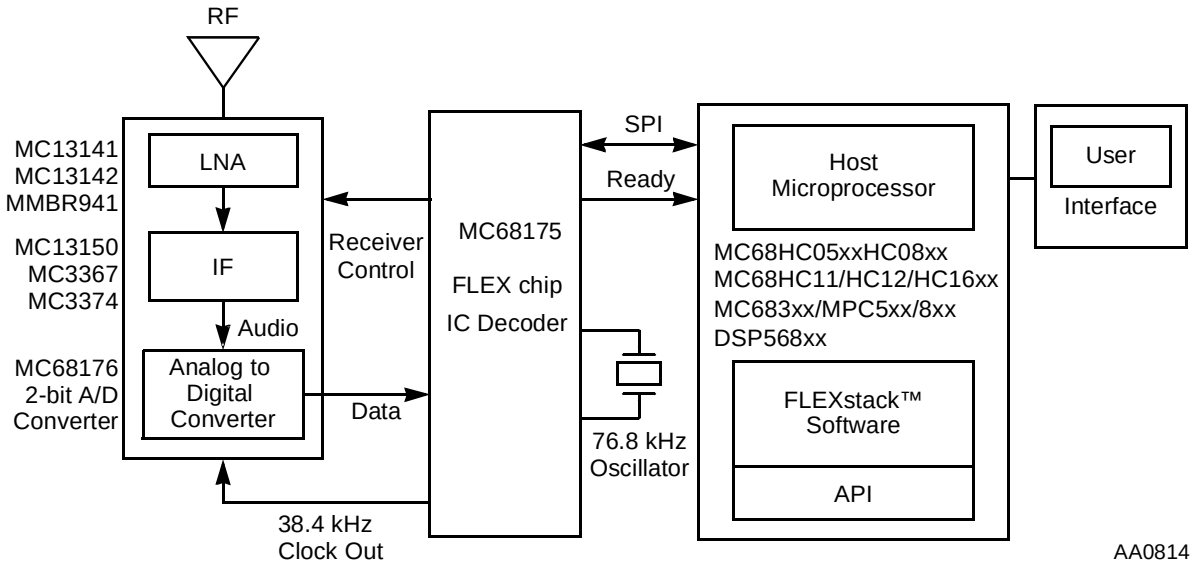


Figure 4-1 FLEX chip System Block Diagram

Sample Application Circuit

Figure 4-2 shows an application example of the MC68176 2-bit FLEX A / D chip in a FLEX pager application. The MC68176 A / D chip will convert an analog FLEX base-band signal into a 2-bit digital signal. The MC68176 A / D can be controlled by a FLEX decoder, such as the MC68175 or MC68181. The following schematic shows the MC68176 A / D chip in a pager application.

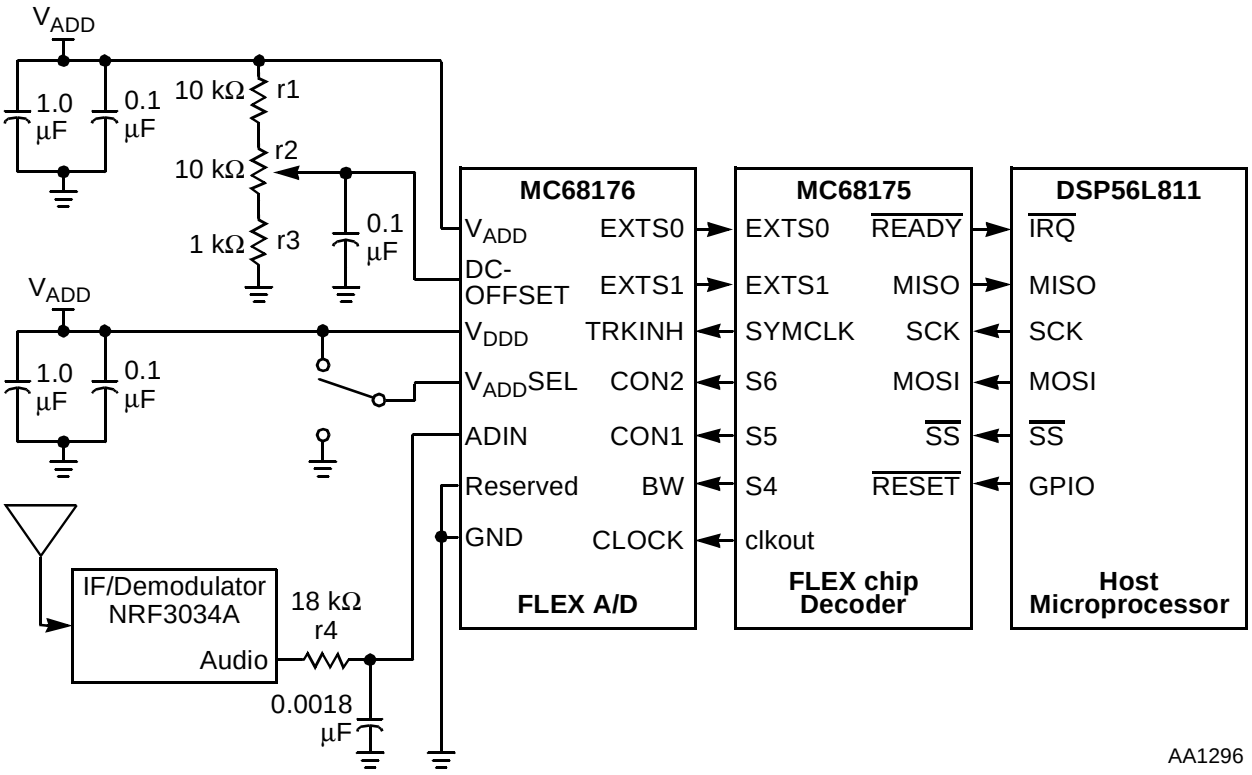


Figure 4-2 An Application Example for the MC68176, FLEX A/D

Note that the dc offset of the audio input signal to the FLEX A / D must be applied to the DC-OFFSET pin for the converter to work properly. Theoretically speaking, we can view the DC-OFFSET pin as an internal resistance of 50 kΩ and a internal capacitance of 1.6 pF in serial. So, the external resisters, r1, r2, and r3 can be as large as 600 kΩ, 600 kΩ, and 60 kΩ, respectively— this will guarantee settling to an accuracy of at least 9 bits.

SECTION 5

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (KHz)	Order Number
MC68176	1.8 V—3.3 V (see Note 1)	SOIC	14	38.4	MC68176DW

Note: 1. The MC68176 has two separate power rails for the analog and digital portions of the circuitry, V_{ADD} and V_{DDD}. Both rails may be set independently to a nominal 2.0 V or 3.0 V supply.

APPENDIX A
DESCRIPTION OF OPERATION

OPERATIONAL DESCRIPTION

The MC68176 is a four-level audio band 2-bit A/D symbol decoder for the FLEX paging system. The input signal to the ADIN pin is generated by a FLEX RF receiver. There are four amplitude levels, which represent four unique output digital codes. The digital levels are defined relative to the peak and valley voltages of the signal.

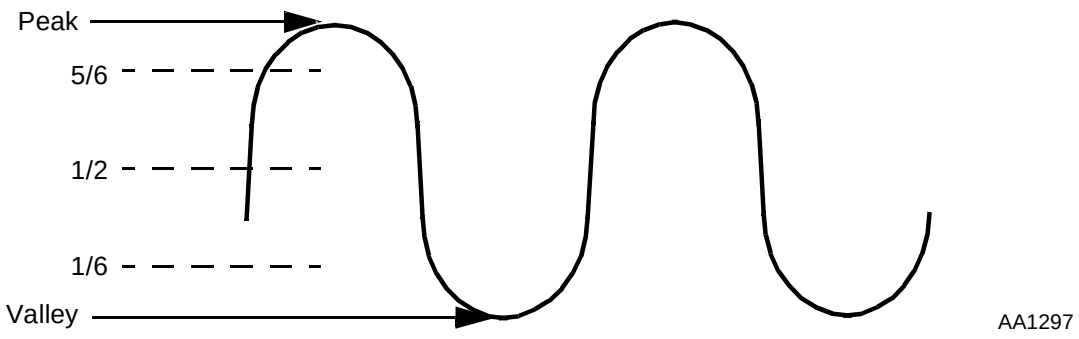


Figure A-1 ADIN Analog Input Signal

The ideal digital transition levels are at the following thresholds:

- Upper Threshold = (Peak – Valley) × 5 / 6 + Valley
- Middle Threshold = (Peak – Valley) × 1 / 2 + Valley
- Lower Threshold = (Peak – Valley) × 1 / 6 + Valley

The Gray scale regions are shown in **Table A-1** on page A-2.

Table A-1 Gray Scale Regions

Signal Range	EXTS1, EXTS0
Peak	
	1, 0
5/6	
	1, 1
1/2	
	0, 1
1/6	
	0, 0
Valley	

Each threshold in **Table A-1** must be accurate to within 5% of the ideal threshold, or the FLEX bit error rate will increase beyond acceptable levels.

The problem is that both the amplitude and the dc offset of the received signal will be affected by many variables—temperature, voltage, production lot, vendor, and receiver design. Because of this increase in the dynamic range, an 8-bit DAC is required for both the peak and valley servo loops. This means that the peak and valley levels used by the MC68176 are within one LSB of the actual peak and valley voltage levels.

Peak and Valley Servo Description

A control loop is used to acquire the actual Peak and Valley voltages to an accuracy of one LSB. The Peak control loop is described below; the Valley control loop is similar, with appropriate changes made to acquire a minimum rather than a maximum signal value.

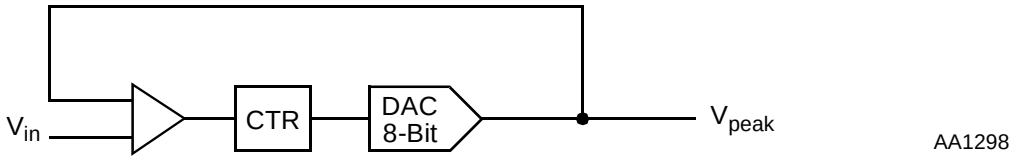


Figure A-2 Peak/Valley Control Loop

The FLEX system uses a symbol rate of 1600 symbols per second during the synchronization period. The MC68176 must acquire the Peak and Valley levels in six symbol periods, with sufficient accuracy that the threshold levels used by the two-bit A/D are within 5% of the actual thresholds.

There are two tracking modes, Fast Track mode and Slow Track mode. The use of these two modes allows the threshold specification to be acquired in the required six symbol periods, that is 6/1600 seconds or six times 625 µS. Fast Track mode is used for one symbol period to obtain a very approximate value quickly, and Slow Track mode is used for the remaining five periods to obtain an accurate value. In both Fast Track mode and Slow Track mode, the Control loop acquires the Peak and Valley by attacking or decaying the Peak counter at different rates.

In Fast Track mode, tracking is controlled only by the relative levels of the two signals V_{in} and the Peak DAC output. If the Peak DAC output is above V_{in}, then the Peak counter will decay, and if it is below V_{in}, then the Peak counter will attack.

Slow Track mode is a little more complicated. For the Peak counter to decay, TRKINH must be low (i.e., tracking is not inhibited), the Peak DAC output must be greater than V_{in}, and no attack or decay may have happened for a set number of CLOCK cycles. If all these conditions are met, then the Peak DAC is decremented. The Peak counter is incremented if TRKINH is low and the Peak DAC output is less than V_{in}.

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