Freescale Semiconductor, Inc.

MOTOROLA

Microprocessor and Memory Technologies Group

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MC68302/D
Rev. 3

MC68302

Product Brief

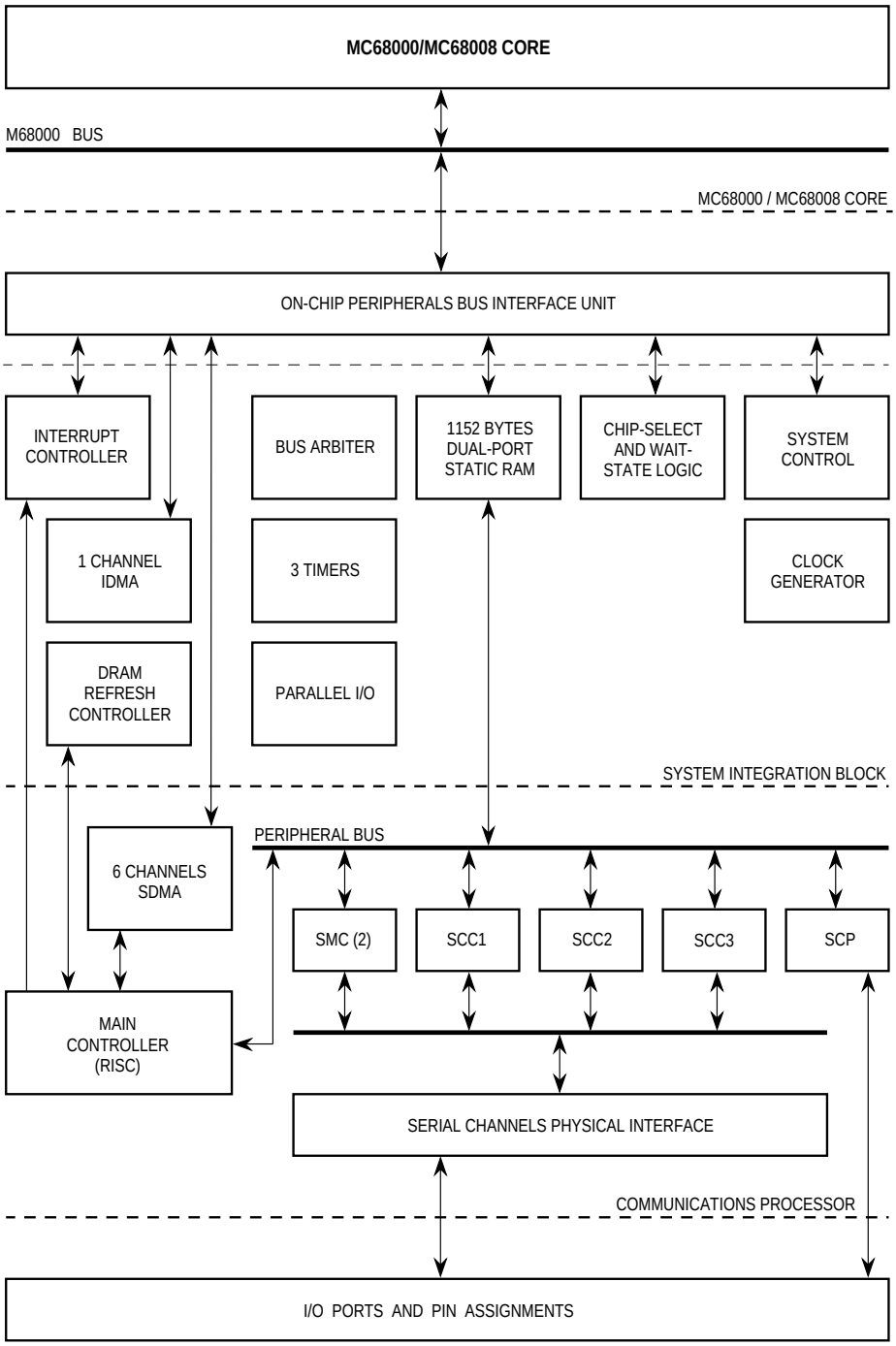
Integrated Multiprotocol Processor (IMP)

The IMP is a VLSI device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suited to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard, MC68000/MC68008 microprocessor core and a flexible communications architecture. This multichannel communications device may be configured to support a number of popular industry-standard interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adapter applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the IMP. Data concentrators, modems, line cards, bridges, and gateways are examples of suitable applications for this versatile device. The IMP is an HCMOS device consisting of an MC68000/MC68008 microprocessor core, a system integration block (SIB), and a communications processor (CP).

The main features of the IMP are as follows:

- MC68000/MC68008 Microprocessor Core (May Be Disabled to Use the IMP As a Peripheral)
- SIB Including:
  - — Independent Direct Memory Access (IDMA) Controller
  - — Interrupt Controller with Two Modes of Operation
  - — Parallel I/O Ports, Some with Interrupt Capability
  - — On-Chip 1152 Bytes of Dual-Port RAM
  - — Three Timers, Including a Software Watchdog Timer
  - — Four Programmable Chip-Select Lines with Wait-State Logic
  - — Programmable Address Mapping of Dual-Port RAM and IMP Registers
  - — On-Chip Clock Generator with an Output Clock Signal
  - — System Control
    - –System Control Register
    - –Bus Arbitration Logic with Low Interrupt Latency Support
    - –Hardware Watchdog for Monitoring Bus Activity
    - –Low Power (Standby) Modes
    - –Disable CPU Logic (M68000)
    - –Freeze Control for Debugging Selected On-Chip Peripherals
    - –DRAM Refresh Controller
- CP Including:
  - — Main Controller (RISC Processor)
  - — Three Full-Duplex Serial Communication Controllers (SCCs) with the Following Protocols:
    - –HDLC/SDLC
    - –Bisync
    - –UART
    - –DDCMP
    - –Totally Transparent
    - –V.110

— Six Serial DMA Channels Dedicated to the Three SCCs
— Capability To Send /Receive Up to Eight Buffers/Frames without M68000 Core Intervention
— Flexible Physical Interface Accessible by SCCs for Interchip Digital Link (IDL), General Circuit Interface (GCI, also called IOM2), Pulse Code Modulation (PCM), and Nonmultiplexed Serial Interface (NMSI) Operation
— Serial Communication Port (SCP) for Synchronous Communication
— Serial Management Controllers (SMCs) for IDL and GCI Channels



MC68302 Block Diagram

The MC68302 uses a microprocessor architecture that has serial channels connected to the system bus through a dual-port memory. Various parameters, counters, and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffers may be located in this on-chip RAM or in the off-chip system RAM. Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If an SCC channel's data is programmed to be located in the external RAM, the CP main controller (RISC processor) will automatically program the corresponding DMA channel to perform the required accesses. If the data resides in the on-chip dual-port RAM, then the CP main controller accesses the RAM with one clock cycle access and no arbitration delays.

The buffer memory structure of the MC68302 can be configured by software to closely match I/O channel requirements. The interrupt structure is also programmable to relieve the on-chip MC68000/MC68008 core from bit manipulation functions for peripherals, allowing the processor more time to perform application software or protocol processing. In some cases, the interface to equipment or proprietary networks may require the use of standard control and data signals. For these signals, the MC68302 can be programmed to use the NMSI mode. This mode is available for one, two, or all three SCC ports; remaining ports may then optionally use one of the multiplexed interface modes: IDL, GCI, or PCM.

The main controller is a microcoded RISC processor that services all the serial channels. The main controller transfers data between the serial channels and internal/external RAM, executes host commands, and generates interrupts to the interrupt controller. The MC68302 core processor allows operation either in the full MC68000 mode with a 16-bit data bus or in the MC68008 mode with an 8-bit data bus.

The MC68302 has an SIB that simplifies the task of hardware and software design. The IDMA controller eliminates the need for an external DMA controller on the system board. In addition, there is an interrupt controller that can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Similarly, the chip-select signals and wait-state logic eliminate the need to generate these signals externally. The SIB includes the IDMA controller, interrupt controller, parallel I/O ports, dual-port RAM, three timers, chip-select logic, clock generator, and system control.

The MC68302 has one IDMA channel and six serial DMA channels that operate concurrently with other CPU operations. The IDMA can operate in different modes of data transfer as programmed by the user. The six serial DMA channels for the three full-duplex SCC channels are transparent to the user, implementing bus-cycle-stealing data transfers controlled by the MC68302 internal RISC controller. These six channels have priority over the separate IDMA channel. The IDMA controller can transfer data between any combination of memory and I/O devices.

The interrupt controller, which manages the priority of internal and external interrupt requests, generates a vector number during the CPU interrupt acknowledge cycle. Nested interrupts are fully supported.

The IMP has 1152 bytes of RAM configured as a dual-port memory. The RAM can be accessed by the internal RISC controller or one of three bus masters: the M68000 core, an external bus master, or the IDMA. All internal bus masters synchronously access the RAM with no wait states. External bus masters can access the RAM and registers synchronously or asynchronously. The RAM is divided into two parts. There are 576 bytes used as a parameter RAM, which includes pointers, counters, and registers for the serial ports. The other 576 bytes may be used for system RAM, which may include data buffers, or may be used for other purposes such as RAM for downloadable microcode packages provided by Motorola.

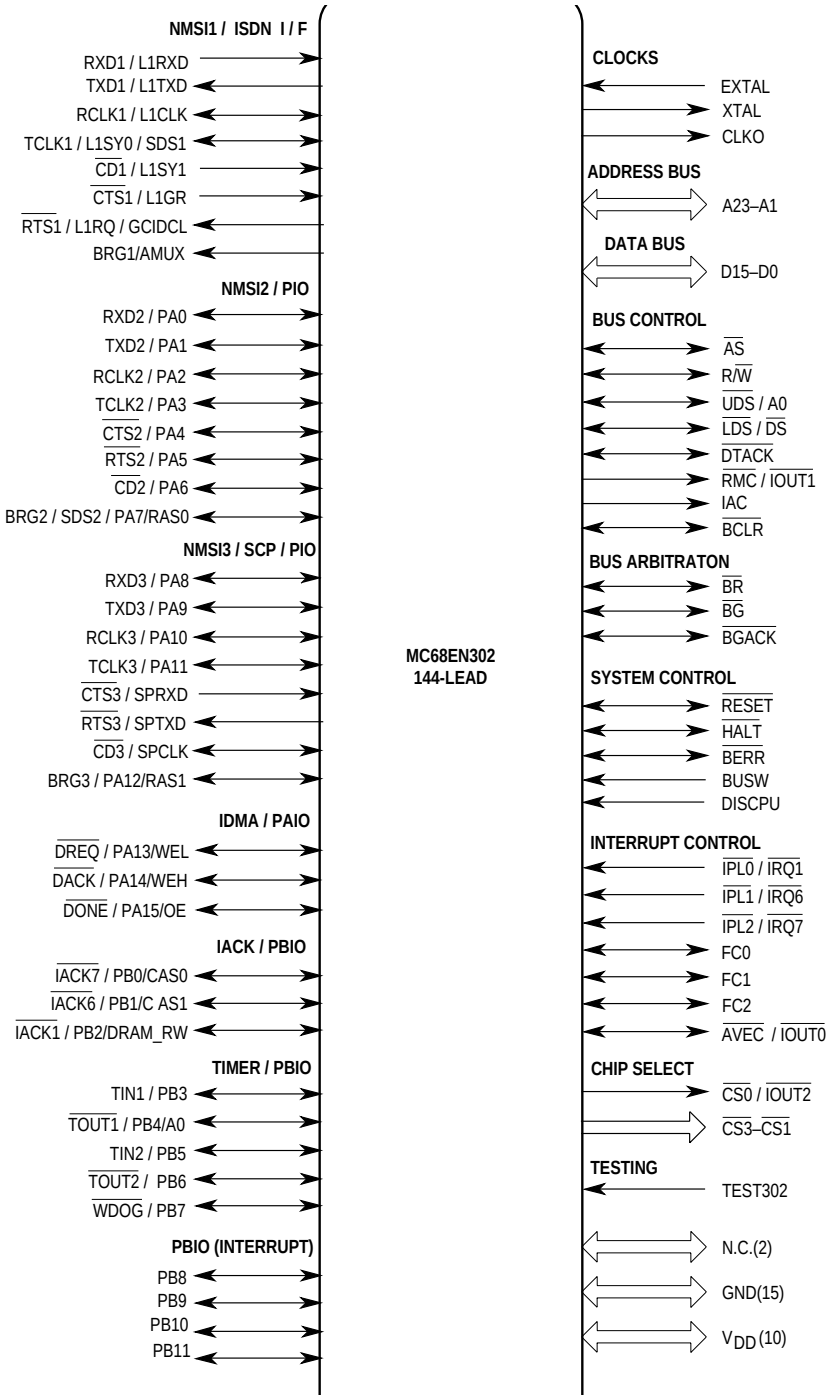
Port A and port B are two general-purpose I/O ports, with 16 and 12 pins, respectively.

There are three timer units. Two units are identical, general-purpose timers; the third unit can be used to implement a watchdog timer function.

The MC68302 has a set of four programmable chip-select signals. Each chip select has an identical structure. For each memory area, an internally generated cycle-termination signal (DTACK) may be defined with up to

six wait states to avoid using board space for cycle-termination logic. The four signals may each support four different classes of memory, such as high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. The chip-select and wait-state generation logic is active for all potential bus masters.

The MC68302 has an on-chip clock generator that supplies internal and external high-speed clocks (up to 20 MHz).



Functional Signal Groups

The following table identifies the packages and operating frequencies available for the MC68302.

MC68302 Package/Frequency Availability

Package	Frequency	
	16.67 MHz	20 MHz
Surface Mount	•	•
Pin Grid Array	•	•

The documents listed in the following table contain information on the MC68302. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of the last page of this document.

Related Documentation

Document Title	Order Number	Contents
MC68302 User's Manual	MC68302UM/AD	Detailed information for design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
M68000 8-/16-/32-Bit Microprocessors User's Manual	MC68000UM/AD	Detailed information for design
MC68195 LocalTalk Adapter Product Brief	MC68195/D	Related Product Information
MC68302 Development Support	BR469	Development Support for MC68302
The 68K Source	BR729/D, Rev 1	Independent vendor listing supporting software and development tools

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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