

## **MC68HC11EA9** **MC68HC711EA9**

### *Product Preview*

### **8-bit HCMOS Single-Chip Microcontroller with A/D converter**

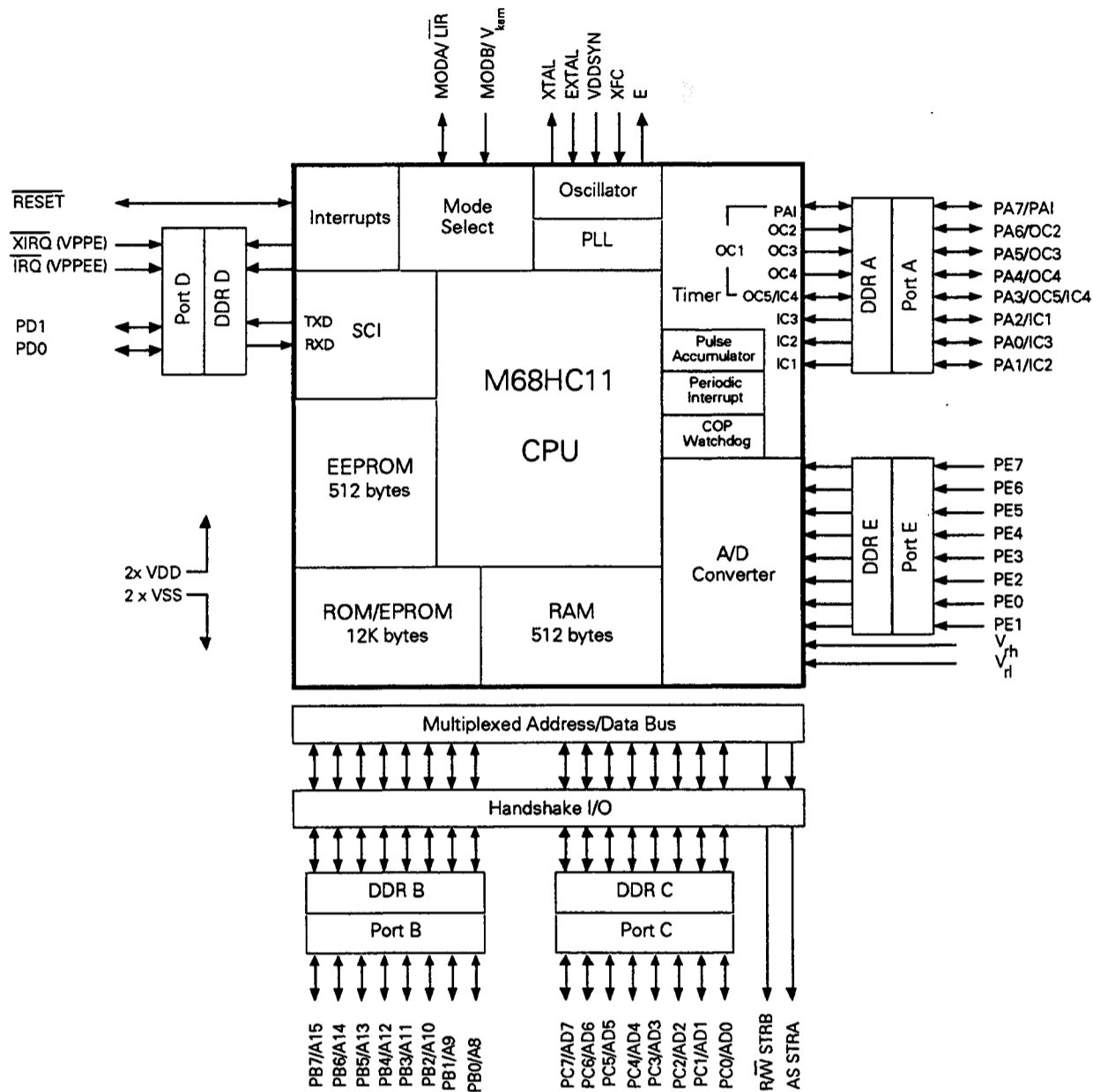
The MC68HC11EA9, with 12 kbytes of ROM, and the MC68HC711EA9, with 12 kbytes of EPROM, are high-performance microcontroller units based on the Motorola M68HC11 CPU core. Their hardware features make these devices suitable for use in a wide range of application areas including automotive and communications. Features common to both devices include a phase-lock-loop clock circuit, Serial Communications Interface (SCI) with 13-bit modulus prescaler, 16-bit timer with multiple input capture and output compare functions, 8-bit pulse accumulator, 8-channel A/D converter and a Computer Operating Properly (COP) watchdog timer. The phase-lock-loop clock circuit with its automatic disable capability during WAIT mode, combined with the pull-up loads on Ports A, B, C and D and the A/D converter, make the parts ideally suited to automotive body electronics applications such as air conditioning, automatic window mechanisms and central door locking, where the system is required to react to changes in speed/temperature or keypad activity. Another notable feature of these devices is their UART communication capability which, coupled with the A/D converter and the bi-directional parallel ports, makes them ideal for industrial control/communication environments. Both devices can operate in expanded multiplexed mode where they are capable of accessing a 64 kbyte address space.

The main features of the devices are listed below:

- Fully static design featuring the M68HC11 family CPU core with 2.1 MHz bus frequency
- Single-Chip, Expanded and Bootstrap modes of operation
- 64K addressing capability in expanded mode
- Power-saving phase-lock-loop (PLL) clock circuit with software selectable voltage-controlled oscillator
- Low-noise power supply and external filter capacitor can be connected using VDDSYN and XFC input pins, thus minimising distortion of the voltage-controlled oscillator
- E-clock output with software disable
- 12 kbytes of mask-programmable ROM (MC68HC11EA9) or 12 kbytes of EPROM (MC68HC711EA9)
- 512 bytes of EEPROM with block protection for enhanced security
- 512 bytes of RAM
- Power saving STOP and WAIT modes
- Automatic phase-lock-loop disable during WAIT mode, further reducing power consumption
- 16-bit timer with four-stage programmable prescaler, four output compare functions, three input capture functions and one software-selectable input capture or output compare channel
- 8-bit Pulse Accumulator
- Real Time Interrupt circuit
- Eight channel, 8-bit Analog-to-Digital (A/D) converter
- Computer Operating Properly (COP) watchdog timer
- Serial Communications Interface with 13-bit modulus prescaler for baud rate control, idle mode detect, receiver active flag and hardware parity circuit
- Three 8-bit bi-directional parallel ports, one 8-bit input-only port and one 2-bit bi-directional port
- Pull-up loads active in input mode on Ports A, B, C and D
- Two Interrupt Request inputs, one of which is non-maskable, plus 13 on-board hardware interrupt sources and one non-maskable software interrupt source (SWI)
- Both Interrupt Request inputs can be used as general purpose inputs using the Interrupt Request disable function in the Port D Data Direction register
- 52-pin PLCC and 56-pin SDIP packages

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**Functional Block Diagram**

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